11.41 REGISTER 116 – FIFO READ WRITE

Register Name: FIFO_R_W

Register Type: READ/WRITE

Register Address: 116 (Decimal); 74 (Hex)

BIT	NAME	FUNCTION
[7:0]	FIFO_DATA[7:0]	Read/Write command provides Read or Write operation for the FIFO.

Description:

This register is used to read and write data from the FIFO buffer.

Data is written to the FIFO in order of register number (from lowest to highest). If all the FIFO enable flags (see below) are enabled, the contents of registers 59 through 72 will be written in order at the Sample Rate.

The contents of the sensor data registers (Registers 59 to 72) are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN (Register 35).

If the FIFO buffer has overflowed, the status bit *FIFO_OFLOW_INT* is automatically set to 1. This bit is located in INT_STATUS (Register 58). When the FIFO buffer has overflowed, the oldest data will be lost and new data will be written to the FIFO unless register 26 CONFIG, bit[6] FIFO_MODE = 1.

If the FIFO buffer is empty, reading register FIFO_DATA will return a unique value of 0xFF until new data is available. Normal data is precluded from ever indicating 0xFF, so 0xFF gives a trustworthy indication of FIFO empty.

11.42 REGISTER 117 – WHO AM I

Register Name: WHO_AM_I

Register Type: READ only

Register Address: 117 (Decimal); 75 (Hex)

BIT	NAME	FUNCTION
[7:0]	WHOAMI	Register to indicate to user which device is being accessed.

This register is used to verify the identity of the device. The contents of *WHOAMI* is an 8-bit device ID. The default value of the register is 0x11. This is different from the I^2C address of the device as seen on the slave I^2C controller by the applications processor. The I^2C address of the ICM-20600 is 0x68 or 0x69 depending upon the value driven on AD0 pin.

11.43 REGISTERS 119, 120, 122, 123, 125, 126 ACCELEROMETER OFFSET REGISTERS

Register Name: XA_OFFSET_H

Register Type: READ/WRITE

Register Address: 119 (Decimal); 77 (Hex)

BIT	NAME	FUNCTION
[7:0]	XA_OFFS[14:7]	Upper bits of the X accelerometer offset cancellation. ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps

Register Name: XA_OFFSET_L

Register Type: READ/WRITE

Register Address: 120 (Decimal); 78 (Hex)

BIT	NAME	FUNCTION
[7:1]	XA_OFFS[6:0]	Lower bits of the X accelerometer offset cancellation. ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps
[0]	-	Reserved.

Register Name: YA_OFFSET_H

Register Type: READ/WRITE

Register Address: 122 (Decimal); 7A (Hex)

BIT	NAME	FUNCTION
[7:0]	YA_OFFS[14:7]	Upper bits of the Y accelerometer offset cancellation. ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps