**CSC 411** 

Computer Organization (Spring 2023)
Lecture 6: RISC-V Memory Organization

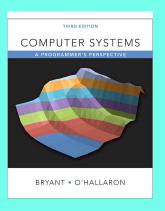
Prof. Marco Alvarez, University of Rhode Island

## **Disclaimer**

Some of the following slides are copied from:

Computer Systems (Bryant and O'Hallaron)

A Programmer's Perspective



## **Byte-Oriented Memory Organization**



#### ■ Programs refer to data by address

- Imagine all of RAM as an enormous array of bytes
- An address is an index into that array
  - A pointer variable stores an address

#### ■ System provides a private address space to each "process"

- A process is an instance of a program, being executed
- An address space is one of those enormous arrays of bytes
- Each program can see only its own code and data within its enormous array
- We'll come back to this later ("virtual memory" classes)

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#### **Machine Words**

- Any given computer has a "Word Size"
  - Nominal size of integer-valued data
    - and of addresses
  - Until recently, most machines used 32 bits (4 bytes) as word size
    - Limits addresses to 4GB (2<sup>32</sup> bytes)
- Increasingly, machines have 64-bit word size
  - Potentially, could have 18 EB (exabytes) of addressable memory
  - That's 18.4 X 10<sup>18</sup>
- Machines still support multiple data formats
  - Fractions or multiples of word size
  - Always integral number of bytes

Bryant and O'Hallaron, Computer Systems: A Programmer's Perspective, Third Edition

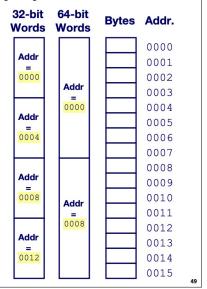
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# Addresses Always Specify Byte Locations

- Address of a word is address of the first byte in the word
- Addresses of successive words differ by 4 (32-bit) or 8 (64-bit)



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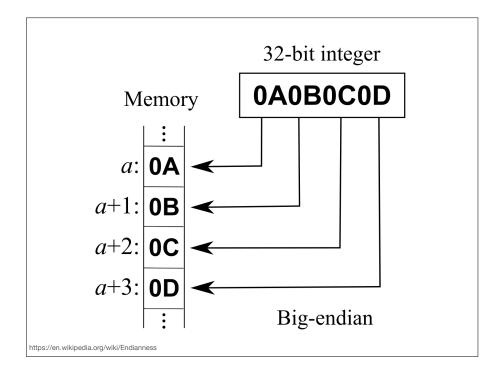
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#### **Example Data Representations** Typical 32-bit Typical 64-bit C Data Type x86-64 char 1 1 1 short 2 2 2 int long 8 float double pointer Bryant and O'Hallaron, Computer Systems: A Programmer's Perspective, Third Edition

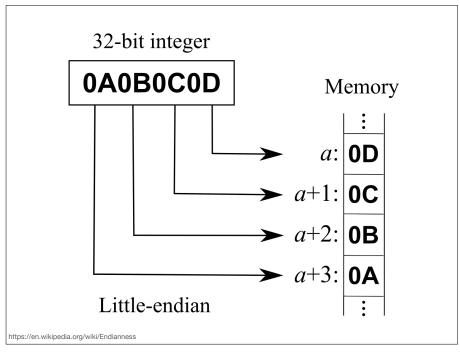
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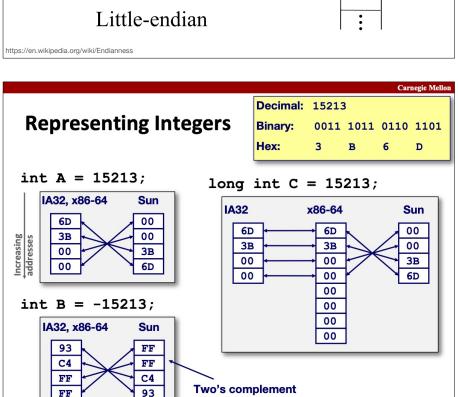
# **Byte Ordering**

- So, how are the bytes within a multi-byte word ordered in memory?
- Conventions
  - Big Endian: Sun, PPC Mac, network packet headers
    - Least significant byte has highest address
  - Little Endian: x86, ARM processors running Android, iOS, and Windows
    - Least significant byte has lowest address



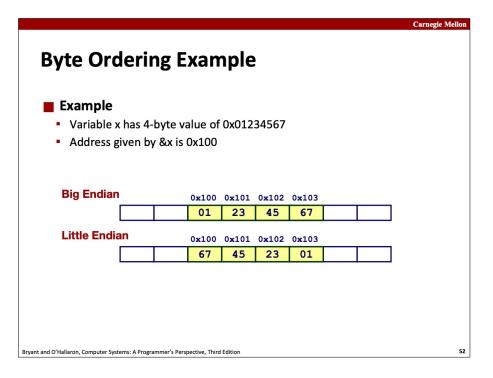
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representation

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# Examining Data Representations ■ Code to Print Byte Representation of Data

Casting pointer to unsigned char \* allows treatment as a byte array

```
typedef unsigned char *pointer;

void show_bytes(pointer start, size_t len) {
    size_t i;
    for (i = 0; i < len; i++)
        printf("%p\t0x%.2x\n", start+i, start[i]);
    printf("\n");
}</pre>
```

#### **Printf directives:**

%p: Print pointer
%x: Print Hexadecimal

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# show\_bytes Execution Example

```
int a = 15213;
printf("int a = 15213;\n");
show_bytes((pointer) &a, sizeof(int));
```

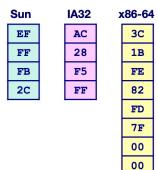
#### Result (Linux x86-64):

```
int a = 15213;
0x7fffb7f71dbc 6d
0x7fffb7f71dbd 3b
0x7fffb7f71dbe 00
0x7fffb7f71dbf 00
```

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**Representing Pointers** 

int 
$$B = -15213;$$
  
int \*P = &B



Different compilers & machines assign different locations to objects Even get different results each time run program

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# **Representing Strings**

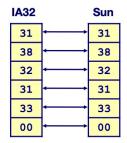
#### **■ Strings in C**

Represented by array of characters

- Each character encoded in ASCII format
  - Standard 7-bit encoding of character set
  - Character "0" has code 0x30
    - Digit i has code 0x30+i
- String should be null-terminated
  - Final character = 0

#### Compatibility

Byte ordering not an issue



char S[6] = "18213";

ASCII control characters				ASCII printable characters						Extended ASCII characters							
00	NULL	(Null character)		32	space	64	@	96	•	128	Ç	160	á	192	L	224	Ó
01	SOH	(Start of Header)		33	1	65	A	97	a	129	ű	161	í	193	1	225	ß
02	STX	(Start of Text)		34	"	66	В	98	b	130	é	162	Ó	194	т	226	Ô
03	ETX	(End of Text)		35	#	67	С	99	C	131	â	163	ú	195	-	227	Ò
04	EOT	(End of Trans.)		36	\$	68	D	100	d	132	ä	164	ñ	196	_	228	ő
05	ENQ	(Enquiry)		37	%	69	E	101	e	133	à	165	Ñ	197	+	229	Õ
06	ACK	(Acknowledgement)		38	&	70	F	102	f	134	å	166	a	198	ã	230	- 1
07	BEL	(Bell)		39		71	G	103	g	135	ç	167	0	199	Ã	231	į.
80	BS	(Backspace)		40	(	72	Н	104	h	136	ê	168	3	200	L	232	
09	HT	(Horizontal Tab)		41	)	73	- 1	105	i	137	ë	169	®	201	1	233	Ú
10	LF	(Line feed)		42	*	74	J	106	j	138	è	170	7	202	Ţŗ	234	- (
11	VT	(Vertical Tab)		43	+	75	K	107	k	139	Ϋ́	171	1/2	203	TF	235	Ü
12	FF	(Form feed)		44	,	76	L	108	- 1	140	î	172	1/4	204	Ţ	236	,
13	CR	(Carriage return)		45		77	M	109	m	141	ì	173	i	205		237	1
14	SO	(Shift Out)		46		78	N	110	n	142	Ä	174	<b>«</b>	206	#	238	
15	SI	(Shift In)		47	1	79	0	111	0	143	Α	175	>>	207	п	239	
16	DLE	(Data link escape)		48	0	80	Р	112	р	144	É	176		208	ð	240	
17	DC1	(Device control 1)		49	1	81	Q	113	q	145	æ	177	- 1	209	Ð	241	
18	DC2	(Device control 2)		50	2	82	R	114	r	146	Æ	178		210	Ê	242	
19	DC3	(Device control 3)		51	3	83	S	115	S	147	ô	179	T	211	Ë	243	3
20	DC4	(Device control 4)		52	4	84	Т	116	t	148	Ö	180	-	212	È	244	•
21	NAK	(Negative acknowl.)		53	5	85	U	117	u	149	ò	181	Á	213	1	245	
22	SYN	(Synchronous idle)		54	6	86	٧	118	V	150	û	182	Â	214	ĺ	246	
23	ETB	(End of trans. block)		55	7	87	W	119	w	151	ù	183	À	215	î	247	
24	CAN	(Cancel)		56	8	88	X	120	X	152	ÿ	184	©	216	ï	248	
25	EM	(End of medium)		57	9	89	Υ	121	У	153	Ö	185	4	217	ı,	249	
26	SUB	(Substitute)		58	:	90	Z	122	z	154	Ü	186		218	г	250	
27	ESC	(Escape)		59	;	91	[	123	{	155	Ø	187	j	219		251	
28	FS	(File separator)		60	<	92	Ī	124	T.	156	£	188	J	220	-	252	
29	GS	(Group separator)		61	=	93	]	125	}	157	Ø	189	¢	221	T	253	
30	RS	(Record separator)		62	>	94	۸	126	~	158	×	190	¥	222	i	254	
31	US	(Unit separator)		63	?	95	_			159	f	191	7	223		255	nb
127	DEL	(Delete)															

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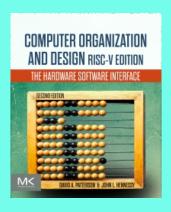
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Computer Organization and Design (Patterson and Hennessy)

The Hardware/Software Interface



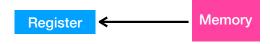
# Memory operands

# **Data transfer instructions**

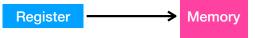
- Main memory used for composite data
  - · arrays, structures, dynamic data
- Register <-> Memory instructions
  - load values from memory into registers
  - store result from register to memory
- Memory is byte addressed
  - each address identifies an 8-bit byte
  - RISC-V is Little Endian
  - RISC-V and x86 do not require words to be aligned in memory
    - alignment restriction forces words to start at addresses that are multiples of the word size

# Fetching and storing data

- Values can be fetched from memory
  - using a load instruction



- Values can be stored in memory
  - using a **store** instruction



## **Load instructions**

Load word from memory

destination register

source address

 $lw \times 9$ ,  $32(\times 22)$ 

- · destination can be any register
- source address uses a constant (offset) added to the register value (base)

## Store instruction

Store word into memory

source register

destination address

x9.48(x22)

- · source can be any register
- destination address uses a constant (offset) added to the register value (base)

# **Example with memory operand**

C code

$$g = h + A[8];$$

- Compiled RISC-V code
  - index 8 requires offset of 32 (4 bytes)

```
assume g in x21, h in x22
# assume base address of A in x23
   x21, 32(x23)
lw
      x21, x21, x22
add
```

# **Example with memory operand**

C code

$$A[7] = h + A[5];$$

- Compiled RISC-V code
  - try yourself (assume h in x21 and base address of A in x22)

x9, 20(x22)lw x9, x21, x9 add x9, 28(x22)SW

# **Registers vs memory**

- Operating on memory data requires loads and stores
  - consider memory latency and additional instructions to be executed
- Registers are a fast read/write memory right on the CPU that can hold values
- Compiler must use registers for variables as much as possible
  - only spill to memory for less frequently used variables
  - register optimization is important!