



UNIVERSITY OF RIZAL SYSTEM

Computer Architecture and Organization

Nurturing Tomorrow's Noblest



UNIVERSITY OF RIZAL SYSTEM

Memory System Organization and Architectures

Nurturing Tomorrow's Noblest



UNIVERSITY OF RIZAL SYSTEM

Internal Memory

Nurturing Tomorrow's Noblest



URS

Semiconductor Main Memory

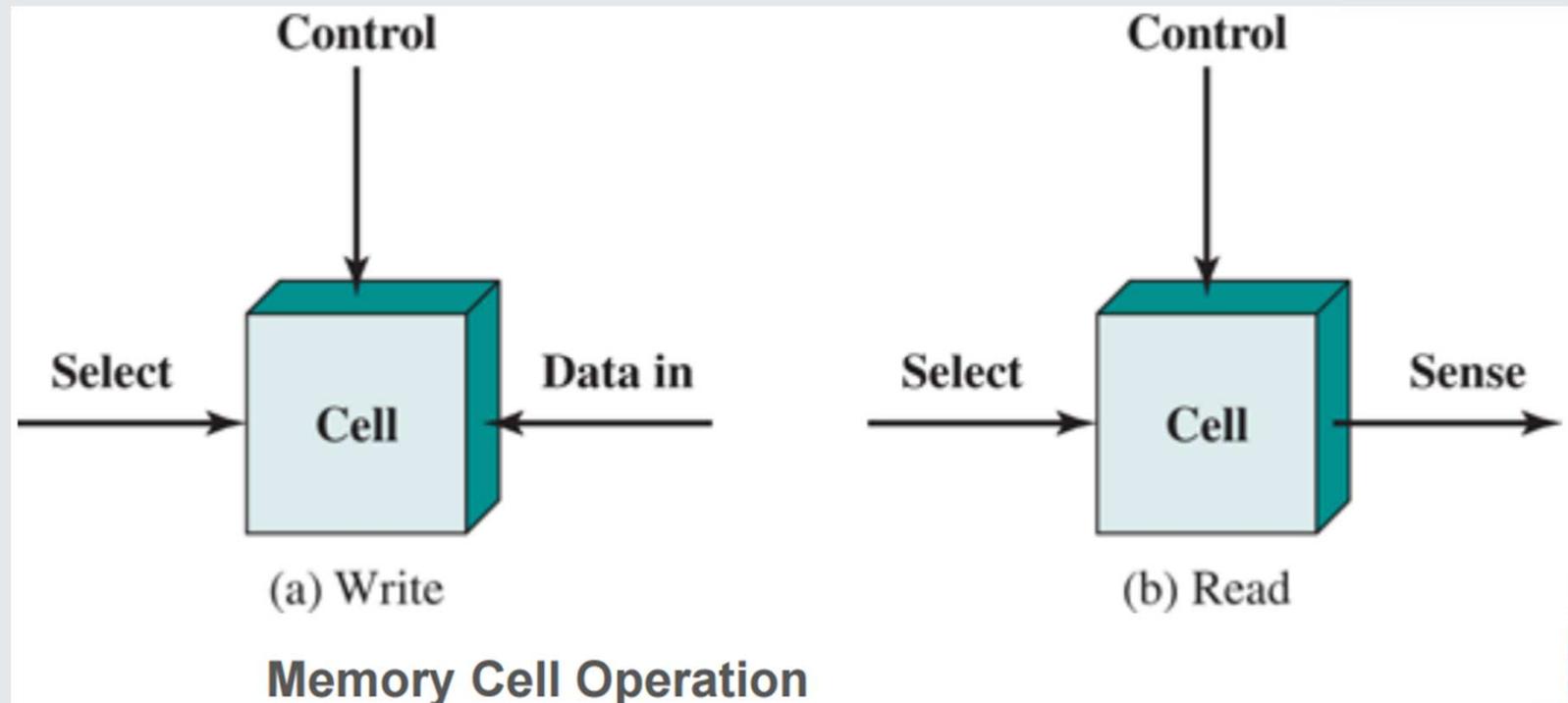
In earlier computers, the **most common form of random-access storage for computer main memory** employed an **array of doughnut-shaped ferromagnetic loops** referred to as **cores**. Hence, **main memory** was often referred to as **core**, a term that persists to this day. The advent of, and advantages of, **microelectronics** has long since **vanquished the magnetic core memory**. Today, the use of **semiconductor chips** for **main memory** is almost universal.

Organization

The **basic element of a semiconductor memory** is the **memory cell**. Although a variety of electronic technologies are used, all semiconductor memory cells share certain **properties**:

- They exhibit **two stable** (or **semistable**) states, which can be used to represent **binary 1** and **0**.
- They are capable of being **written** into (at least once), to **set the state**.
- They are capable of being **read** to **sense the state**.

Most commonly, the **cell** has **three functional terminals** capable of carrying an electrical signal. The **select terminal**, as the name suggests, **selects** a memory cell for a **read or write operation**. The **control terminal** indicates **read or write**. For **writing**, the other terminal provides an electrical signal that sets the state of the cell to 1 or 0. For **reading**, that terminal is used for output of the cell's state.





URS

DRAM and SRAM

Random access is individual words of memory are directly accessed through wired-in addressing logic.

Semiconductor Memory Types				
Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)		UV light, chip-level		
Electrically Erasable PROM (EEPROM)	Read-mostly memory	Electrically, byte-level		
Flash memory		Electrically, block-level		



URS

The most common is referred to as **random-access memory (RAM)**. This is, in fact, a misuse of the term, because all of the types listed in the table are **random access**. **One distinguishing characteristic of memory** that is designated as RAM is that it is possible **both** to **read data from** the **memory** and **to write new data into** the **memory** easily and rapidly. **Both** the **reading** and **writing** are accomplished through the **use** of **electrical signals**.

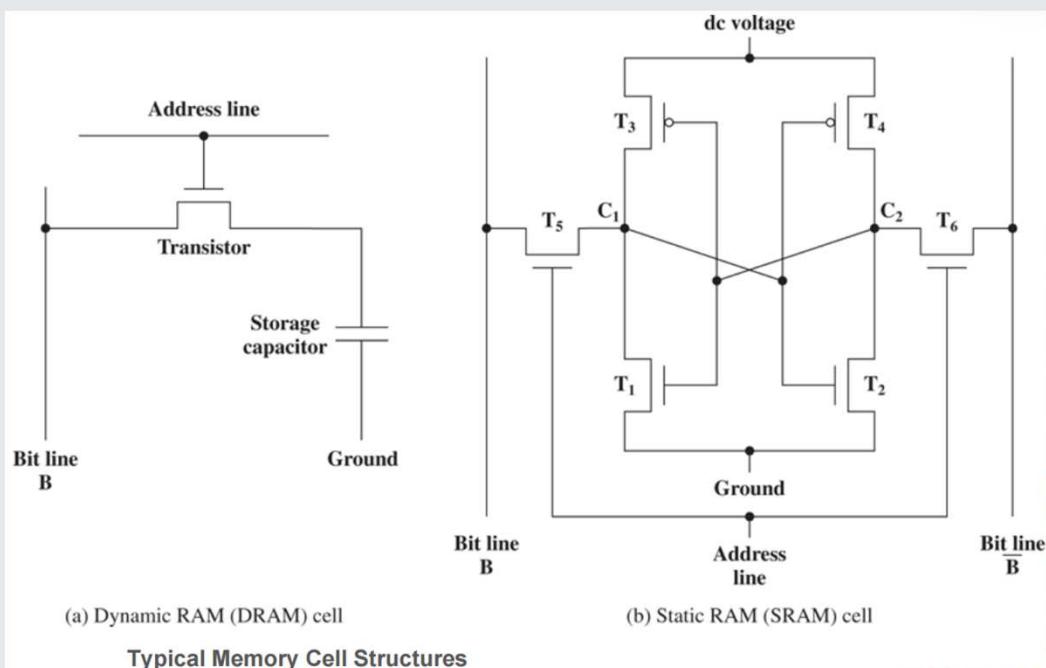
The **other distinguishing characteristic of traditional RAM** is that it is **volatile**. A RAM must be provided with a **constant power supply**. If the **power** is interrupted, then the **data** are **lost**. RAM can be used only as **temporary storage**. The **two traditional forms** of **RAM** used in computers are **DRAM** and **SRAM**. Newer forms of **RAM** are **nonvolatile**.

Dynamic RAM (DRAM)

RAM technology is divided into two technologies: dynamic and static. A **dynamic RAM (DRAM)** is made with cells that store data as charge on capacitors.

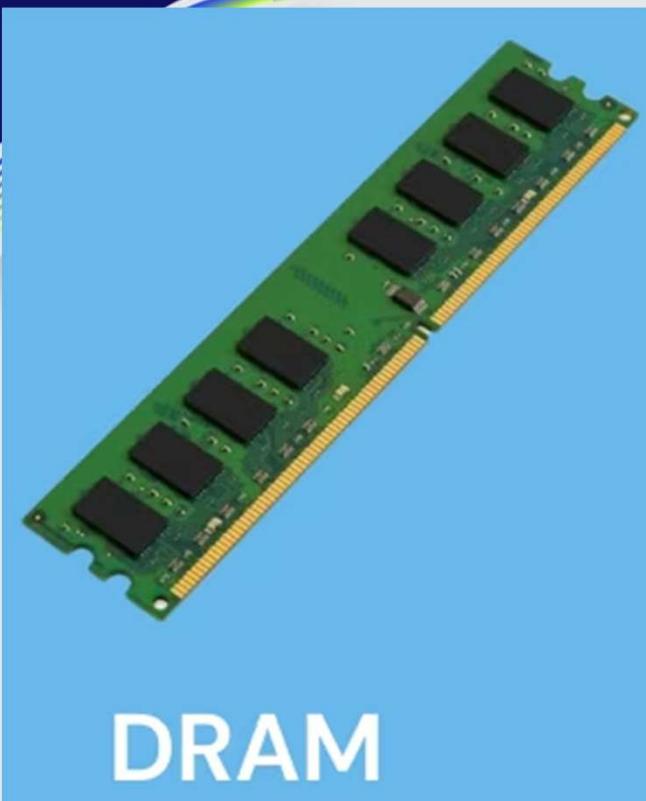
The presence or absence of charge in a capacitor is interpreted as a binary 1 or 0. Because capacitors have a natural tendency to discharge, dynamic RAMs require periodic charge refreshing to maintain data storage. The term **dynamic** refers to this tendency of the stored charge to leak away, even with power continuously applied.

Figure (a) is a typical DRAM structure for an individual cell that stores one bit. The address line is activated when the bit value from this cell is to be read or written. The transistor acts as a switch that is closed (allowing current to flow) if a voltage is applied to the address line and open (no current flows) if no voltage is present on the address line.

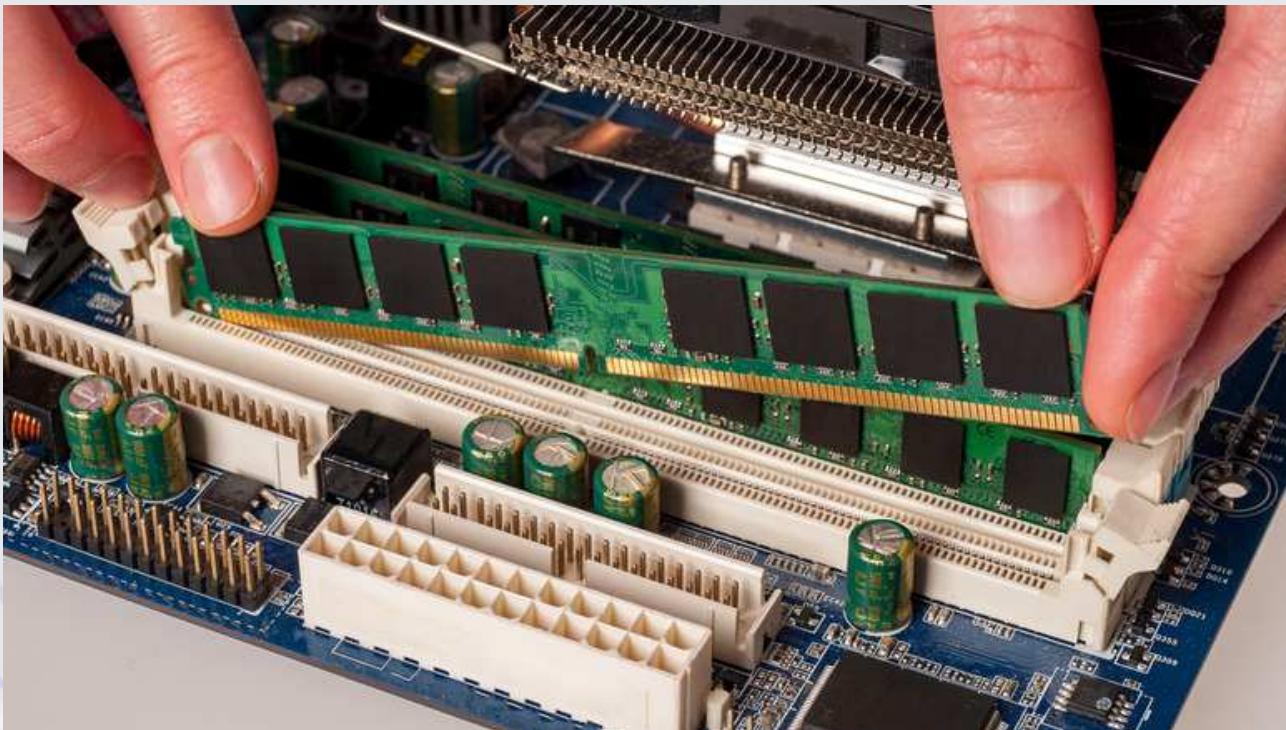
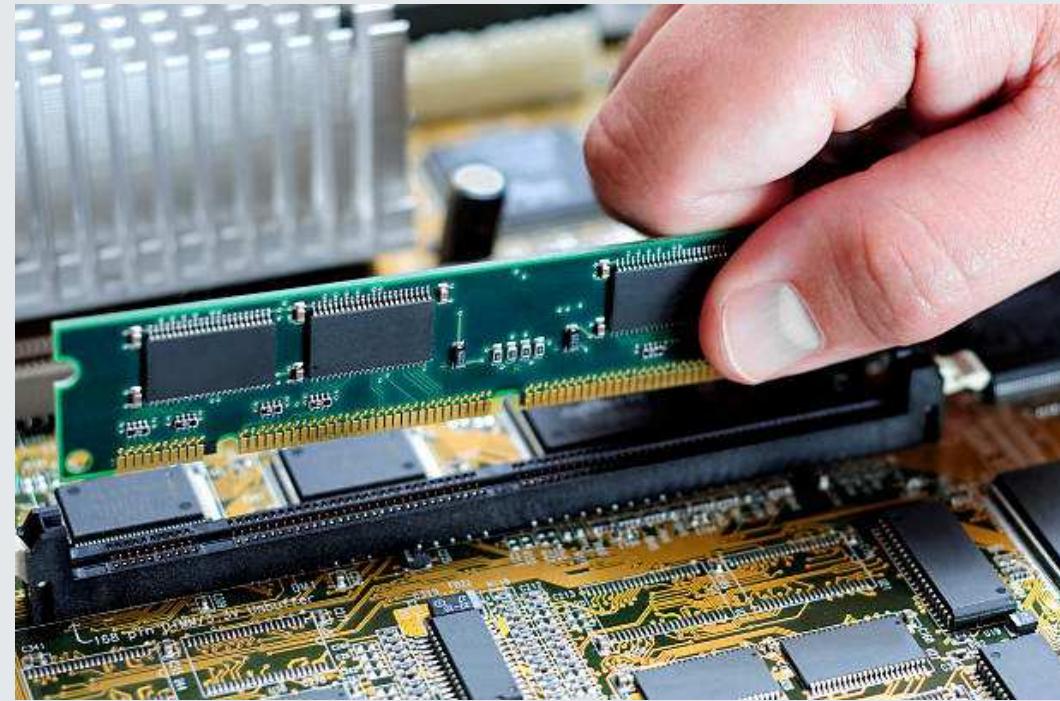




URS

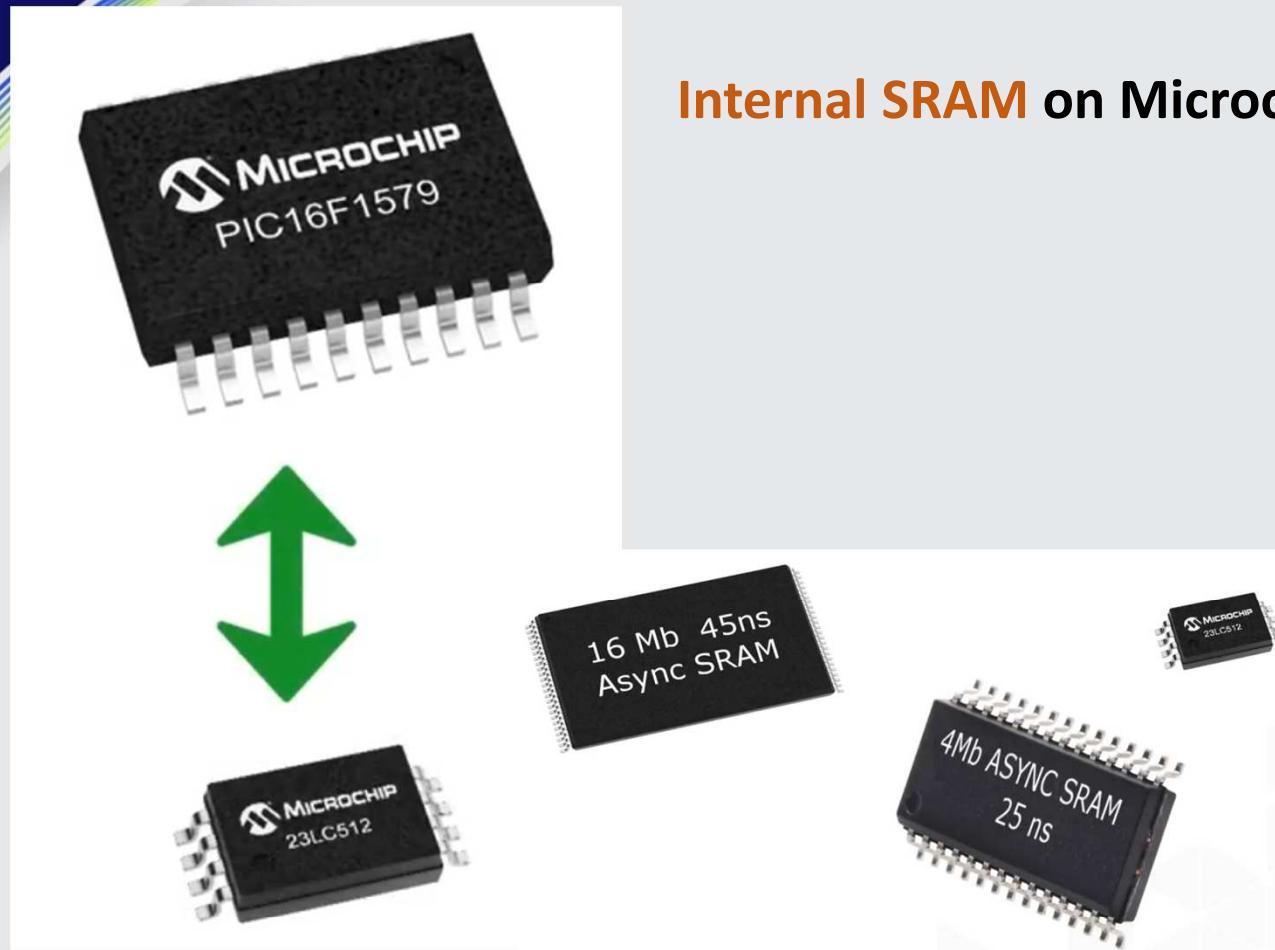


DRAM



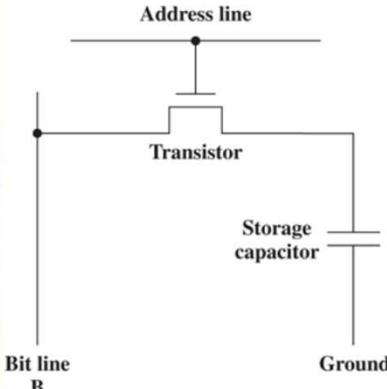
Nurturing Tomorrow's Noblest

Internal SRAM on Microcontroller

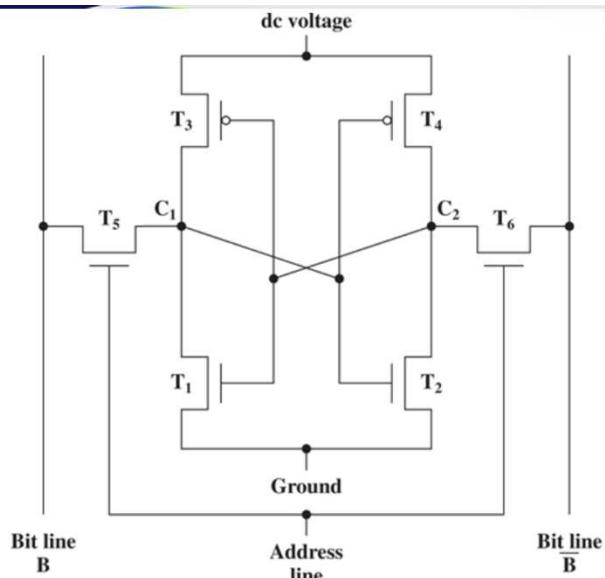


SRAM Standalone (External SRAM)

The **Microchip PIC16F1579** is an 8-bit microcontroller from the PIC16F family produced by Microchip Technology. It is part of the PIC® microcontroller lineup, which is known for offering a wide range of peripherals and ease of use, particularly for small embedded applications.



(a) Dynamic RAM (DRAM) cell



(b) Static RAM (SRAM) cell

Typical Memory Cell Structures

For the **read operation**, when the address line is selected, the **transistor turns on** and the **charge stored** on the **capacitor** is **fed out onto** a **bit line** and to a **sense amplifier**. The **sense amplifier compares** the **capacitor voltage** to a **reference value** and **determines** if the **cell contains** a **logic 1** or a **logic 0**. The readout from the cell **discharges** the **capacitor**, which must be **restored** to complete the **operation**.

Although the **DRAM cell** is used to **store a single bit (0 or 1)**, it is essentially an **analog device**. The capacitor can store any charge value within a range; a **threshold value** **determines** whether the **charge** is interpreted as **1** or **0**.

For the **write operation**, a **voltage signal** is **applied** to the **bit line**; a **high voltage** represents **1**, and a **low voltage** represents **0**. A **signal** is then **applied** to the **address line**, allowing a **charge** to be transferred to the **capacitor**.

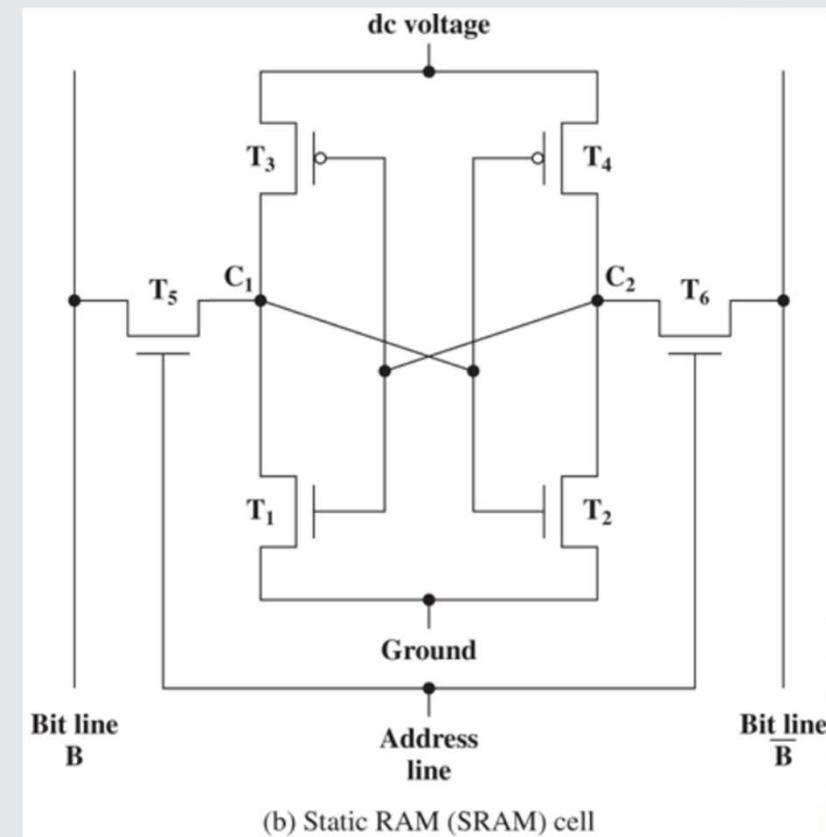
Static RAM (SRAM)

A **static RAM (SRAM)** is a **digital device** that uses the same logic elements used in the processor. In a SRAM, **binary values are stored** using **traditional flip-flop logic-gate configurations**. A **static RAM** will **hold its data as long as power is supplied** to it.

Figure (b) is a typical SRAM structure for an individual cell. **Four transistors (T1, T2, T3, T4)** are cross connected in an arrangement that produces a **stable logic state**. In **logic state 1**, point **C1** is **high** and point **C2** is **low**; in this state, **T1** and **T4** are **off** and **T2** and **T3** are **on**.

In **logic state 0**, point **C1** is **low** and point **C2** is **high**; in this state, **T1** and **T4** are **on** and **T2** and **T3** are **off**.

Both states are stable as long as the **direct current (dc) voltage is applied**. Unlike the **DRAM**, **no refresh** is **needed to retain data**.





URS

As in the DRAM, the SRAM **address line** is used to **open** or **close** a **switch**. The **address line** **controls** two transistors (**T5** and **T6**). When a **signal** is applied to this **line**, the **two** transistors are switched **on**, allowing a **read** or **write** operation. For a **write operation**, the **desired bit value** is **applied** to **line B**, while its **complement** is **applied** to **line A**. This forces the **four** transistors (**T1, T2, T3, T4**) into the proper state. For a **read operation**, the **bit value** is **read** from **line B**.

SRAM Versus DRAM

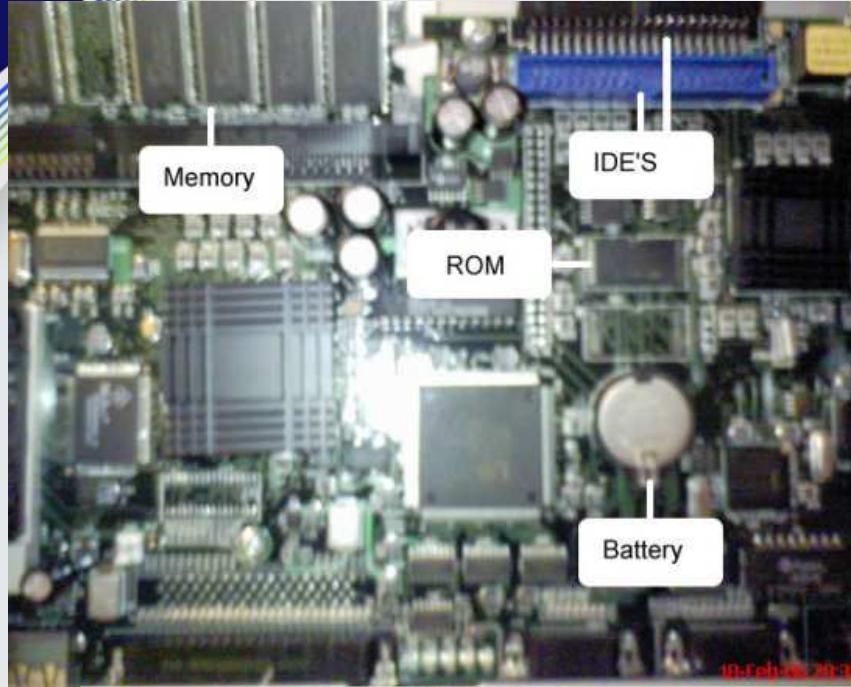
Both **static** and **dynamic RAMs** are **volatile**; **power** must be **continuously supplied** to the **memory** to **preserve** the **bit values**. A **dynamic memory cell** (**DRAM**) is **simpler** and **smaller** than a **static memory cell** (**SRAM**). A **DRAM** is **more dense** (smaller cells = more cells per unit area) and **less expensive** than a corresponding **SRAM**.

On the other hand, a **DRAM** **requires** the supporting **refresh circuitry**. For **larger memories**, the **fixed cost** of the **refresh circuitry** is **more than compensated** for by the **smaller variable cost** of **DRAM cells**. Thus, **DRAMs** tend to be **favored** for **large memory requirements**. A final point is that **SRAMs** are **faster** than **DRAMs**. Because of these relative characteristics, **SRAM** is **used** for **cache memory** (both on and off chip), and **DRAM** is **used** for **main memory**.



URS

ROM





URS

Types of ROM

A **read-only memory (ROM)** contains a **permanent pattern** of data that **cannot** be **changed**. A ROM is **nonvolatile**; **no power source** is **required** to maintain the **bit values** in **memory**. While it is possible to **read** a ROM, it is **not** possible to **write** new data into it. An important **application** of ROMs is **microprogramming**. Other potential **applications** include:

- Library subroutines for frequently wanted functions
- System programs
- Function tables

For a **modest-sized requirement**, the **advantage** of ROM is that the data or program is **permanently** in **main memory** and **need never be loaded** from a secondary storage device.

A ROM is created like any other **integrated circuit chip**, with the **data** actually wired into the **chip** as **part** of the **fabrication process**. This presents **two problems**:

- The **data insertion step** includes a **relatively large fixed cost**, whether one or thousands of copies of a particular ROM are fabricated.
- There is **no room for error**. If **one bit** is **wrong**, the **whole batch** of ROMs must be **thrown out**.



URS

When only a **small number** of ROMs with a particular memory content is needed, a **less expensive alternative** is the **programmable ROM (PROM)**. Like the ROM, the **PROM** is **nonvolatile** and may be **written** into **only once**. For the PROM, the **writing process** is performed **electrically** and may be **performed** by a **supplier** or **customer** at a time **later than** the original chip fabrication. **Special equipment** is required for the **writing** or “**programming**” **process**. PROMs provide **flexibility** and **convenience**. The **ROM** remains attractive for **high-volume** production runs.

Another **variation on read-only memory** is the **read-mostly memory**, which is **useful** for applications in which **read operations** are **far more frequent than write operations** but for which **nonvolatile** storage is **required**.



URS

Three common forms of read-mostly memory: EPROM, EEPROM, and flash memory.

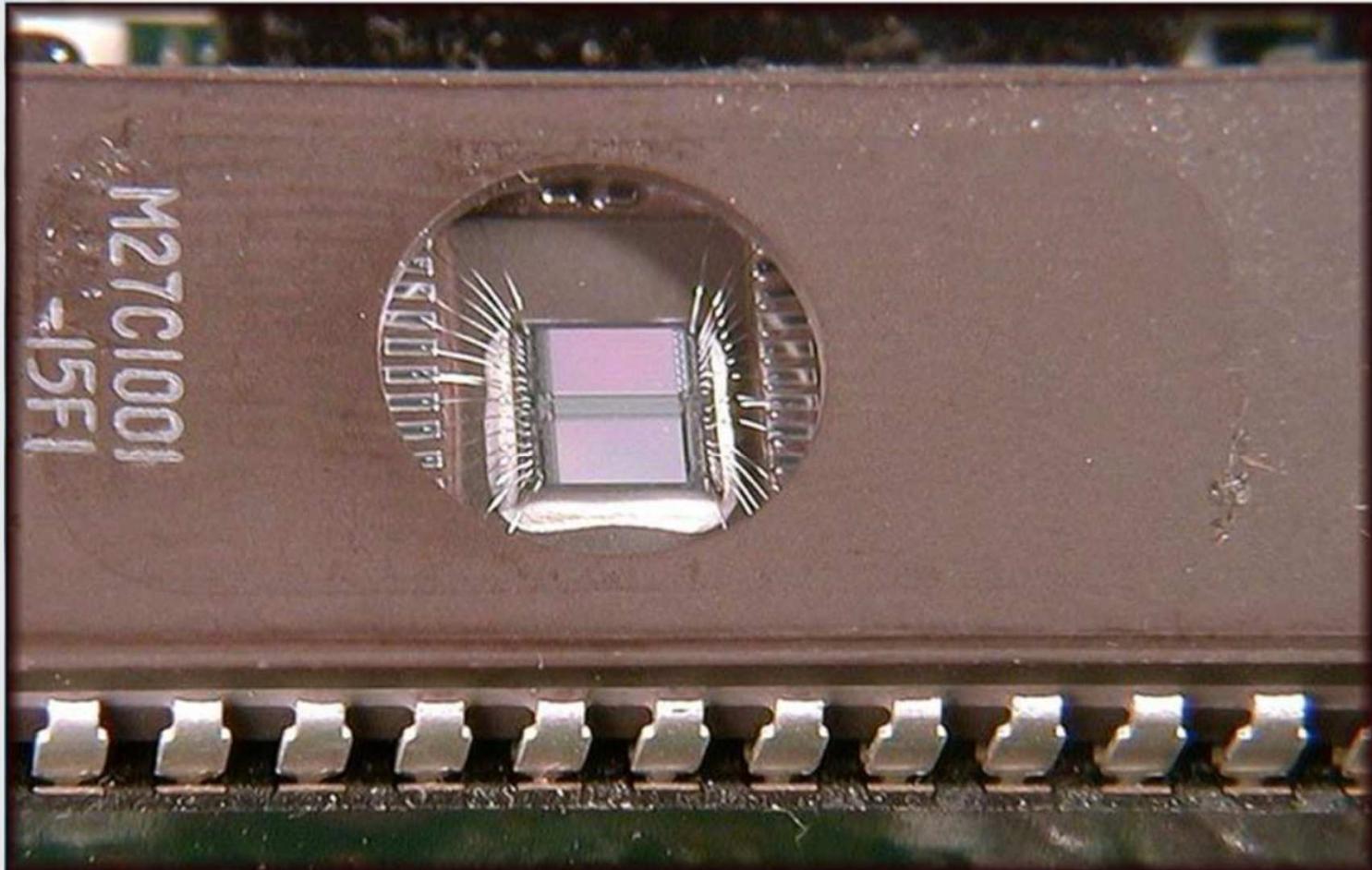
The **optically erasable programmable read-only memory (EPROM)** is read and **written electrically**, as with PROM. **Before** a write operation, **all** the **storage cells** must be **erased** to the same initial state by **exposure** of the packaged chip to ultraviolet radiation.

Erasure is performed by shining an **intense ultraviolet light** through a **window** that is designed into the **memory chip**. This **erasure process** can be performed **repeatedly**; each **erasure** can take as much as **20 minutes to perform**. Thus, the **EPROM** can be **altered multiple times** and, like the ROM and PROM, **holds** its **data virtually indefinitely**. For **comparable amounts of storage**, the **EPROM** is **more expensive than PROM**, but it has the **advantage** of the **multiple update capability**.



URS

Erasable PROM... EPROM





URS

A more attractive form of read-mostly memory is electrically erasable programmable read-only memory (EEPROM). This is a read-mostly memory that can be written into at any time without erasing prior contents; only the byte or bytes addressed are updated.

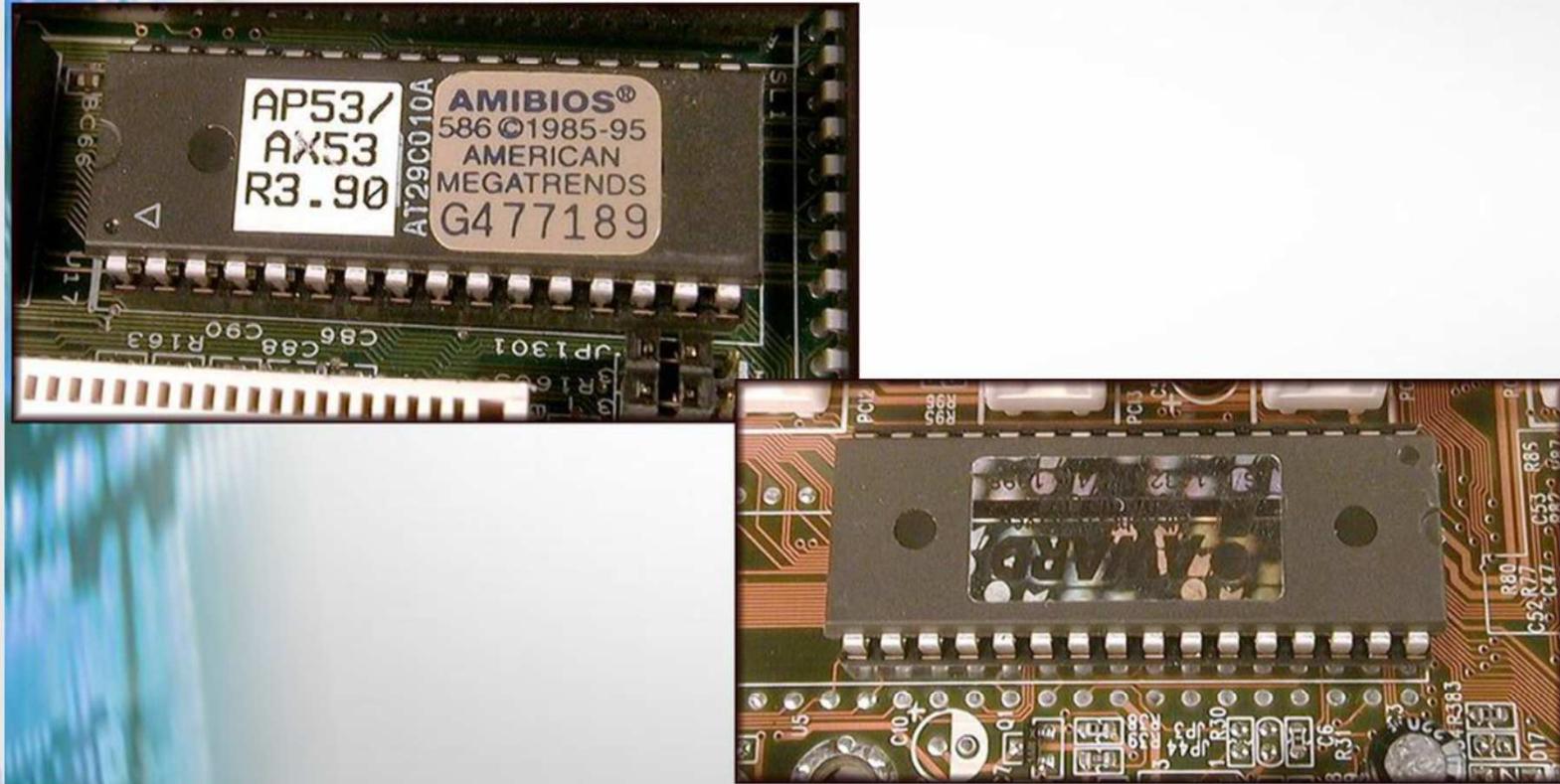
The write operation takes considerably longer than the read operation, on the order of several hundred microseconds per byte. The EEPROM combines the advantage of nonvolatility with the flexibility of being updatable in place, using ordinary bus control, address, and data lines. EEPROM is more expensive than EPROM and also is less dense, supporting fewer bits per chip.

Another form of semiconductor memory is flash memory (so named because of the speed with which it can be reprogrammed). First introduced in the mid-1980s, flash memory is intermediate between EPROM and EEPROM in both cost and functionality. Like EEPROM, flash memory uses an electrical erasing technology. An entire flash memory can be erased in one or a few seconds, which is much faster than EPROM. In addition, it is possible to erase just blocks of memory rather than an entire chip. Flash memory gets its name because the microchip is organized so that a section of memory cells are erased in a single action or “flash.” However, flash memory does not provide byte-level erasure. Like EPROM, flash memory uses only one transistor per bit, and so achieves the high density (compared with EEPROM) of EPROM.



URS

Electrically-Erasable PROM... EEPROM



Nurturing Tomorrow's Noblest

Chip Packaging

Figure (a) shows an example EPROM package, which is an 8-Mbit chip organized as **1Mx8**. In this case, the organization is treated as a **one-word-per-chip package**. The package includes **32 pins**, which is **one of the standard chip package sizes**. The pins support the following signal lines:

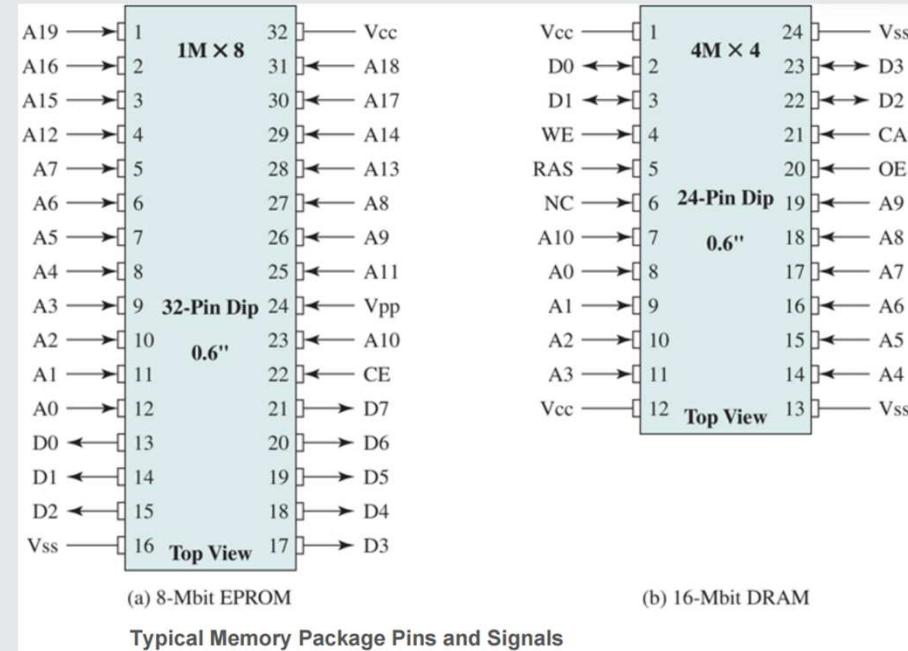
1Mx8 describes the memory organization of the chip:

1M stands for **1 megabit**, which is the number of memory locations or rows in the chip. In this case, it means there are $2^{20} = 1048576$ rows.

8 represents the **number of bits per memory location** (column or data width).

1Mx8 means the chip has **1 megabit of memory**, with each memory location containing **8 bits** (1 byte). To get the **total storage capacity** of the chip, you multiply **1Mx8=8 megabits (Mb)**, which **equals 1 megabyte (MB)**.

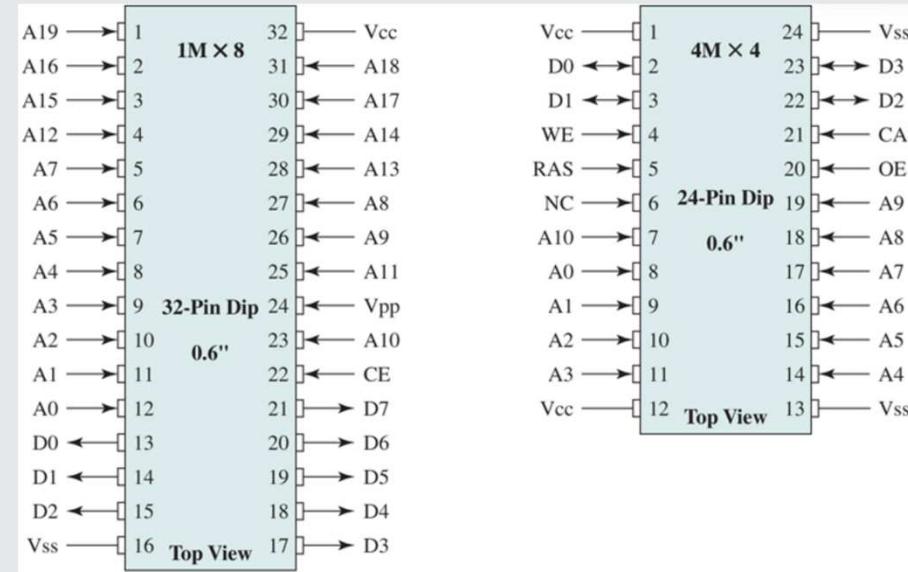
1Mx8: 1 megabit per row (1,048,576 rows), and each row contains 8 bits (1 byte).



Chip Packaging

Figure (a) shows an example EPROM package, which is an 8-Mbit chip organized as **1M \times 8**. In this case, the organization is treated as a **one-word-per-chip package**. The package includes **32 pins**, which is **one of the standard chip package sizes**. The pins support the following signal lines:

- The **address** of the word being accessed. For **1M words**, a total of **$20(2^{20} = 1M)$** pins are needed (**A0–A19**).
- The **data to be read out**, consisting of **8 lines** (**D0–D7**).
- The **power supply** to the chip (**V_{cc}**)
- A **ground pin** (**V_{ss}**)
- A **chip enable (CE) pin**. Because there may be more than one memory chip, each of which is connected to the same address bus, the **CE pin** is **used to indicate whether or not the address is valid** for this chip. The **CE pin** is **activated by logic connected to the higher-order bits of the address bus (i.e., address bits above A19)**.
- A **program voltage (V_{pp})** that is supplied during programming (write operations).



(a) 8-Mbit EPROM

Typical Memory Package Pins and Signals

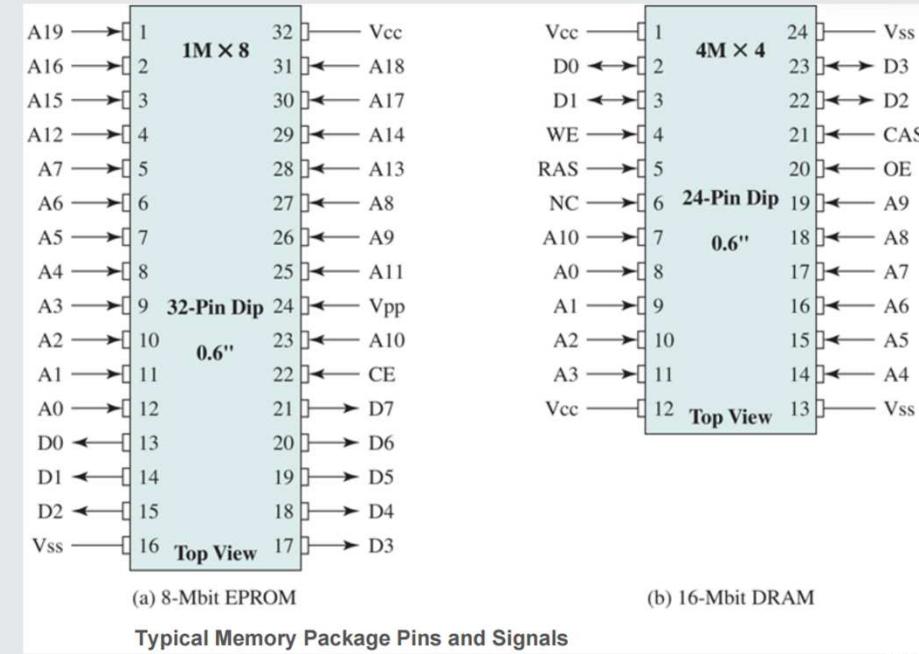
(b) 16-Mbit DRAM

A typical DRAM pin configuration is shown in **Figure (b)**, for a 16-Mbit chip organized as **4MX4**.

4M stands for **4 megabits**, which is the number of memory locations (rows or words) in the chip. In this case, it means there are $2^{22} = 4,194,304$ rows.

4 represents the **number** of bits per memory location (column or data width).

a **4M×4** organization means that the chip has **4 megabits of memory** organized in **4-bit wide data words**. To get the **total storage capacity** of the chip, multiply **$4M \times 4 = 16$ megabits (Mb)**, which **equals 2 megabytes (MB)**.

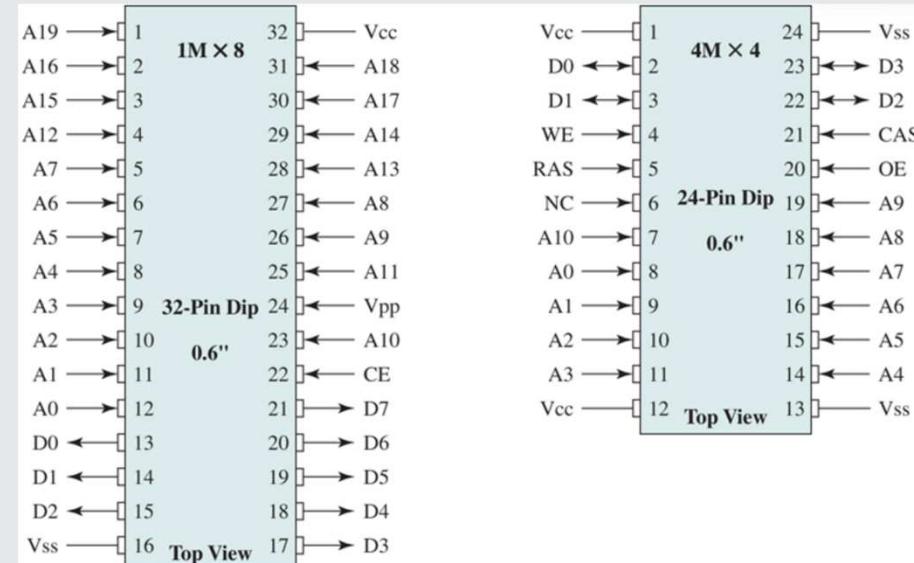


There are several **differences** from a ROM chip. Because a RAM can be **updated**, the **data pins** are **input/output**. The **write enable (WE)** and **output enable (OE)** pins indicate whether this is a **write** or **read** operation.

Because the DRAM is **accessed** by **row** and **column**, and the **address** is multiplexed, only **11 address** pins are needed to specify the 4M row/column combinations ($2^{11} \times 2^{11} = 4M$).

Row address select (RAS) and column address select (CAS) pins.

No connect (NC) pin is provided so that there are an **even number** of pins.



(a) 8-Mbit EPROM

(b) 16-Mbit DRAM

Typical Memory Package Pins and Signals



URS

Error Correction

A **semiconductor memory system** is subject to **errors**. These can be **categorized** as **hard failures** and **soft errors**. A **hard failure** is a permanent physical defect so that the **memory cell or cells affected** cannot reliably store data but become **stuck** at 0 or 1 or switch erratically between 0 and 1. **Hard errors** can be **caused** by harsh environmental abuse, manufacturing defects, and wear.

A **soft error** is a random, nondestructive event that alters the contents of one or more memory cells **without** damaging the memory. **Soft errors** can be **caused** by power supply problems or alpha particles. These **particles** result from radioactive decay and are distressingly common because radioactive nuclei are found in small quantities in nearly all materials. **Both** hard and soft errors are clearly **undesirable**, and most modern main memory systems include logic for both detecting and correcting errors.

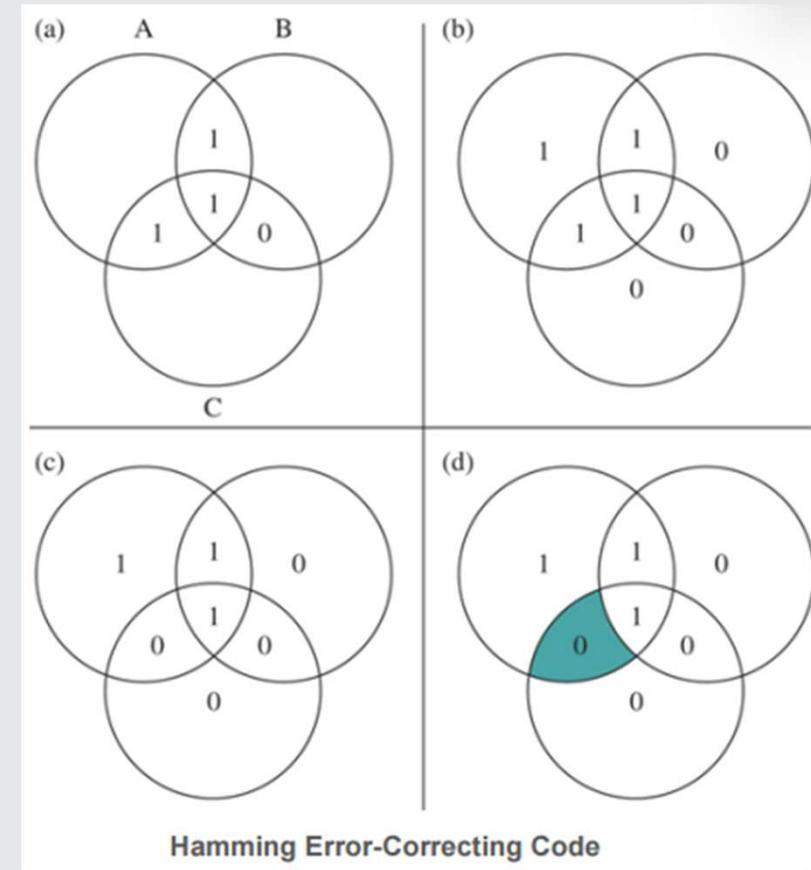
The **simplest** of the **error-correcting codes** is the **Hamming code** devised by **Richard Hamming** at **Bell Laboratories**. Figure uses **Venn diagrams** to illustrate the use of this code on **4-bit words ($M = 4$)**.

With **three intersecting circles**, there are **seven compartments**. Assign the **4 data bits** to the **inner compartments** (**Figure a**). The **remaining compartments** are filled with what are called **parity bits**.

Each parity bit is chosen so that the **total number of 1s** in its **circle** is **even** (**Figure b**). **Circle A** includes **three data 1s**, the **parity bit** in that circle is **set to 1**. If an error **changes one** of the **data bits** (**Figure c**), it is **easily found**. By **checking** the **parity bits**, **discrepancies** are found in

circle A and circle C but not in circle B. **Only one** of the **seven compartments** is in A and C but not B (**Figure d**). The **error** can be **corrected** by **changing** that **bit**.

A **parity bit** is a simple error detection mechanism used in computing and digital communications. Its main purpose is to ensure that the data being transmitted or stored is accurate and hasn't been corrupted.





URS

DDR DRAM (Double Data Rate Random Access Memory)

The **basic building block** of main memory remains the **DRAM chip**. The **traditional DRAM chip** is **constrained both** by its **internal architecture** and by its **interface to the processor's memory bus**.

DDR RAM a type of **memory** used in computers that is an **improvement** over **traditional SDR (Single Data Rate) RAM**. It transfers data twice per clock cycle, effectively doubling the data throughput compared to SDR RAM.

Synchronous DRAM (SDRAM)

One of the **most widely used forms** of **DRAM** is the **synchronous DRAM (SDRAM)**. Unlike the **traditional DRAM**, which is **asynchronous**, the **SDRAM** exchanges data with the **processor synchronized** to an **external clock signal** and running at the **full speed** of the **processor/memory bus** **without** **imposing wait states**.



URS

eDRAM

An increasingly widespread technology used in the memory hierarchy is the **embedded DRAM (eDRAM)**. eDRAM is a DRAM integrated on the same chip or MCM of an application-specific integrated circuit (ASIC) or microprocessor. For a number of metrics, eDRAM is **intermediate between** on-chip SRAM and off-chip DRAM:

- For the same surface area, **eDRAM** provides a **larger size memory than SRAM** but **smaller than off-chip DRAM**.
- **eDRAM's cost-per-bit is higher** when compared to equivalent stand-alone **DRAM** chips used as **external memory**, but it has a **lower cost-per-bit than SRAM**.
- **Access time to eDRAM is greater than SRAM** but, because of its proximity and the ability to use wider busses, **eDRAM provides faster access than DRAM**.

An **MCM (Multi-Chip Module)** is an advanced packaging technology in which multiple integrated circuits (ICs), or chips, are placed on a single module or substrate to function as a **single component**. This approach allows for the integration of various types of chips—such as processors, memory (like eDRAM), and other logic circuits—into a compact unit, improving performance, space efficiency, and power consumption.



URS

A variety of technologies are used in fabricating eDRAMs, but fundamentally they use the same designs and architectures as DRAM.

Trends that have led to increasing use of eDRAM:

- For larger systems and high-end applications, the spatial locality curves have become flatter and wider, meaning that the likely area of memory for upcoming references is larger. This makes DRAM-based caches attractive due to their bit density.
- On-chip or on-MCM eDRAM matches the performance of off-chip SRAM, so that greater cache size can be achieved by replacing some on-chip area that would otherwise be dedicated to SRAM with DRAM, avoiding or reducing the need for off-chip SRAM or DRAM.
- eDRAM generally dissipates less power than SRAM.

Flash Memory

Another form of **semiconductor memory** is **flash memory**. **Flash memory** is used both for **internal memory** and **external memory** applications.

First introduced in the mid-1980s, **flash memory** is intermediate between EPROM and EEPROM in **both cost and functionality**. Like EEPROM, **flash memory** uses an **electrical erasing technology**. An **entire flash memory** can be **erased** in **one or a few seconds**, which is **much faster than EPROM**. In addition, it is possible to **erase just blocks of memory**, **rather than an entire chip**. Flash memory gets its **name** because the microchip is organized so that a section of memory cells are **erased in a single action or flash**. Like EEPROM, flash memory **uses only one transistor per bit**, and so achieves the **high density**.



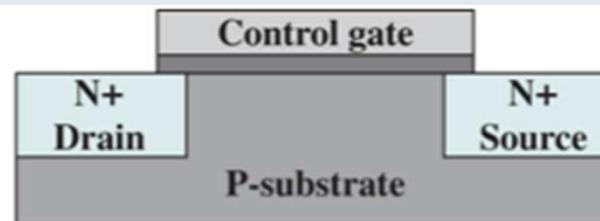
NOR Flash by Intel



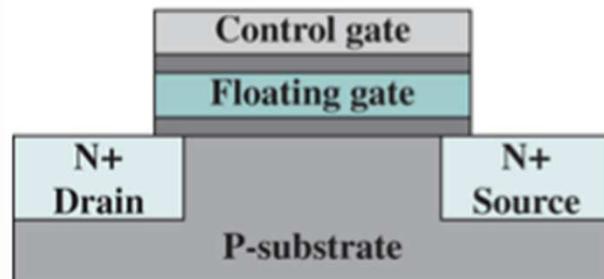
Nor

Operation

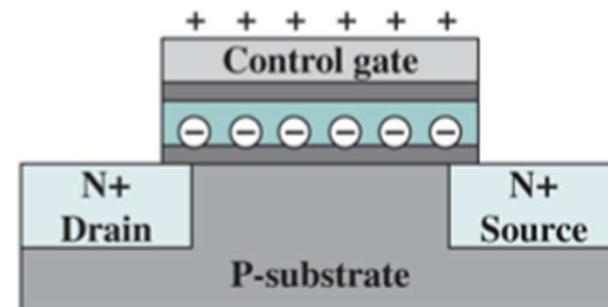
Figure (a) illustrates the **basic operation** of a **flash memory**. For comparison, Figure (a) depicts the **operation** of a **transistor**. Transistors exploit the **properties** of **semiconductors** so that a **small voltage applied** to the **gate** can be **used** to control the **flow** of a **large current between** the **source** and the **drain**.



(a) Transistor structure



(b) Flash memory cell in one state



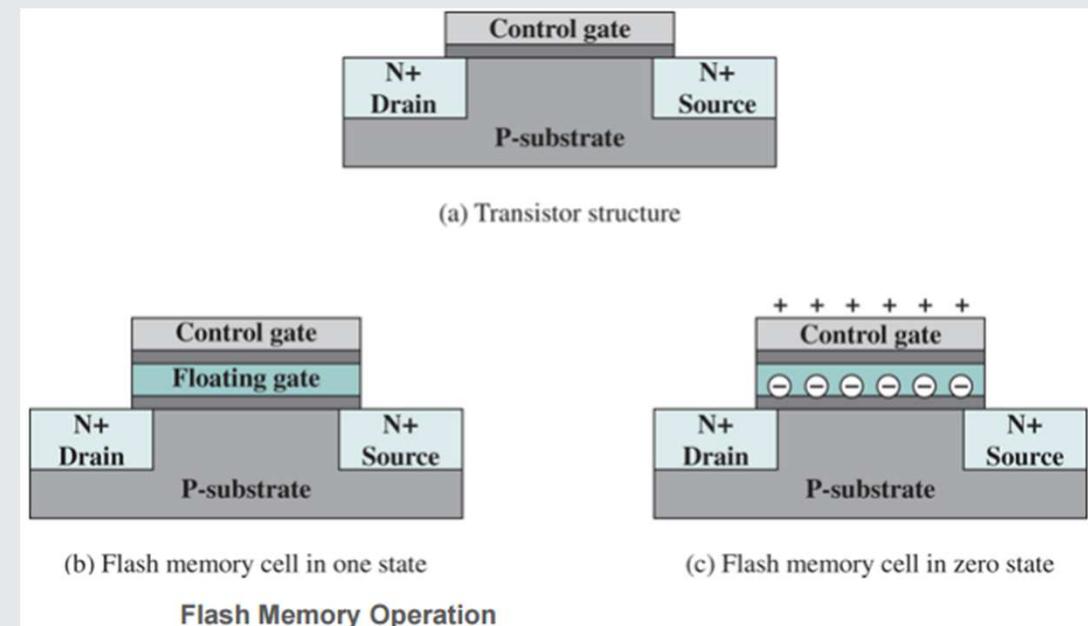
(c) Flash memory cell in zero state

Flash Memory Operation

Operation

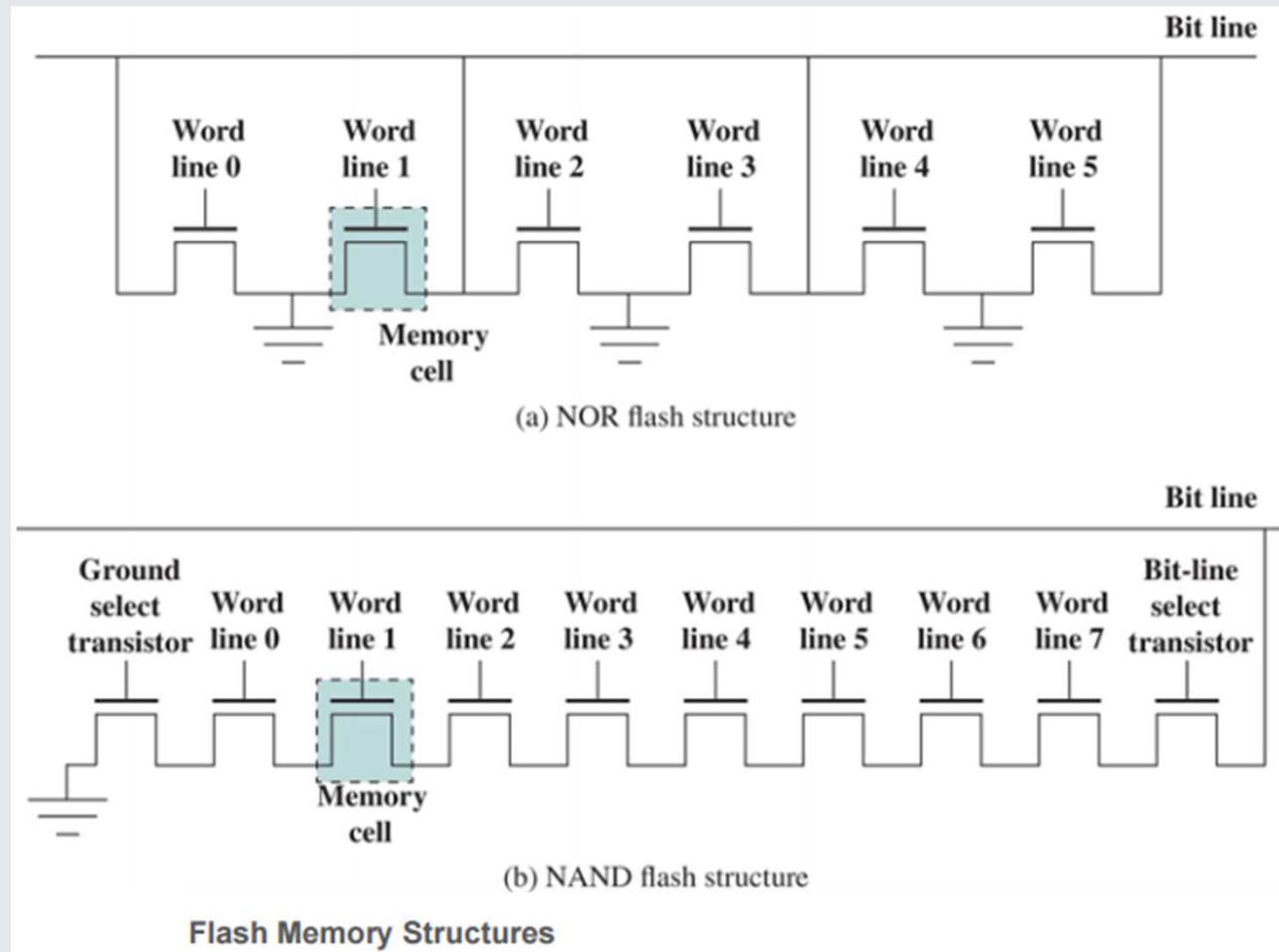
In a **flash memory cell**, a second gate—called a **floating gate**, because it is **insulated** by a **thin oxide layer**—is added to the transistor. **Initially**, the **floating gate** does **not interfere** with the **operation** of the **transistor** (**Figure b**). In this **state**, the **cell** is deemed to represent **binary 1**.

Applying a large voltage across the **oxide layer causes** electrons to tunnel (flow) through it and become **trapped** on the **floating gate**, where they **remain** even if the power is disconnected (**Figure c**). In this **state**, the **cell** is deemed to represent **binary 0**.



The **state** of the **cell** can be **read** by using external circuitry to **test** whether the **transistor** is **working or not**. **Applying** a **large voltage** in the **opposite direction removes** the **electrons** from the **floating gate**, **returning** to a **state of binary 1**.

An important characteristic of **flash memory** is that it is **persistent memory**, which means that it **retains** data when there is **no power applied** to the **memory**. It is **useful** for **secondary (external) storage**, and as an **alternative** to **random access memory (RAM)** in computers.



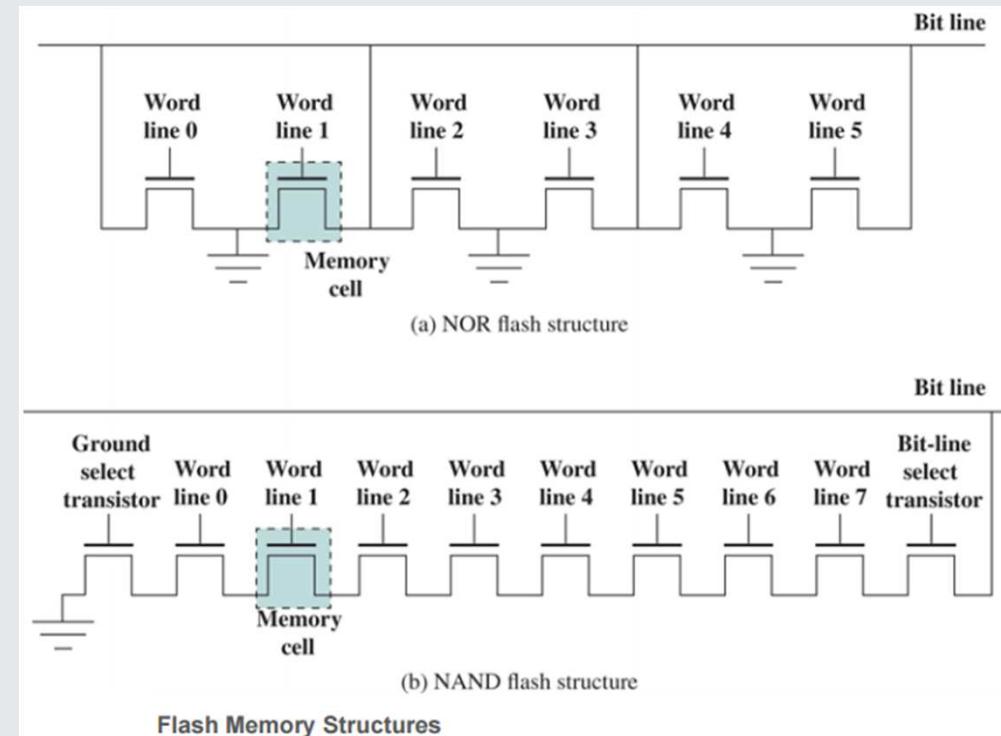
Flash Memory Structures

There are **two distinctive types** of **flash memory**, designated as **NOR** and **NAND** (**Figure**). In **NOR flash memory**, the basic unit of **access** is a **bit**, referred to as a **memory cell**. Cells in **NOR flash** are **connected in parallel** to the bit lines so that each cell can be **read/write/erased individually**. If **any** memory cell

of the device is **turned on** by the corresponding **word line**, the **bit line goes low**. This is **similar in function** to a **NOR logic gate**.

NAND flash memory is **organized in transistor arrays** with **16 or 32 transistors in series**. The **bit line goes low** only if **all the transistors** in the corresponding **word lines** are **turned on**.

This is **similar in function** to a **NAND logic gate**.





URS

NOR flash memory provides high-speed random access. It can read and write data to specific locations, and can reference and retrieve a single byte. **NAND** reads and writes in small blocks. **NAND** provides higher bit density than **NOR** and greater write speed. **NAND flash** does not provide a random-access external address bus, so the data must be read on a blockwise basis (also known as page access), where each block holds hundreds to thousands of bits.

For internal memory in embedded systems, **NOR flash memory** has traditionally been preferred. **NAND memory** has made some inroads, but **NOR** remains the dominant technology for internal memory. It is ideally suited for microcontrollers where the amount of program code is relatively small and a certain amount of application data does not vary. For example, the flash memory in is **NOR** memory.

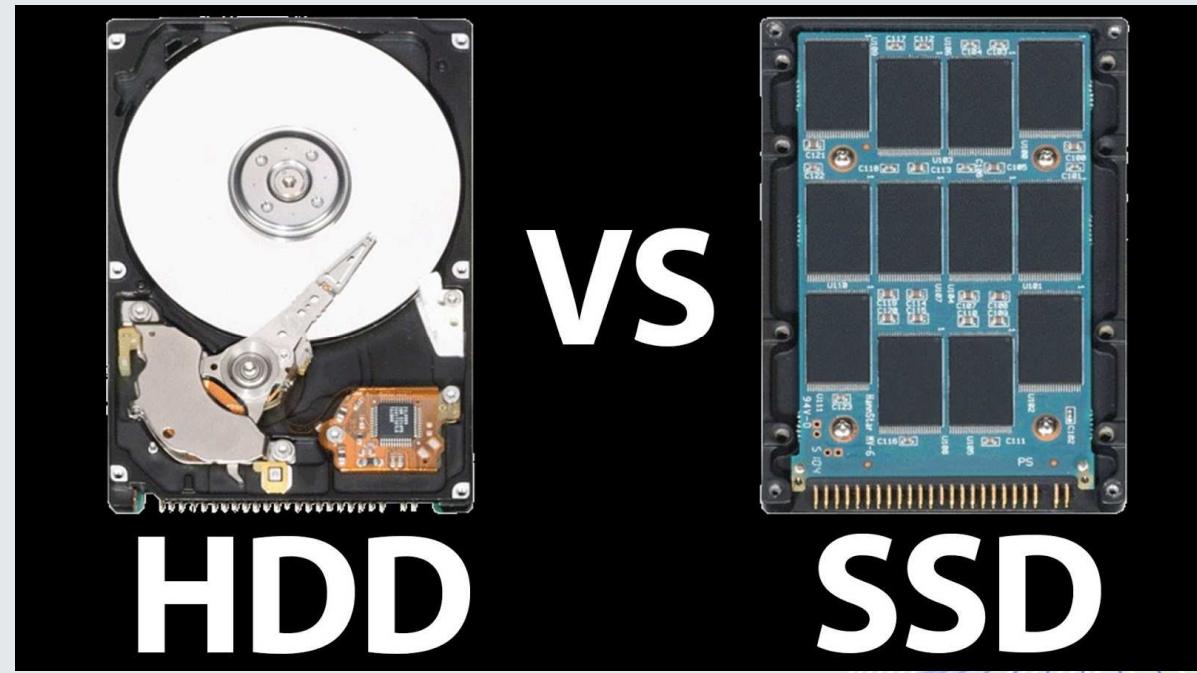
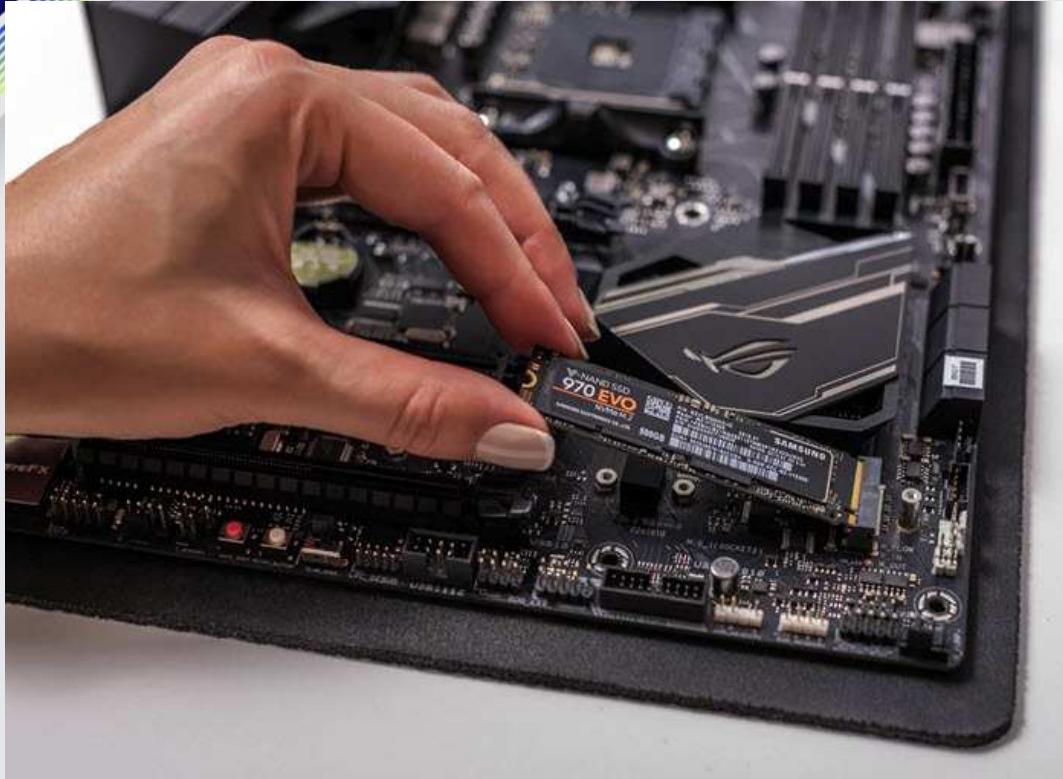
NAND memory is better suited for external memory, such as USB flash drives, memory cards (in digital cameras, MP3 players, etc.), and in what are known as solid-state disks (SSDs).

blockwise basis or **page access** refers to how data is read from or written to the memory. Unlike random access memory (RAM) types, **NAND flash memory** is structured into larger units, and accessing data occurs in groups of bits rather than one bit or byte at a time.



URS

SSD



oblest



URS

Newer Nonvolatile Solid-State Memory Technologies

The traditional memory hierarchy has consisted of **three levels**:

- **Static RAM (SRAM)**: SRAM provides **rapid access time**, but is the **most expensive** and the **least dense** (bit density). SRAM is **suitable** for **cache memory**.
- **Dynamic RAM (DRAM)**: Cheaper, denser, and slower than SRAM, DRAM has traditionally been the **choice** for **off-chip main memory**.
- **Hard disk**: A magnetic disk provides **very high bit density** and **very low cost per bit**, with **relatively slow access times**. It is the traditional choice for **external storage** as part of the memory hierarchy.

Flash memory has the **advantage** over **traditional memory** that it is nonvolatile. NOR flash is best suited to storing programs and static application data in embedded systems, while NAND flash has characteristics intermediate between DRAM and hard disks.

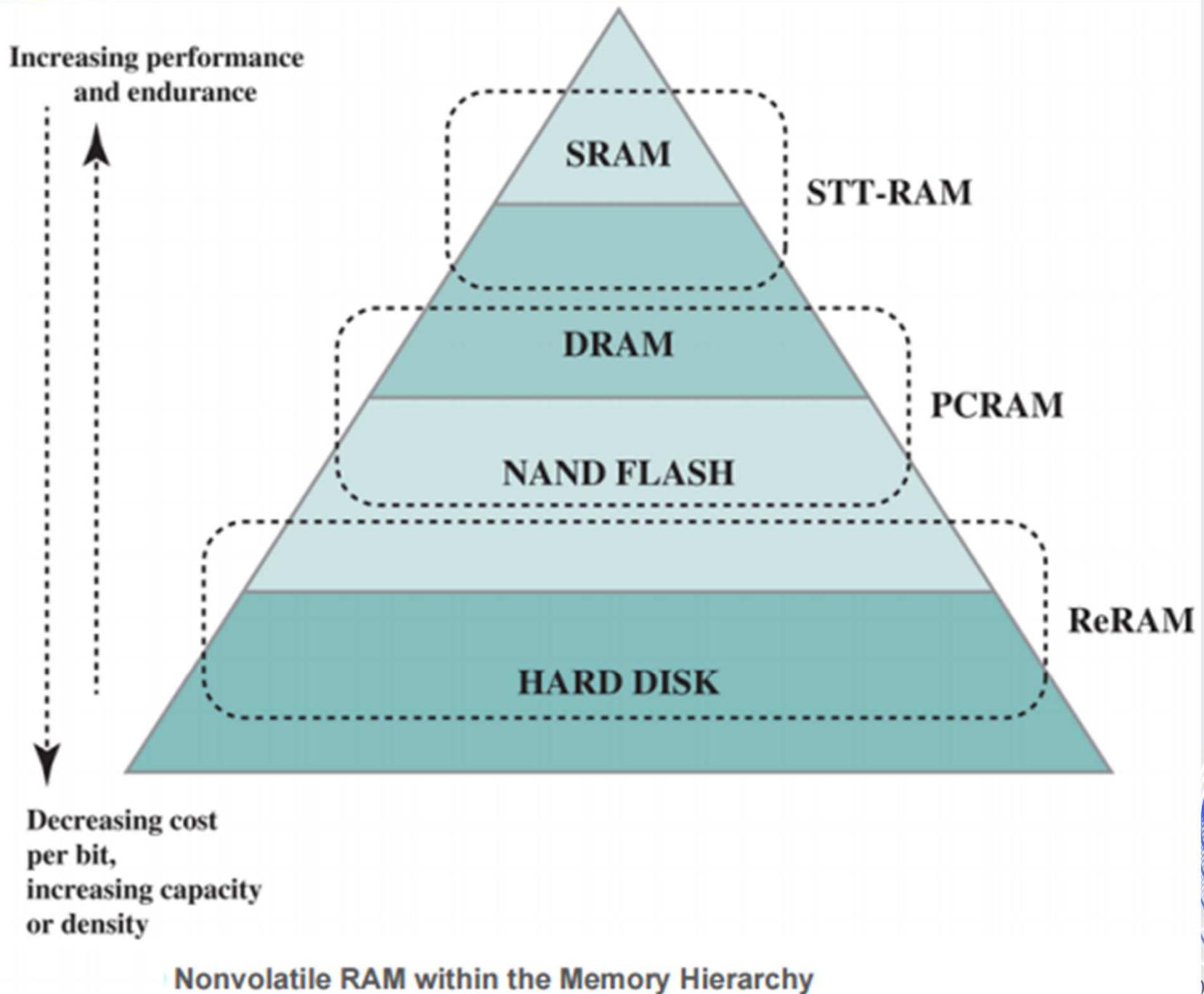


URS

Over time, each of these technologies has seen improvements in scaling: higher bit density, higher speed, lower power consumption, and lower cost. However, for semiconductor memory, it is becoming increasingly difficult to continue the pace of improvement.

Recently, there have been breakthroughs in developing new forms of nonvolatile semiconductor memory that continue scaling beyond flash memory. The most promising technologies are spin-transfer torque RAM (STT-RAM), phase-change RAM (PCRAM), and resistive RAM (ReRAM).

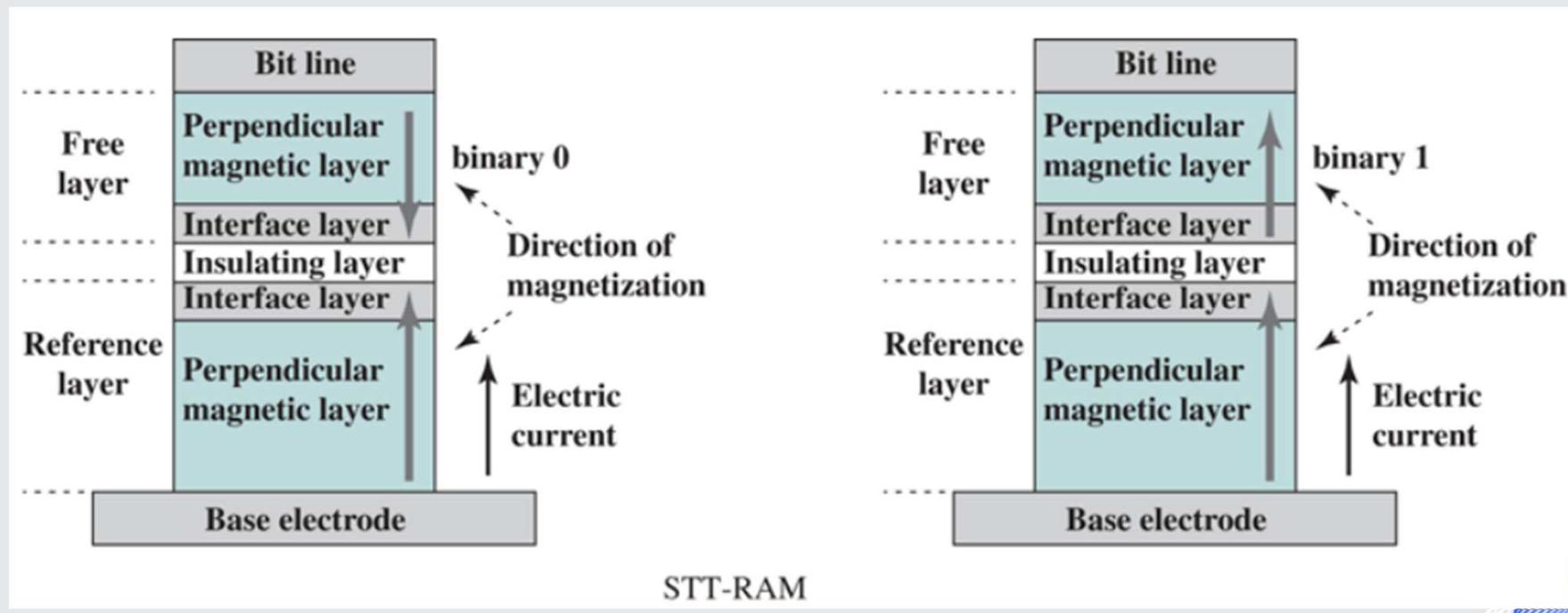
Figure shows how these **three technologies** are likely to fit into the **memory hierarchy**.



STT-RAM

STT-RAM is a **new type** of **magnetic RAM (MRAM)**, which features **non-volatility**, fast writing/reading speed ($< 10ms$), high programming endurance ($> 10^{15}$ cycles) and **zero standby power**.

For STT-RAM is believed to have a **better scaling property** than the first-generation MRAM. STT-RAM is a **good candidate** for either cache or **main memory**.



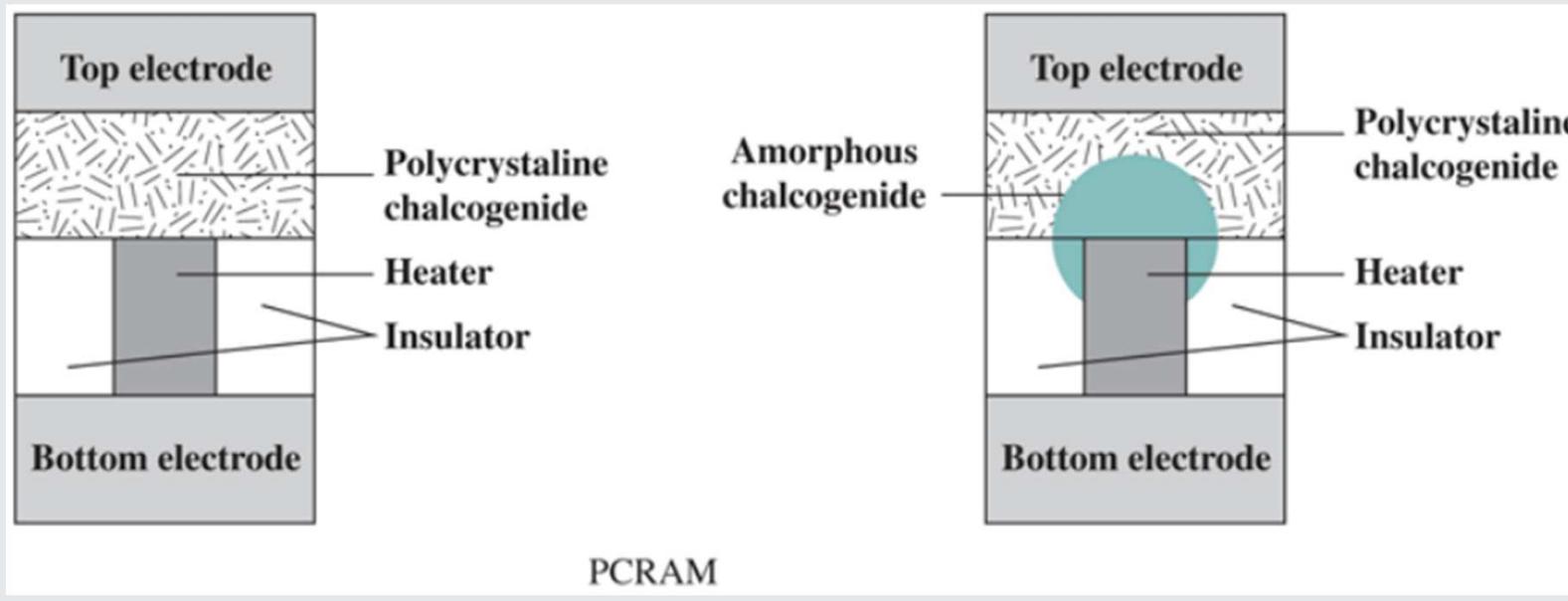
Nonvolatile RAM Technologies

STT-RAM (Spin-Transfer Torque Random Access Memory) is a **type** of magnetic RAM (MRAM) that utilizes the **spin-transfer torque (STT) effect** to store data.

PCRAM

Phase-change RAM (PCRAM) is the most mature of the new technologies.

PCRAM technology is based on a chalcogenide alloy material, which is similar to those commonly used in optical storage media (compact discs and digital versatile discs). PCRAM is a good candidate to replace or supplement DRAM for main memory.



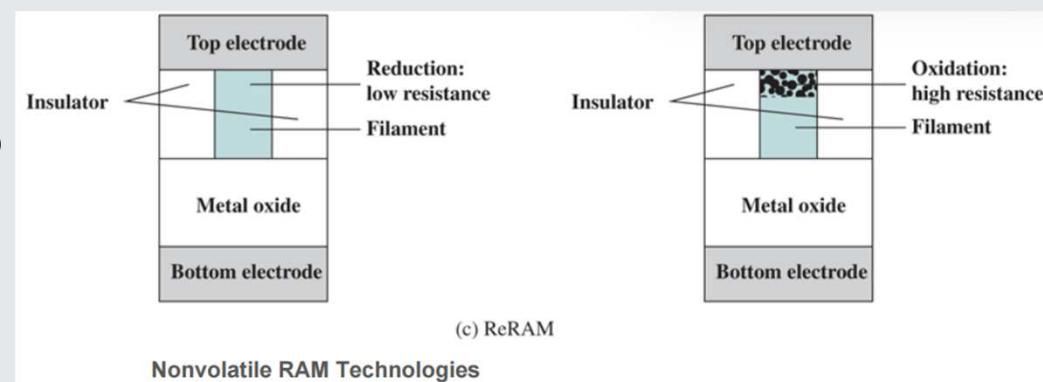
A chalcogenide alloy material is a compound that primarily contains one or more chalcogen elements—such as sulfur (S), selenium (Se), or tellurium (Te)—combined with other elements like germanium (Ge), antimony (Sb), or indium (In). These materials are known for their unique electrical and optical properties, which make them particularly useful in Phase-Change Memory (PCRAM) and optical storage technologies like CDs, DVDs, and Blu-ray discs.

ReRAM

ReRAM (also known as **RRAM**) works by creating resistance rather than directly storing charge. An electric current is applied to a material, changing the resistance of that material.

The **resistance state** can then be measured and a **1** or **0** is **read** as the **result**. Much of the **work done** on **ReRAM** to date has **focused** on **finding appropriate materials** and measuring the resistance state of the cells. **ReRAM designs** are **low voltage**, **endurance** is **far superior** to flash memory, and the **cells** are **much smaller**.

ReRAM is a **good candidate** to **replace** or **supplement** both **secondary storage** and **main memory**.

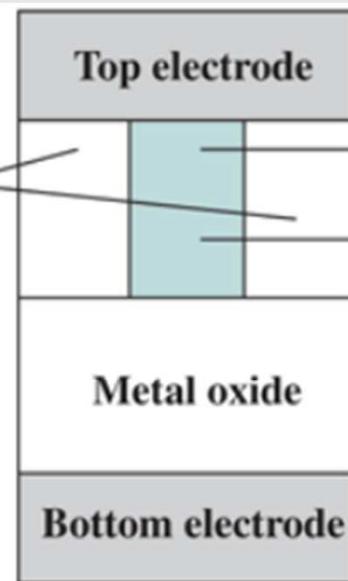


ReRAM (Resistive Random Access Memory), also known as **RRAM**, is a type of **non-volatile memory** that **stores data** by **altering the resistance** of a material rather than **storing electric charge**, as in traditional memory technologies like DRAM or flash. The key **principle** behind ReRAM is its ability to **switch between different resistance states**, which **represent binary data (0s and 1s)**.

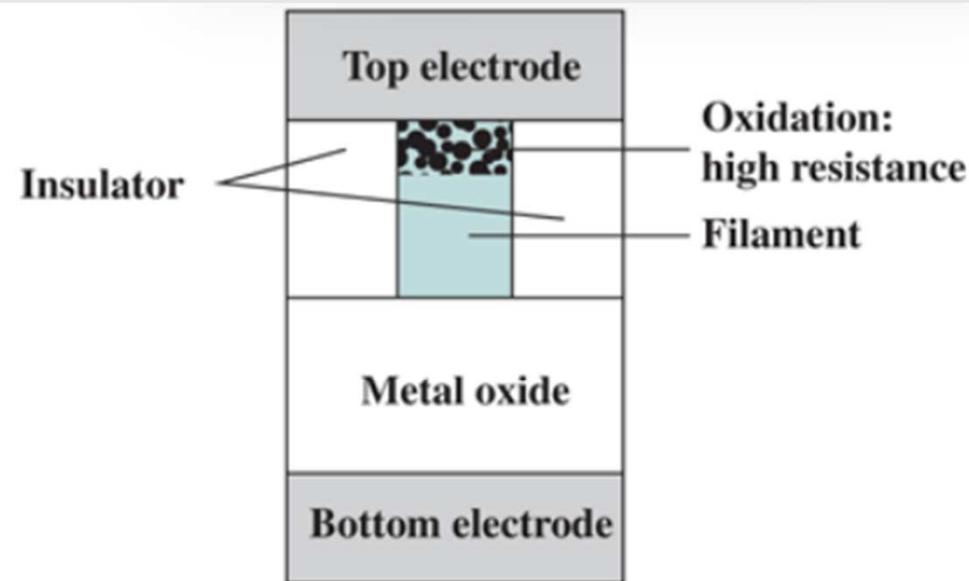
ReRAM

ReRAM (also known as **RRAM**) works by creating resistance rather than directly storing charge. An electric current is applied to a material, changing the resistance of that material.

The **resistance state** can then be measured and a **1** or **0** is **read** as the **result**. Much of the **work done** on **ReRAM** to date has **focused** on **finding appropriate materials** and measuring the resistance state of the cells. **ReRAM designs** are **low voltage**, **endurance** is **far superior** to flash memory, and the **cells** are **much smaller**.



Reduction:
low resistance
Filament



Oxidation:
high resistance
Filament

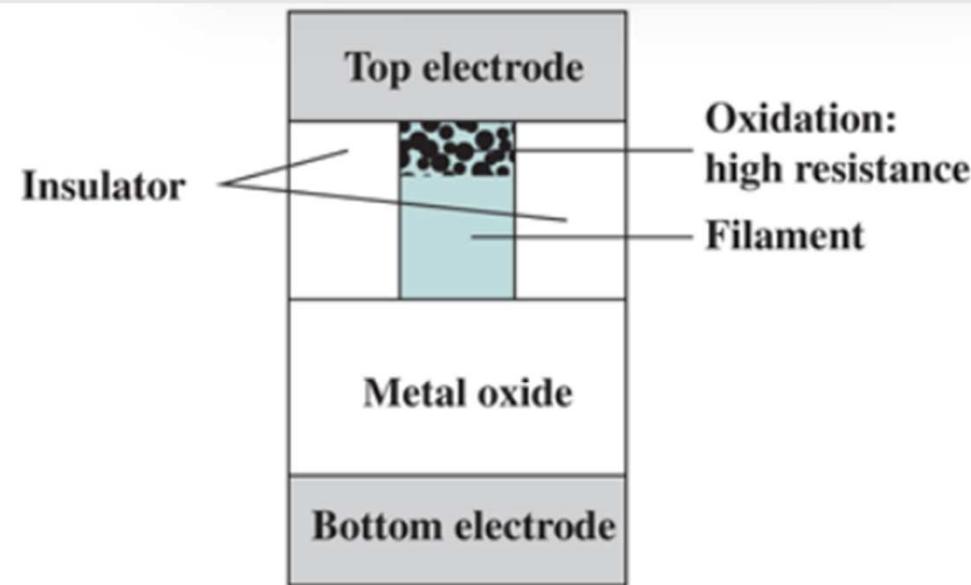
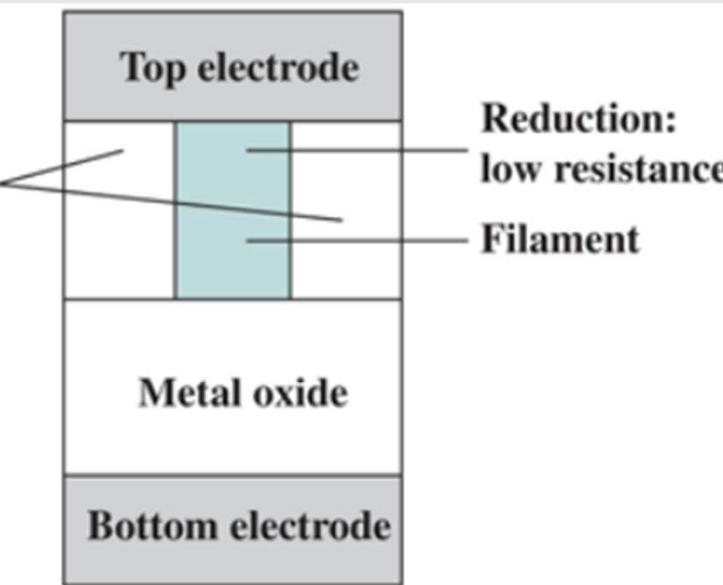
(c) ReRAM

Nonvolatile RAM Technologies

ReRAM

ReRAM is a **good candidate** to **replace or supplement** both secondary storage and main memory.

ReRAM (Resistive Random Access Memory), also known as **RRAM**, is a type of **non-volatile memory** that **stores data** by **altering the resistance** of a **material rather than storing electric charge**, as in traditional memory technologies like DRAM or flash. The key **principle** behind ReRAM is its ability to **switch between different resistance states**, which **represent binary data (0s and 1s)**.



(c) ReRAM

Nonvolatile RAM Technologies

A large, colorful word cloud centered around the words "thank you" in various languages. The words are in different colors and sizes, creating a dense and vibrant composition. The background is black, making the colorful words stand out.



UNIVERSITY OF RIZAL SYSTEM



Management
System
ISO 9001:2015

www.tuv.com
ID 9108653929



Thank you!

Nurturing Tomorrow's Noblest



www.facebook.com/UniversityofRizalSystem



University of Rizal System - Official



www.urs.edu.ph