Name:_____ **Section:** ○ M1 ○ T1

Homework Assignment: Submit via gradescope

1. [1.2] Volume of sale (i.e., the number of parts sold) is a factor when determining which device technology is to be used. Assume that a system can be implemented by FPGA, gate array or standard-cell technology. The per-part cost is $15, $3, and $1 for FPGA, gate array, and standard cell respectively. Gate-array and standard-cell technologies also involve a one-time mask generation cost of $20,000 and $100,000 respectively.

   a. Assume the number of parts sold is *N*. Derive an expression for per-unit cost for the three technologies. Put your answer in the boxes on the right.

   FPGA

   Gate array

   Standard cell

   b. Plot the equations with *N* as the x-axis. [I recommend using a program like excel]

PLACE PLOT HERE

c. Determine the range of *N* for which FPGA technology has the minimal per-unit cost. Note: For ≤ or ≥ bubble-in both "<" or ">" and "=". For example, to answer with *N ≤ 50* you would bubble in "<" and "=" and then write 50 in the box.

N ○ < ○ = ○ > ☐

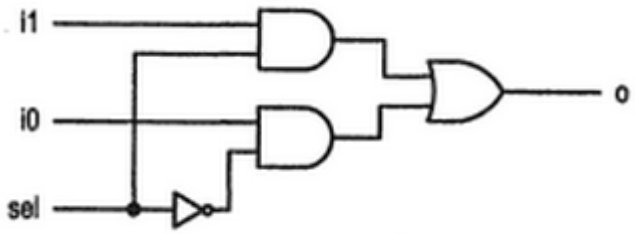
d. Determine the range of *N* for which gate-array technology has the minimal per-unit cost.

☐ ○ < ○ = ○ > N ○ < ○ = ○ > ☐

e. Determine the range of *N* for which standard-cell technology has the minimal per-unit cost.

N ○ < ○ = ○ > ☐

2. [1.3] What is the view (behavioral, structural, or physical) of the following illustration?



○ Behavioral ○ Structural ○ Physical

3. [1.4] What is abstraction? Why is it important for digital system design?

4. [1.5] What is the difference between testing and verification?

5. Did you install and test Vivado? Note: Installation instructions are on the course website.

○ Yes ○ No

6. Design a digital system with four bits of inputs I3 I2 I1 I0 and two bits of outputs O1 O0. At least one of the inputs is always equal to 1. The output encodes the index of the most significant 1 in the input. For example, if I3 I2 I1 I0 = 0101, then the index of the most significant 1 is 2, hence O1 O0 = 10. Hint, you will need a **don't care** somewhere. Turn in....
    a. Complete truth table.

Hexadecimal Digit	Inputs				Outputs	
	I3	I2	I1	I0	O1	O0
0	0	0	0	0		
1	0	0	0	1		
2	0	0	1	0		
3	0	0	1	1		
4	0	1	0	0		
5	0	1	0	1		
6	0	1	1	0		
7	0	1	1	1		
8	1	0	0	0		
9	1	0	0	1		
A	1	0	1	0		
B	1	0	1	1		
C	1	1	0	0		
D	1	1	0	1		
E	1	1	1	0		
F	1	1	1	1		

Bonus: What is this device called?

b. Two 4-variable k-maps.

c. Minimal SOP expressions for O1 and O0

O0

O1

d. VHDL code for the circuit pushed to Github and shared with your instructor.