Lesson 28 Worksheet

For question 1a to 1f, assume you need to implement a **50-tap** FIR filter on a continuous stream on input data from a **16-bit** A/D sampled at **1 MHz**, and have a programmable DSP chip that is rated at **500 MFLOPS** (million floating point operations per second) for single precision floating point operations (fixed point samples are converted to 32-bit floating point numbers). The DSP chip's bandwidth of the external data bus into the DSP chip is **600 Mbytes/second** (from the ADC, to the DAC) and the internal data bus is **1200 Mbytes/second** (to internal RAM)

1a) Approximately, how many math operations (multiplies and adds) are required to implement this filter for each output data point (ignore load/store/decrement/branch instructions)?

1b) To keep up with the stream of incoming data (speed determined by sample rate), how much time does the processor have to calculate each output data point y(n) (in nsec)?

1c) Approximately, what is the M-FLOPS (millions of floating-point operations per second) requirement for this filter? (remember: requirement is dictated by the algorithm requirements)

1d). Approximately, what is the **external I/O** (input/output) requirement to implement this filter (in Mbytes/second)? Remember: External I/O is from what must come in and out of the DSP from external sources (like ADC) or to external destinations (like DAC). Note: assume the filter coefficients h(n) can all be stored in on-chip RAM, so are not part of the external I/O requirement. Also assume you are outputting each y(n) value calculated for each new x(n) sample received. Also, assume the input/output values are 16-bit fixed point numbers.

1e. Approximately, what is the **internal I/O** (input/output) requirement to implement this filter (in Mbytes/second) ? Remember: Internal I/O is the movement of data from on-chip RAM to/from the DSP, plus the external I/O requirement. We assume a Harvard architecture so we can ignore the I/O requirement of the instructions (the program). Note: assume the filter coefficients h(n) are all be stored in on-chip RAM (not registers), so are part of the internal I/O requirement, and assume all data and coefficients are now 32-bit floating point numbers.

1f. Is the processing requirement a greater challenge (compute-bound) or is the I/O requirement a greater challenge (IO-bound) for this filter application on this DSP chip? hint: look at the ratio of (1c)/500 MFLOPS versus the worst case of the ratios of (1d)/600Mbytes/sec and (1e)/1200 Mbytes/sec.