Introduction to EE by Peterson/Wright DFEC

4.3.2 QUANTIZING

Since there are a finite number of outputs from an A/D converter (ADC), output will be a digital signal. After an ADC has sampled the analog signal, it must determine which output to associate with the sampled value. This process is called *quantization*. In order to calculate the quantized (discrete) level of any given sample, we need the voltage limits (V_{max} and V_{min}), and the number of bits, b, of the ADC.

All A/D converters are designed for a specific maximum and minimum input voltage. The maximum voltage, V_{max}, is the highest input voltage that the ADC will correctly convert. Input voltages higher than V_{max} will be treated as though they were V_{max}. Similarly, the minimum voltage, V_{min}, is the lowest input voltage the ADC will correctly convert. Voltages lower than V_{min} will be treated as though they were at V_{min}. Due to these constraints, we must be sure the range of the analog input signal does not fall outside the range V_{max} to V_{min}.

For example, a music studio uses an analog-to-digital converter to record music. The A/D converter accepts signals between a maximum of V_{max} = 4 V and a minimum of V_{min} = -4 V. A particular passage of jazz recorded in the studio produced signals that varied between 2.7 V and -3.6 V. In this case, the analog signals representing the jazz music fell within the converter's range and the music should be digitized accurately.

The number of ADC outputs is based on the number of output lines. The ADC converts the discrete level to a binary number, so there is one line per bit. Consider a one-bit ADC. The bit can be set to either a "0" or "1." This means we can produce two outputs with a one-bit ADC. Similarly, if we have a two-bit ADC we have the combinations "00", "01", "10", or "11." We can produce four outputs with a two-bit ADC. In general, if b is the number of bits, the number of levels that can be represented by an ADC is given by Equation 4.2.

$$\text{levels} = 2^b \tag{4.2}$$

To determine which voltages are quantized to each level, we must know the distance in volts between adjacent levels. This is called the *resolution* of the ADC and is dependent on the voltage range and the number of bits.

$$\text{Resolution} = \Delta V = \frac{V_{max} - V_{min}}{2^b} \tag{4.3}$$

Drill Exercise 4.3 Calculating ADC Resolution.
Given: A 4-bit ADC with V_{max}=10 V and V_{min}=-10 V.
Required: Find the resolution for this ADC. **Answer:** $\Delta V = 1.25 \frac{\text{V}}{\text{Level}}$

In Figure 4.15, we're using a three-bit ADC which has eight outputs. The eight levels are labeled "0" to "7" and not "1" to "8" because we have to represent the levels with binary codes. The lowest value that can be represented is all zeros, hence we start at level "0." Besides, it takes four bits to represent the number "8."

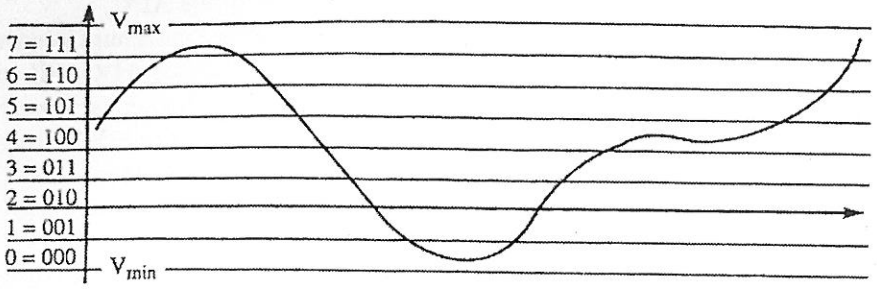

Figure 4.15 Dividing V_{max} and V_{min} into eight discrete levels.

To improve the resolution is to make it smaller. We can make the resolution smaller by either changing V_{max} and V_{min} (to decrease $V_{max} - V_{min}$), or increasing the number of bits.

Drill Exercise 4.4 Calculating ADC Number of Bits.
Given: An ADC with V_{max} = 10 V and V_{min} = -10 V.
Required: Find the number of bits to produce a resolution of 100 mV or better.
Answer: 8 bits.

Referring again to Figure 4.15, to calculate the resolution for the three-bit ADC, we need the voltage range. If V_{max} = 10 V and V_{min} = -4 V, use Equation 4.3 to determine the resolution.

$$\Delta V = \frac{V_{max} - V_{min}}{2^b} = \frac{10 - (-4)\ \text{V}}{2^3\ \text{levels}} = 1.75\ \frac{\text{V}}{\text{level}}$$

There are 1.75 V between each level. Level "0" is used for all voltages from V_{min} to $V_{min} + \Delta V$, i.e., from -4 V up to, but not including -2.25 V. This can be mathematically expressed as [-4.00 V, -2.25 V). A sample value of -3.42 V would be quantized to level "0."

You can manually determine the voltage range for each level in a similar manner and the results are summarized in Table 4.1. After making all these calculations, the ADC level can be determined for any sample value. For example, a sample of -1.5 V will be quantized to level "1." This is fine for a small number of bits, but there are 65,536 levels for a 16-bit ADC and it would be unreasonable to take this approach for finding the ADC level.

Table 4.1 Example Quantization Voltages for Three-Bit ADC

Level	Voltage Range	Level	Voltage Range
0	[-4.00 V, -2.25 V)	4	[3.00 V, 4.75 V)
1	[-2.25 V, -0.50 V)	5	[4.75 V, 6.50 V)
2	[-0.50 V, 1.25 V)	6	[6.50 V, 8.25 V)
3	[1.25 V, 3.00 V)	7	[8.25 V, 10.00 V)

If instead, you count up the number of "resolutions" the sample value is from the minimum, you can more easily find the ADC level. Mathematically, the expected level for the sample voltage can be found using Equation 4.4

$$\text{Expected Level} = \text{E.L.} = \frac{V_{in} - V_{min}}{\Delta \text{V}} \tag{4.4}$$

For this specific example, we can calculate the expected level for a sample value of -1.5 V using Equation 4.4:

$$\text{E.L.} = \frac{-1.5 - (-4)\,V}{1.75\ \text{V/level}} = \text{Level } 1.43$$

Since there is no Level 1.43, the ADC will quantize to the nearest level. Although there are many ADCs that round, we will use a simpler method, truncation. This sample has not made it to Level 2, so the ADC will quantize to Level 1 and output the code for Level 1.

There is some error associated with this quantization process and there are two ways to look at it:

1. The voltage associated with Level 1 is -2.25 V and our sample value is -1.5 V. There is a difference of -1.5 V -(-2.25 V) = 750 mV.

2. The Expected Level is Level 1.43 and the ADC quantized to Level 1. There is an error of 0.43 Levels. The resolution specifies the voltage associated for a level, so the error can be calculated as $(0.43\ \text{Level}) \times 1.75\ \frac{\text{V}}{\text{Level}} = 750$ mV.

The *quantization error*, Q.E., is the difference between the *actual* input voltage and the *represented* input voltage. Equation 4.5 summarizes the methods for finding the quantization error. The only way to decrease the quantization error is to improve the resolution so the sample will be associated with a closer level.

$$\text{Quantization Error} = \text{Q.E.} = V_{in} - V_{\text{level}} = \text{Level}_{\text{truncated}} \times \Delta V \tag{4.5}$$

The largest quantization error for an input voltage within the ADC's range (V_{max} to V_{min}) occurs when the ADC is maxed out. Calculating the level for a sample value of V_{max} always results in one level higher than the ADC can produce. In our example,

$$\text{E.L.} = \frac{10 - (-4)\,V}{1.75\,\text{V/level}} = \text{Level } 8$$

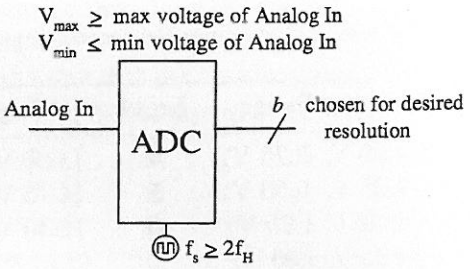

Figure 4.16 Complete block diagram of typical analog-to-digital converter.

The ADC would have to quantize to Level 7 and the error will be one level. This amount is equal to the the resolution, so

$$\text{Maximum Quantization Error} = \text{Q.E.}_{max} = \Delta V \tag{4.6}$$

Increasing the number of bits increases the number of levels and decreases the resolution. Better resolutions result in smaller quantization errors, which explains why the analog signal can be more accurately represented with more bits. This is; however, only improving the sampling process along one axis. The sampling frequency must still meet the Nyquist criterion or the signal will be distorted, no matter how many bits are used. A complete block diagram of an ADC is shown in Figure 4.16, and includes specifications for the voltage range, bits, and sampling rate.

4.3.3 ENCODING

The third step of A/D conversion is to produce an output signal on each of the output lines. The ADC will generate a binary code to represent each level and produce our standard 0 V for "0" and 5 V for a "1." In Figure 4.15, the binary codes for each level are listed next to the level number. Note that the lowest level, 000, is determined by V_{min} regardless of the voltage value associated with it; i.e., Level 000 is not necessarily associated with 0 V.

There is an output line for each bit. In the case of a 3-bit ADC, there will always be three bits output, so Level 1 will be encoded as 001 and the ADC will output 0 V, 0 V, and 5 V on parallel lines as shown in Figure 4.17. Each output value lasts until the next sample is taken and this is determined by the sampling frequency.