RISC-V Exercise **Name:_____**

See Collaboration and GenAI policy at the end of this document.

Given this RISC-V assembly program

```
        addi    x5, x0, 9       # x5 = number of values in array
        la      x6, array       # x6 = address of array 0X10000000
        lw      x7, 0(x6)       # x7 = initial value
loop:   addi    x6, x6, 4
        lw      x10, 0(x6)
        add     x7, x10, x7
        subi    x5, x5, 1
        bne     x5, x0, loop
done:   j       done            # infinite loop (breakpoint)

        # initialize data in the array

array:  .word 0x5, 0x4, 0x10, 0x3, 0x12, 0x1, 0x7, 0x4, 0x8, 0x2
```

1. How many total assembly instructions are executed by this program [include the first "j done"]?

2. For the Single Cycle unpipelined RISC-V processor, every instruction executes in the same amount of time (during one long clock period). If each instruction executes in 50 nsec, how long does it take the program to run?

3. Now you will analyze this program's execution on the H&P 5-stage RISC-V pipeline using the attached spreadsheet file riscv_template.xlsx (tab "**with stalls and no forwarding**"). Assume this 5-stage pipeline has no support for forwarding but has hardware interlocks to stall when necessary, and branching delays similar to figure C.19 in your textbook. Add all the instructions executed by this program, and put the 5 stages (IF ID EX M WB) for each instruction with the proper stall cycles inserted to prevent any hazards from occurring.

4. How many total cycles did it take for this program to run?

5. If each cycle takes 11 ns, how long does it take the program to run?

6. What is the speedup of this 5-cycle pipelined RISC-V processor without forwarding versus the original single-cycle RISC processor?

7. What is the average cycles per instruction (CPI) for this 5 cycle pipelined RISC-V processor without forwarding?

8. Now you will analyze this program's execution on the H&P 5 stage RISC-V pipeline using the attached spreadsheet file mips_template.xlsx (tab "**with forwarding & branch fix**"). Assume this 5-stage pipeline now has support for forwarding, but also has hardware interlocks to stall if necessary, and has improved branching, similar to figure C.25 [note: assume the branch decision is made in stage ID, not stage EX] in your textbook. Add all the instructions executed by this program, and put the 5 stages (IF ID EX M WB) for each instruction assuming forwarding, and add the proper stall cycles inserted to prevent any hazards from occurring if needed. Do not **reorder** any of the instructions.

9. How many total cycles did it take for this program to run?

10. If each cycle takes 11 ns, how long does it take the program to run?

11. What is the speedup of this 5-cycle pipelined RISC-V processor with forwarding versus the original single-cycle RISC processor?

12. What is the average cycles per instruction (CPI) for this 5-cycle pipelined RISC-V processor with forwarding?

13. Now you will analyze this program's execution on the H&P 5 stage RISC-V pipeline using the attached spreadsheet file mips_template.xlsx (tab "**forward & BF & reorder**"). Assume this 5 stage pipeline has all the same features as problem #8, but your compiler reorders the instructions to help fill stall slots (and still produces the correct code). Add all the instructions executed by this program to the spreadsheet, and put the 5 stages (IF ID EX M WB) for each instruction.

14. How many total cycles did it take for this program to run?

15. If each cycle takes 11 ns, how long does it take the program to run?

16. What is the speedup of this 5-cycle pipelined RISC-V processor with forwarding, branch fix, and reorder versus the original single cycle RISC processor?

17. What is the average cycles per instruction (CPI) for this 5-cycle pipelined RISC-V processor with forwarding?

Documentation Statement: The only collaboration allowed with classmates is for general questions, such as how the 9 assembly instructions work and relate to the block diagrams of figures C.18, C.19 and C.25. All the work filling out the spreadsheets and answering the above questions must be your own work. Do not look at each other's spreadsheets or answers to the above questions. All collaboration must be clearly documented below; copying another person's work, with or without documentation, will result in **NO** academic credit.

Similarly, regarding the use of GenAI use of generative AI (e.g., ChatGPT) or search engines is "level 1: Organizational / Explanatory use of GenAI." For example, you can prompt GenAI on how the 9 assembly instructions work and relate to the block diagrams of figures C.18, C.19 and C.25; however, all the work filling out the spreadsheets and answering the above questions must be your own work. Do not ask GenAI to produce specific answers to the spreadsheets or the above questions. Any use of GenAI or internet searches must be clearly documented, including all prompts used. Failure to follow this policy will result in **NO** academic credit. One warning about GenAI and RISC-V: besides the common problem of GenAI hallucinations, there are different versions of RISC-V, different from this assignment, so GenAI could lead you astray.

Insert your Documentation Statement Below: