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Final report

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Purpose and scope

The automation of schematic designs for mixed-signal and analog circuits has been an outstanding challenge for many years. While analog mixed signal (AMS) circuits typically have a very small transistor count compared to digital transistors in a system, they take a disproportionate amount of time to design, require experts, and can be a barrier to the overall efficiency of small design teams. The USC POSH team successfully addressed these issues by applying new insights and modern Machine-Learning (ML) guided optimization techniques.

Our approach is inspired by, and is a significant generalization of, earlier efforts that used very specific searches for discovery. Starting in the mid-1990s [1][2][3] with the observation that most analog circuits use a small number of transistors, a numerical study of all possible configurations of a two-transistor circuit was initiated. This inefficient exhaustive search led to the discovery of two low-noise amplifiers, one of which not only provided superior performance but also showed for the first time that thermal noise could be canceled. Independently, in the early 2000s, we noticed that electromagnetic waveguide design was limited by available theory and human imagination and waveguides were largely confined to symmetric structures or periodic dielectric designs. We developed a numerical optimization approach to explore different waveguide materials and configurations to discover completely new aperiodic waveguide designs with remarkable performance [4][5]. Around 2010, this approach was adapted by another USC group to discover aperiodic patterns of vertical nanowires for solar cells with unprecedented efficiencies [6]. Also, during this period, we demonstrated the existence of a class of non-intuitive computer-generated aperiodic semiconductor heterostructure band-edge profiles in electronic devices and small circuits capable of delivering precision analog functionality [7][8].

Analyzing these early approaches and their potential application to design automation we realized that the failure of past attempts to use conventional approaches to optimization (most notoriously, convex optimization) to automate creation of analog circuit schematics was simply lack of essential design information. Absent proper prior information (priors) the search space becomes ill-conditioned such that mapping experimentally accessible design parameters to desired (objective) output metrics is infeasible. Application of contemporary unsupervised ML techniques is also not possible due to the lack of large training datasets.

Our key insight is that it is necessary to create mechanisms to insert appropriate priors to enable an efficient automated design process. We did this in two ways, first by exploiting the existence of a few known good designs (KGD) and second by using expert human-in-the-loop while developing the search algorithm. The KGD included schematic, layout, physical realization in silicon, and experimental test and measurement results. Remarkably, this approach succeeded beyond our initial expectations. We were able to show dramatic speedup in automated schematic generation for analog mixed-signal circuits, automated layout generation, and verification in physical silicon. We also showed transfer learning could be used to map designs to different technologies and that local optimization could be used to finetune and enhance performance.

The following summarizes high-level results and aspects of our participation in the DARPA POSH/IDEA program.

USC-POSH

The core activity of the USC-POSH effort centered around development of software to explore the design space for analog circuits. Highlights of this software that we called the Analog Mixed-signal Parameter Search Engine (AMPSE) are illustrated in Fig. 1. The search engine uses gradient decent on a neural network to efficiently explore the design space of circuit schematics that meet user design objectives.

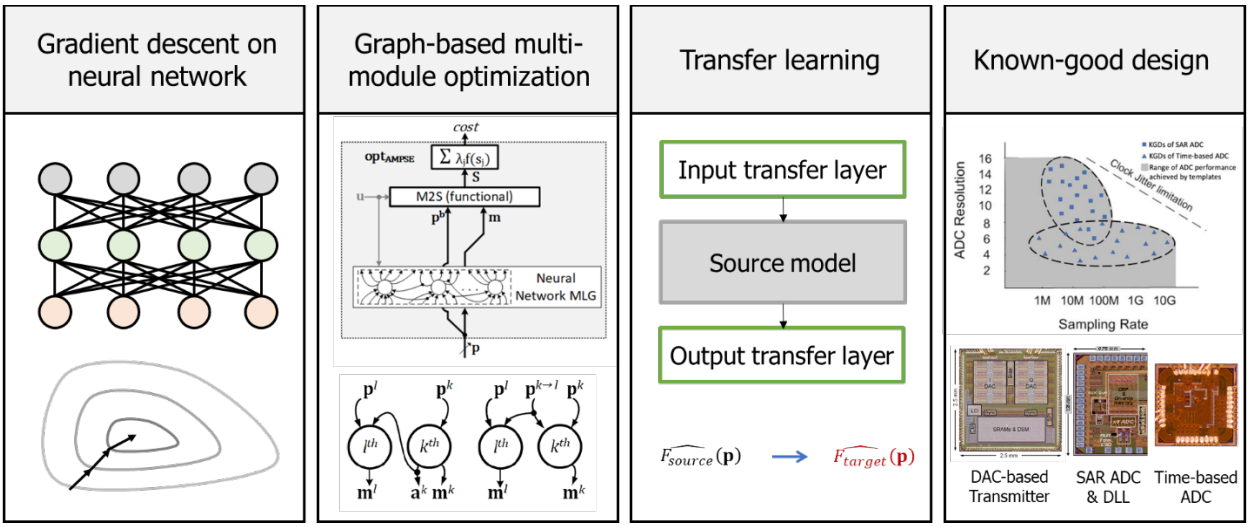

Figure 1: Highlights of AMPSE functionality and capabilities. The search engine uses gradient decent on a neural network with an option for graph-based multimodule optimization. Transfer learning has successfully been demonstrated for circuit layout and design in different technologies. The success of AMPSE is in large part due to the use of KGD to seed the accessible design space.

The USC-POSH program also engaged with and was supported by commercial, academic and government entities. Collaboration partners included GlobalFoundries (GF) who provided no-cost access to MPW tape-outs and fabrication in their GF14LPP and later GF12LP FinFET technology. We also worked with Sandia National Laboratories and provided guidance for development of their Xyce (SPICE simulator) and their rapid optimization library (ROL) for local optimization. We also collaborated with the University of Minnesota (UMN) and others for automated layout generation in GF12LP.

Figure 2 illustrates the complete USC-POSH Analog Mixed Signal (AMS) circuit design-flow and partner interactions.

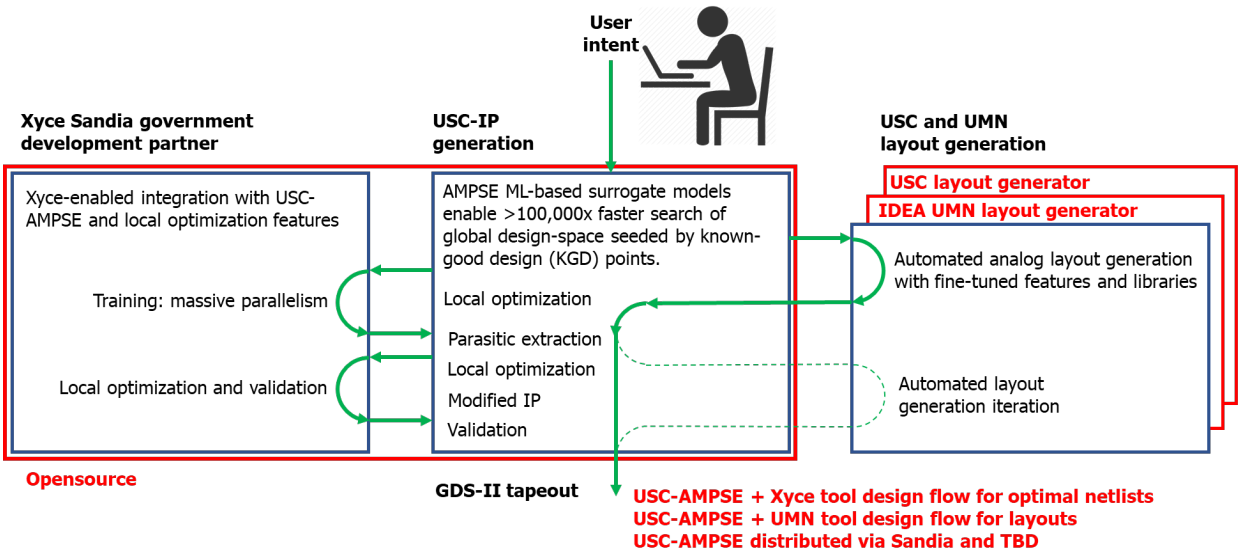

Figure 2: The USC-POSH AMS circuit design-flow and partner interactions.

USC-POSH has demonstrated an ML-based AMS design flow with silicon validation. The AMPSE tool development focused on enabling small teams to achieve competitive designs that can meet a wide range of target (objective) specifications. AMPSE uses ML to created surrogate models that dramatically accelerate simulations and expand the search space. The USC-POSH effort also created numerous ADC, PLL, DLL, and DAC tapeouts in different technologies that ranged from 65nm to 12nm CMOS. Several AMS IP blocks developed by the USC-POSH team are available on GitHub [9].

The USC-POSH program influenced activity at Sandia and UMN and at USC the AMPSE tools were used in graduate-level courses on circuit design.

An example of AMPSE tool value for a SAR ADC design example is illustrated in Fig. 3. AMPSE uses ML to create thousands of new designs (over 8000 new netlist versions for this example). A pareto boundary (gold dots) forms that defines the feasible from the infeasible region in the metric-space plane of number of bits versus sampling rate. Accessible designs are to the left of the pareto boundary in the Fig. The designs span a very large range of performance specifications (in this example 4b to 11b linearity and 120MS/s to 740MS/s sampling rate). Green dots with the indicated figure of merit (FoM) are the SPICE verified performance. The FoM is in units of fJ per conversion step. In this example, the AMPSE tool directly creates the set of pareto-optimal designs in less than 20 minutes on a laptop, demonstrating that what traditionally can take years of work is reduced to minutes on a PC. While there is a few percent reduction in accuracy compared to SPICE simulations, in nearly all cases this can be remedied by separately applying local optimization techniques.

AMPSE also provides testbenches for validation.

In principle, AMPSE enables non experts, for example digital circuit designers, to create viable AMS circuits efficiently and, in this way, enable small circuit design teams.

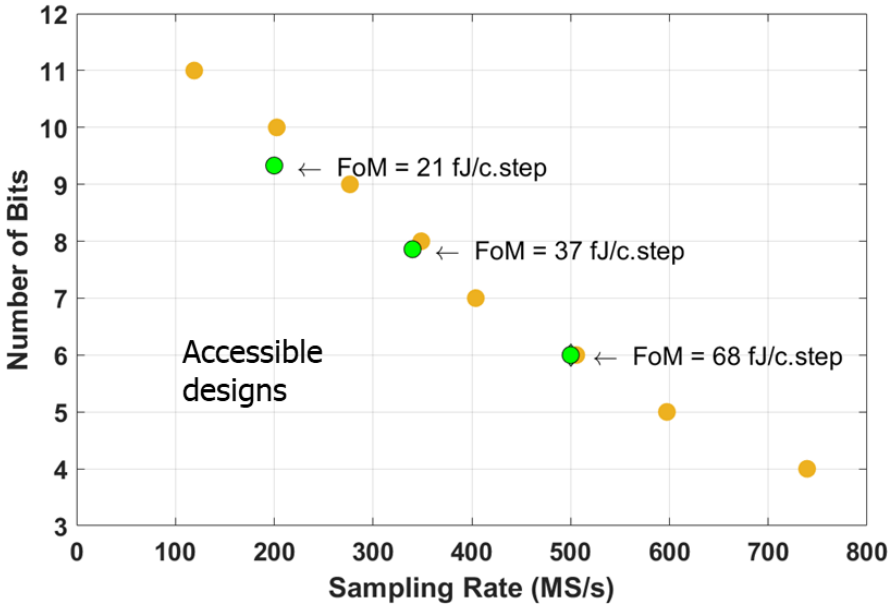

Figure 3: SAR ADC pareto boundary (gold dots) for number of bits versus sampling rate that was created by AMPSE. The designs cover of very large range of performance metrics. Accessible designs are to the left of the boundary. Green dots with the indicated figure of merit (FoM) are the SPICE verified performance. The FoM is in units of fJ per conversion step.

In general, AMPSE ML-based surrogate models enable >100,000x faster search of global design-space seeded by known-good design (KGD) points. Importantly, new versions of netlists that satisfy a wide range of user specifications and attain a high figure of merit (FoM) can be found. Specification range extension with, for example, a SAR ADC can be 5x in sampling and 16x in resolution span. As part of the USC-POSH program, AMSPE has been used for ADC, DAC, PLL and DLL design.

Local optimization with Xyce

While AMPSE enables rapid exploration of a global design space it does so at the cost of some accuracy. After finding a viable global solution, local optimization can be used to refine parameter values and finetune the design. We collaborated with Sandia National Laboratory to assist with development of local circuit schematic optimization using their Xyce tool. We explored both constrained and unconstrained optimization but rapidly moved towards developing unconstrained local optimization to avoid the complexity of constrained optimization that slowed development. Several bugs and errors in Xyce were discovered that also slowed development. Many of these have been fixed, including a complete rewrite of the AC sensitivity code.

We delivered opensource Python and Xyce code to Sandia that included local optimization algorithms for unconstrained Powell line search with bounds, unconstrained BFGS with bounds, and constrained sequential quadratic programing (SQP).

Testbenches were delivered for a voltage divider and an OPAMP containing more than 80 transistors and 30 design variables that has been designed and validated in GF65 silicon and ported to opensource PTM65. The use of gradient-based BFGS allowed direct comparison with the Cadence Spectre proprietary ADE-GXL suite. For development purposes the analog test circuit input metrics were transistor dimensions, output load, voltage bias, and voltage operating point. The output metrics were DC power, Total Harmonic Distortion (THD), bandwidth, and gain. We used Xyce .AC, .TRAN, .DC, and .FOUR. We found the Cadence tools gave results faster than our approach because of our use of an optimizer external to Xyce and the subsequent necessity of passing data through input and output interfaces. To address this issue the Sandia group decided to incorporate local optimization into Xyce. This approach to increasing efficiency involved integration of the Sandia Rapid Optimization Library (ROL) into Xyce.

USC-POSH continued to contribute to the effort by providing optimization code and detailed working examples of circuit optimization, performance comparison with Cadence's Optimization toolbox ADE-GXL, and descriptions of various fixes required in Xyce. We highlighted the need to enable optimizations on multiple analyses at the same time, i.e., the ability to perform .DC, .AC, and .TRAN at each inner-loop optimization iteration. We also highlighted the need for user flexibility in precise specification of the optimization problem.

To enable free exchange of proprietary PDK and circuit design information, Sandia, USC, and GF executed a multi-way NDA. In addition to worked examples of optimization of analog circuits, Sandia received USC's silicon-validated KGDs (schematic, layout, testbenches), including OPAMP (GF65), SAR ADC (GF 65), and a 6-pole Butterworth filter (GF 65). Additional tools were also developed including a parser for Spectre (*.scs) that was to be integrated into Xyce.

The challenge of opensource PDKs

We explored a number of ways to remove the barrier to adoption of opensource tools. This included the idea of sanitizing and de-sanitizing schematics of PDK information. Another approach was to modify existing opensource PDKs to become compatible with proprietary PDKs. To explore this, we started with known good design (KGD) of 10-bit linearity OPAMP and 6-pole triple-biquad 7-MHz Anti-Alias Filter (AAFilter) designed, simulated at 39 PVT corners, fabricated and performance measured in silicon in the GF65LPe process technology. The designs use low-Vt (LVT) PFET, regular Vt (RVT) NFET and thin-oxide native NFET GF65LPe transistors. The challenge was to transition the KGD from the proprietary GF65LPe KGD to opensource Predictive Technology Model 65 (PTM65) and create a PTM65 device library in Cadence for schematic capture and simulation.

PTM65 targets bulk MOSFET, it has bsim4v5 model decks, with no binning. Importantly, multifinger device layout parasitics and strain-related device performance variation is not captured by the model. PTM65 has only one NFET and one PFET device model and has no process corner information other than typical. There are also no resistor or capacitor devices other than ideal. With these and other limitations, PTM is of little utility for translation to practical, fabricable designs with acceptable yield in foundry processes.

To preserve the OPAMP architecture shown in Fig. 4, we created a thin-oxide native-nfet PTM model which is a reduced Vt version of existing PTM65 model. The geometry parameters of each transistor were preserved (i.e., no change in L and W) in the schematic as we migrated from GF65 to PTM65 for estimated extrinsic device parasitics and we maintained multiplicity of devices in the PTM65 OPAMP schematic as in the GF65 schematic. Wiring capacitance and resistance is not included or estimated in either the GF65 or the PTM65 schematic. We also created a PTM65 device library in Cadence for schematic capture and simulation.

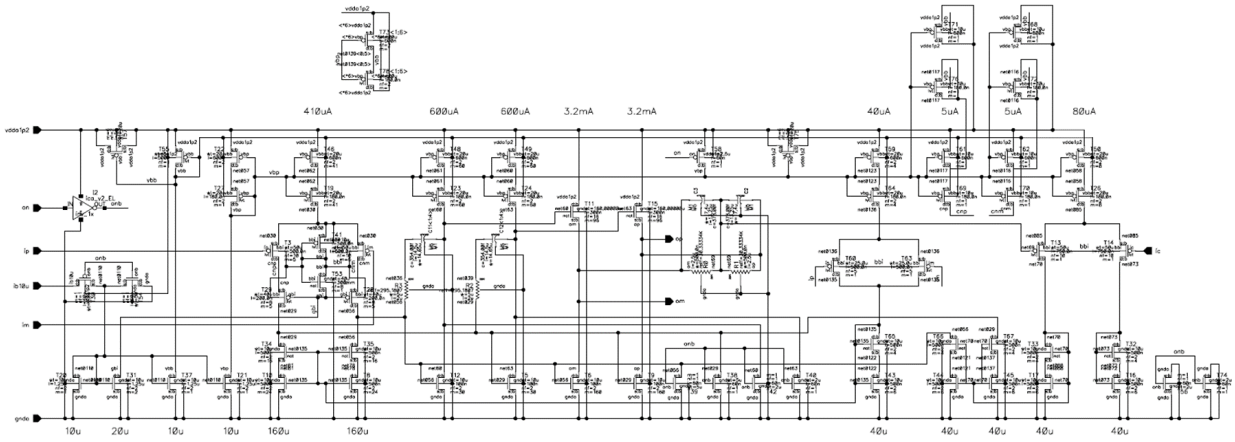

Figure 4: Schematic of multistage, differential input, differential output OPAMP with common-mode feedback control circuit designed and validated in GF65LPe process technology. The design comprises of 87 transistors including subcircuits.

The following table illustrates our success in using this approach to map the OPAMP and 6-pole filter designs from proprietary GF65LPe KGD to opensource Predictive Technology Model 65 (PTM65).

Opamp	GF65, GF65Bias	PTM65+PTM65 Native Fets
Open-loop gain (dB)	79.24	76.12
Fu (MHz)	150.00	99.18
Phase margin (degrees)	53.08	50.14
6-pole AA-filter		
DC gain (dB)	-0.005631	-0.004844
f_3dB (MHz)	7.079	7.244
f_50dB (MHz)	18.47	18.33
IM3 from DFT plot (dB)	62.08	66.86
Estimated linearity in bits from IM3	10.52	11.31
Integrated output (input) noise voltage 10 Hz to 100 MHz (uVrms)	144.20	167.10
Avg. Power (mW)	30.14	29.45

High-performance time-domain ADC design example

The development of AMPSE is predicated on the idea that KGD can be used to seed the search space of many designs with different performance metrics. As part of the USC-POSH effort new designs and new architectures were explored and implemented in silicon to create new KGDs.

An example of this work is a medium resolution, high conversion speed and high power/area efficiency ADC. In this case an 8-bit time-domain ADC achieving 10GS/s conversion speed with only two time-interleaved (TI) channels was demonstrated in silicon. The circuit consists of a successive approximation register (SAR) time-to-digital converter (TDC) with sub-picosecond resolution time quantization. The throughput of the SAR TDC is enhanced by delay-tracking pipelining to enable 5GS/s single-channel conversion. At the circuit level, the reference time generation for the SAR TDC is realized by a selective delay tuning (SDT) cell for high efficiency and small reference time variation. The design was fabricated in the GF 14nm FinFET CMOS technology. The ADC has a measured 37.2dB signal-to-noise and distortion ratio (SNDR) and a 50.6dB spurious-free dynamic range (SFDR) at the Nyquist input frequency. The circuit has a 24.8fJ/conv-step Walden figure of merit. The active area of the fabricated circuit is only 2850μm^2. Figure 5 is a chart comparing ADC performance to other published results [10].

	This work		ISSCC 20 M. Zhang[3]	CICC 19 M.Hassanpourghadi[4]	JSSC 19 D. Oh	JSSC 18 S. Zhu[5]	ISSCC 20 Z. Zheng	VLSI 19 M.Guo[1]
Architecture	Time-domain ADCs						Voltage-domain ADCs	
	Delay-tracking pipelined-SAR TDC		Interpolation TDC	Flash TDC	Interpolation TDC	Flash TDC	Dynamic Pipeline	TI-SAR
Technology	14nm CMOS		65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	28nm CMOS	28nm CMOS
Supply (V)	0.8		1	1	1	1	0.9	1
Resolution (bits)	8		8	7.3	6	8	6	10
# of TI channels	2	1	4	2	1	1	1	16
Sample rate (GS/s)	10	5	10	10	2.5	2	3.3	5
Power (mW)	14.8	7.4	50.8	29.7	7.5	21	5.5	29
SFDR@Nyq (dB)	50.69	53.12	52.8	40.7	45.07	48.36	45.5	59.6
SNDR@Nyq (dB)	37.2	40.8	40.1	32.5	33.84	40.68	34.2	48.5
FOM_{Walden} @Nyq(fJ/conv-step)	24.8	16.6	61.5	86.0	74.7	119	40.0	26.7
Active area (um^2)	2850	1425	95000	15000	120000	80000	16600	103000

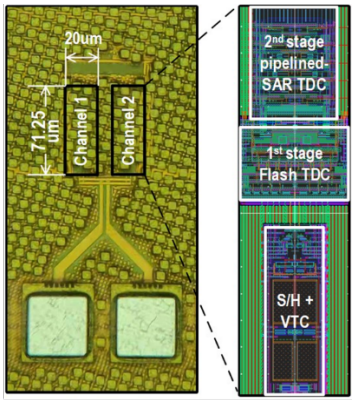

Figure 5: Comparison chart and die photograph of a 10 GS/s 8b 25fJ/c-s 2850um^2 two-stage time-domain ADC using delay-tracking pipelined-SAR TDC with 500 fs time step implemented in a 14nm FinFET CMOS technology [10]. Remarkable performance is achieved.

We have published several papers as part of the USC-POSH program. The topics include design methodology and creation of new known good designs. In the following, we provide a summary of the publications [10-20].

Opensource repository

A number of KGDs, AMPSE, and other support material is available on a GitHub repository [9]: https://github.com/USCPOSH

Figure 6 shows the organization of files and documentation for KGD and AMPSE that is available on the USC-POSH GitHub site.

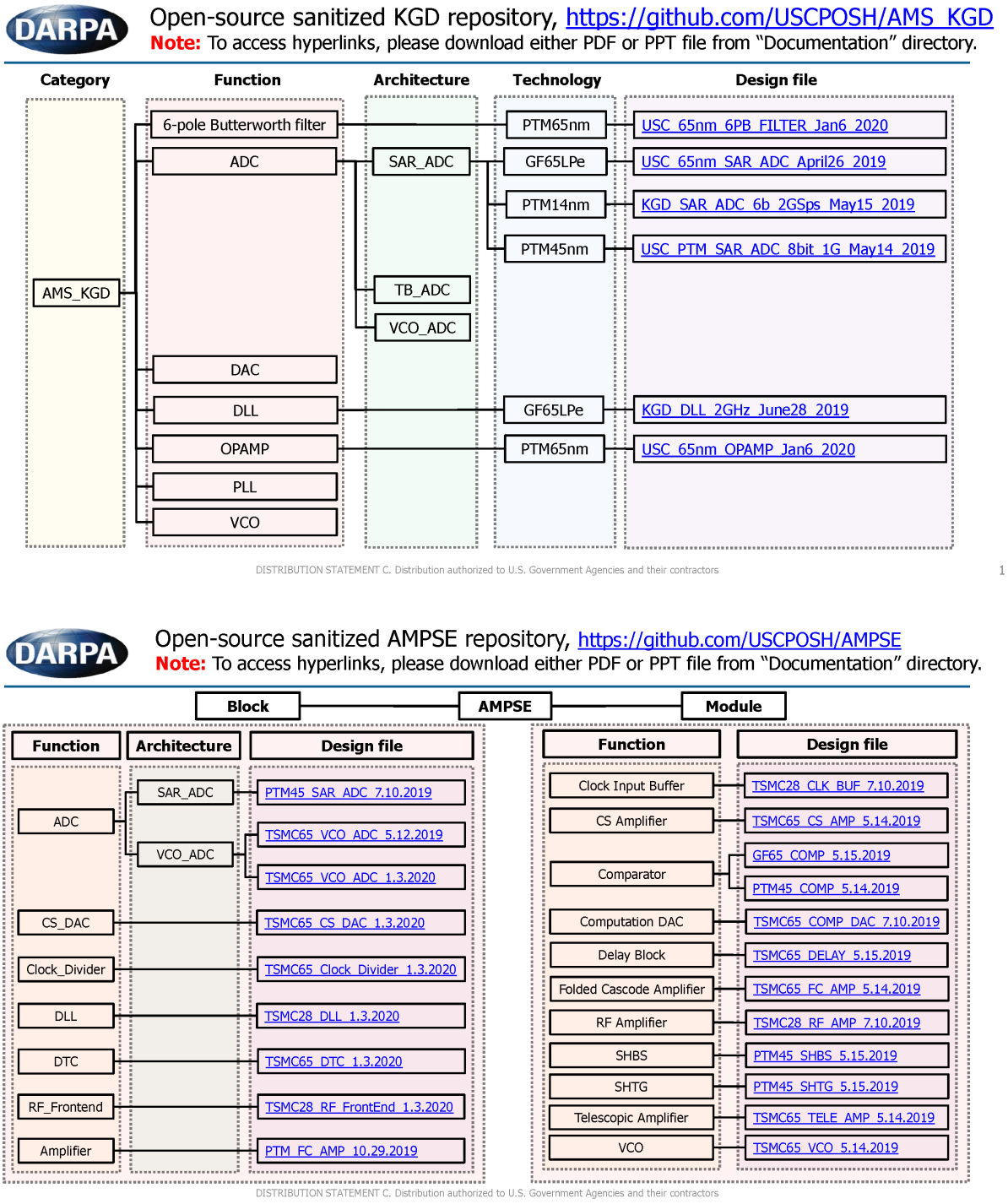

Figure 6: Organization of files and documentation for KGD and AMPSE available on the USC-POSH GitHub site: https://github.com/USCPOSH

USC-POSH new known good designs

1. A 10GS/s 8b 25fJ/cs 2850um^2 Two-Step Time-Domain ADC Using Delay-Tracking Pipelined-SAR TDC with 500fs Time Step in 14nm CMOS Technology, Juzheng Liu, Mohsen Hassanpourghad, Mike Shuo-Wei Chen, in IEEE International Solid-State Circuits Conference (ISSCC), 10.1, Feb. 2022

In this work, an ADC KGD design targeting medium resolution, high conversion speed and high power/area efficiency is explored. We demonstrate an 8-bit time-domain ADC achieving ten-GS/s conversion speed with only two time-interleaved (TI) channels. A successive approximation register (SAR) time-to-digital converter (TDC) is implemented for the sub-picosecond resolution time quantization with high power/area efficiency and low jitter. The throughput of the SAR TDC is enhanced by a unique delay-tracking pipelining technique to enable a 5GS/s single-channel conversion. At the circuit level, the reference time generation for the SAR TDC is realized by a selective delay tuning (SDT) cell for high efficiency and small reference time variation. Fabricated in the 14nm FinFET CMOS technology, this ADC achieves a 37.2dB signal-to-noise and distortion ratio (SNDR) and a 50.6dB spurious-free dynamic range (SFDR) at the Nyquist input frequency, leading to a 24.8fJ/conv-step Walden figure of merit with an active area of only 2850μm^2.

2. A Fractional-N Digital MDLL with Background Two-Point DTC Calibration Achieving -60dBc Fractional Spur, Qiaochu Zhang, Shiyu Su, Cheng-Ru Ho, and Mike Shuo-Wei Chen, in IEEE International Solid-State Circuits Conference (ISSCC), 29.4, Feb. 2021.

In this MDLL KGD, we propose a background digital calibration algorithm that corrects the timing error of the digital-to-time converter in the reference injection path. The proposed two-point digital-to-time converter (DTC) calibration algorithm is capable of simultaneous estimation and compensation of DTC gain and offset errors (the major source of timing error of the reference injection). The calibration engine is implemented in the digital domain and incurs a minimum analog design overhead. TDC dithering and comb-filter-assisted dither cancellation are proposed to enhance the accuracy of the DTC error estimation and allow high-precision DTC error estimation (>10-bit accuracy) with a coarse and nonlinear embedded TDC (<5-bit), showing a huge hardware overhead reduction compared with the prior art. The proposed background calibration for DTC achieves >25dB improvement in reference and fraction spurs, constantly tracking PVT variations within a tolerable range. The digital MDLL prototype implemented in a 65nm CMOS technology achieves a lower fractional spur at -60dBc among the state-of-the-art MDLLs and injection-locked PLLs (at the time of the publishing the paper).

3. A Fractional-N Digital MDLL with Injection Error Scrambling and Background Third-Order DTC Delay Equalizer Achieving –67dBc Fractional Spur, Qiaochu Zhang, Hsiang-Chun Cheng, Shiyu Su, and Mike Shuo-Wei Chen, in IEEE International Solid-State Circuits Conference (ISSCC), 14.1, Feb. 2023.

We demonstrate the combination of injection error calibration and randomization for reducing spurs while maintaining a low noise floor in a MDLL KGD. A background third-order delay equalizer that estimates and corrects DTC offset, gain, and integral nonlinearity (INL) errors is implemented. The equalizer corrects different DTC error components at multiple points in the MDLL and thereby relaxes the analog

implementation requirement compared to the prior art. The equalizer linearizes the DTC and hence largely suppress the spurs with a minimum overhead. Furthermore, we propose an injection error scrambling technique allowing more spur reduction beyond the correction limit of the third-order delay equalizer. The proposed injection error scrambling scheme achieves a higher degree of randomization compared with prior arts and thus results in a lower spur level. A digital MDLL prototype was implemented in 65nm CMOS technology that demonstrates 800fs RMS jitter and –67dBc fractional spur with 29dB spur suppression, and performance that is maintained over PVT variation. The fractional spur level is the lowest among the state-of-the-art MDLLs and injection locked PLLs.

USC-POSH design methodology

4. Automated Analog Mixed Signal IP Generator for CMOS Technologies, Mohsen Hassanpourghadi, Qiaochu Zhang, Praveen Sharma, Jaewon Nam, Shiyu Su, Subhajit Chowdhury, Jagannathan Sathyamoorthy, Walter Unglaub, Fangzhou Wang, Mike Shuo-Wei Chen, Sandeep Gupta, Anthony Levi, Wes Hansford, William Taylor, in Government Microcircuit Applications and Critical Technology Conference (GOMACTECH), 2019.

The automation of analog mixed signal schematic generation has remained a challenge for many years. Our approach is inspired by and is a generalization of earlier efforts that used very specific searches to discover new behavior. The proposed automated analog and mixed signal (AMS) circuit generator flow consists of three major steps. The first step is to prepare the parameterized module library. This step consists of breaking a known-good design (KGD) into smaller independent modules which then serve as building blocks for a parameterized library. We then explore the relationship between design parameters and the performance metrics of the module. In our design flow, we explore the possibility of deriving a sufficiently accurate regression model for all the modules, leading to an expedited parameter search process, as the computational requirement for using the regression model is significantly less in comparison to SPICE simulation. Once the module library is created and user intention is well captured at the module level, the appropriate modules for each block are selected using a selection filter. We use a Python script to read the module library and search for modules matching the metrics decomposed in the previous step. Through this process, a few candidates that meet the constraints are selected. They are further validated through SPICE simulation. If the performance is accurate enough and meets the target specification, the best candidate is chosen for generating the final netlist. Otherwise, a local optimization routine can be applied to fine tune the parameter around the selected candidate.

5. TAFA: Design Automation of Analog Mixed-Signal FIR Filters Using Time Approximation Architecture, Shiyu Su, Qiaochu Zhang, Juzheng Liu, Mohsen Hassanpourghadi, Rezwan Rasul, and Mike Shuo-Wei Chen, in IEEE/ACM 27th Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 2022.

This work presents a systematic design methodology to automate AMS FIR filter design using a time approximation architecture without any tunable passive components, such as switched capacitors or resistors. We find that it not only enhances the flexibility of the filter but also facilitates design automation with reduced analog complexity. The proposed design flow features a hybrid approximation scheme that automatically optimize the filter's impulse response in the presence of time quantization effects. We find significant

performance improvement with minimum designer's efforts in the loop. Additionally, a layout-aware regression model based on an artificial neural network (ANN), in combination with gradient-based search algorithm, is used to automate and expedite the filter design. With the proposed framework, we demonstrate rapid synthesis of AMS FIR filters, from specification to layout, in a 65nm process technology.

6. Analog/Mixed-Signal Circuit Synthesis Enabled by the Advancements of Circuit Architectures and Machine Learning Algorithms, Shiyu Su, Qiaochu Zhang, Mohsen Hassanpourghadi, Juzheng Liu, Rezwan Rasul, and Mike Shuo-Wei Chen, in IEEE/ACM 27th Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 2022.

Analog mixed-signal (AMS) circuit architecture has evolved towards increased use of digital elements due to technology scaling and demand for higher flexibility and reconfigurability. Meanwhile, the design complexity and cost of AMS circuits has substantially increased due to the necessity of optimizing the circuit sizing, layout, and verification of typically complex AMS circuits. On the other hand, machine learning (ML) algorithms have been under exponential growth over the past decade and actively exploited by the electronic design automation (EDA) community. Here, we identify the opportunities and challenges brought about by these trends and provide an overview of several emerging AMS design methodologies that are enabled by the recent evolution of AMS circuit architectures and machine learning algorithms. Specifically, we focused on using neural-network-based surrogate models to expedite the circuit design parameter search and layout iterations. Lastly, we demonstrate the rapid synthesis of several AMS circuit examples from specification to silicon prototype, with significantly reduced human intervention.

7. Transfer Learning with Bayesian Optimization-Aided Sampling for Efficient AMS Circuit Modeling, Juzheng Liu, Mohsen Hassanpourghadi, Qiaochu Zhang, Shiyu Su, and Mike Shuo-Wei Chen, in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Nov. 2020.

Neural network modeling of the P2M function of a circuit topology enables fast exploration of the design space thanks to its low computation cost. Unfortunately, to build a NN model with sufficient accuracy, a training dataset is needed, incurring SPICE simulations during different design phases. Therefore, it is prudent to train it with a larger dataset in an earlier design phase (e.g., schematic design) but a significantly reduced dataset in a later design phase (e.g., post-layout design or migration to more advanced technology node), as simulation cost increases sharply in later design phases. We demonstrate a transfer learning (TL) technique to reuse the NN model in the early design phase and reduce the dataset size for the later design phase. To ensure that the transfer learning is effective a Bayesian Optimization Aided Sampling method is used to make sure the circuit is sampled under the desired working conditions (e.g., transistor operation region, biasing condition, etc.) in both the early and late design phase. To prove-in the concept, we show that 150X and 17X dataset reductions are possible for a digital-to-analog converter (DAC) in the post-layout design phase and an amplifier in the technology migration phase, respectively.

8. From Specification to Silicon: Towards Analog/Mixed-Signal Design Automation using Surrogate NN Models with Transfer Learning, Juzheng Liu, Shiyu Su, Meghna

Madhusudan, Mohsen Hassanpourghadi, Samuel Saunders, Qiaochu Zhang, Rezwan Rasul, Yaguang Li, Jiang Hu, Arvind Kumar Sharma, Sachin S. Sapatnekar, Ramesh Harjani, Anthony Levi, Sandeep Gupta, and Mike Shuo-Wei Chen, in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Nov. 2021.

With the transfer learning technique, we demonstrate a complete analog mixed-signal circuit design flow from specification to silicon with minimum human-in-the-loop interaction and verify the flow in a 12nm FinFET CMOS process. The flow consists of three key elements: neural network (NN) modeling of the parameterized circuit component, a search algorithm based on NN models to determine its sizing, and layout automation. To reduce the required training data for NN model creation, we utilize transfer learning to improve the NN accuracy from a relatively small amount of post-layout/silicon data. To prove-in the concept, we use a voltage-controlled oscillator (VCO) as a test vehicle and demonstrate that our design methodology can accurately model the circuit and generate designs with a wide range of specifications. We show that circuit sizing based on the transfer learned NN model from silicon measurement data yields the most accurate results.

9. Circuit Connectivity Inspired Neural Network for Analog Mixed-Signal Functional Modeling, Mohsen Hassanpourghadi, Shiyu Su, Rezwan Rasul, Juzheng Liu, Qiaochu Zhang, and Mike Shuo-Wei Chen, in 2021 58th IEEE/ACM Design Automation Conference (DAC), Dec. 2021.

In the aforementioned circuit design automation flow, the NN structure is a conventional fully connected NN. To further reduce the required training dataset's volume and improve the modeling accuracy, we have proposed a circuit-connectivity-inspired ANN (CCI-NN), including multiple sub-ANNs linked according to the actual circuit connections. The prior knowledge of the circuit topology is encoded in the NN structure, which can effectively improve the modeling efficiency. For validation, we have employed CCI-NN to model a three-stage amplifier and a current-steering digital-to-analog converter. For a certain modeling accuracy, the training dataset requirement is shown to be reduced by 3.5x-7.6x.

10. CEPA: CNN-based Early Performance Assertion Scheme for Analog and Mixed-Signal Circuit Simulation, Qiaochu Zhang, Shiyu Su, Juzheng Liu, and Mike Shuo-Wei Chen, in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Nov. 2020.

The design and verification of analog and mixed-signal (AMS) circuits typically involve many time-consuming simulations to qualify target specifications or optimize the design parameters for better performance. The long simulation time significantly slows down the speed of optimization iterations for both human designers and automatic AMS optimizers, inevitably resulting in high design costs and less than optimal designs. In this work, we report on the use of a convolutional neural network (CNN)-based early performance assertion (CEPA) scheme to identify designs with unsatisfactory performance quickly and accurately. Thanks to the feature extraction capability of CNN, CEPA only needs to sample a short duration transient waveform to predict the satisfaction of the target specifications for a certain design that is otherwise obtained by a long transient simulation. In addition, applying the fine-tuning technique to our CEPA scheme can further extend the inference from schematic-level simulation to post-layout simulation with

only a few training samples (i.e., enhancing CEPA's usage with a low training cost). A sample-and-hold circuit and a delta-sigma digital-to-analog converter are presented to prove the effectiveness of the proposed CEPA scheme. With its maximum assertion accuracy of 99%, CEPA reduces the simulation time for assertion by orders of magnitude.

11. A Module-Linking Graph Assisted Hybrid Optimization Framework for Custom Analog and Mixed-Signal Circuit Parameter Synthesis, Mohsen Hassanpourghadi, Rezwan A Rasul, and Mike Shuo-Wei Chen, ACM Transactions on Design Automation of Electronic Systems, Sep. 2021.

Computer-aided design tools can help expedite the design of many wide-range AMS circuits with varied specifications used in modern system-on-chip (SoCs). Traditionally, to accelerate the design process, the AMS system is decomposed into smaller components (called modules) such that the complexity and evaluation of each module is more manageable. However, this decomposition poses an interface problem, where the module's input-output states when combined to construct the AMS system deviate from the expected state, which degrades the expected system performance. In this work, we developed a module-linking-graph (MLG) assisted hybrid parameter search engine with neural networks to overcome these obstacles. The proposed MLG enforced equality of the modules' interfaces during the parameter search process which utilized the neural networks surrogate model of the AMS circuit. We further proposed a hybrid search consisting of global optimization with fast neural network models and a local optimization with accurate SPICE models to expedite the parameter search process while maintaining the accuracy. The effectiveness of the proposed approach was validated using a successive approximation register analog-to-digital converter design in 65-nm CMOS technology. The approach demonstrated the search time improvement by a factor of 5x and 700x compared to the conventional hierarchical and flat design approaches, respectively, with improved search performance.

12. A Novel Multi-objective Optimization Framework for Analog Circuit Optimal Customization, Mutian Zhu, Mohsen Hassanpourghadi, Qiaochu Zhang, Mike Shuo-Wei Chen, A. F. J. Levi, and Sandeep Gupta, to be submitted to International Conference on CAD (ICCAD), 2023.

As described above, AMPSE starts with the netlist and the values of all parameters of a known-good design (KGD), i.e., a design which has been demonstrated in silicon. It uses the KGD netlist as a template, replaces the values of key parameters by variables, and uses a neural network (NN) model to search over the values of these variables to create other versions of the component that *meet the needs of various users* who have *a wide range of specifications*.

In this work we demonstrate an adaptive sampling method (AS) to identify a range of pareto-optimal versions (as illustrated in Fig. 3) of the AMS component under the given run-time budget. This method starts by using Latin hypercube sampling (LHS) over the parameter space to obtain an initial set of design versions followed by simulations to create an initial regression function for the mapping from parameter to metric values. In subsequent iterations, we use a combination of LHS and our greedy sampling approach to create a large number of new design versions. We use the regression function and our *adaptive method* for selecting a small number of promising versions, simulating these

versions, and retraining the regression model. In each iteration, we also update our decision rules to increasingly favor sampling in the promising parts of the parameter space which are identified using all prior simulation results as well as the regression function and its error.

Experimental results demonstrate that our adaptive sampling method identifies pareto optimal design versions that are superior to known methods. Our method is particularly effective for complex AMS blocks, as these require high simulation run-time for estimating the metric values for each circuit version.

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