Changes from last revision

|  |  |  |
| --- | --- | --- |
| Date | User | Edits |
| 12/13/2019 | Mohsen Hassanpourghadi | Version 3.0 |
| 12/23/2019 | Mohsen Hassanpourghadi | Specifications; Schematic and description of testbench; Design examples; |
|  |  |  |

Block descriptions

|  |  |
| --- | --- |
| Design name | VCO Based ADC in TSMC 65nm CMOS |
| The Top-level cell name | ADC\_vcobased\_v1.scs |
| Designer | Mohsen Hassanpourghadi |
| Organization | University of Southern California |

**Overview**

*This ADC receives analog input voltage and transforms it into the phase information. Then, quantizes the phase information.*

**Block Specifications and Compliance**

|  |  |  |  |
| --- | --- | --- | --- |
| Spec Name | Min | Max | Note |
| Sampling rate (MS/s) | 1 | 10000 | The sampling speed is chosen by the AMPSE tool |
| SFDR (dB) | 40 | 70 | Maximum for the 10 bit ADC can be used |
| BW (MHz) | 1 KHz | 500MHz | High bandwidth cannot achieve excellent ENOB |
| SNDR (dB) | 30 | 60 | - |
| Power Consumption (mW) | 1 | 100 | - |
| VDD (Volt) | 1 | 1 | 1 Volt VDD |

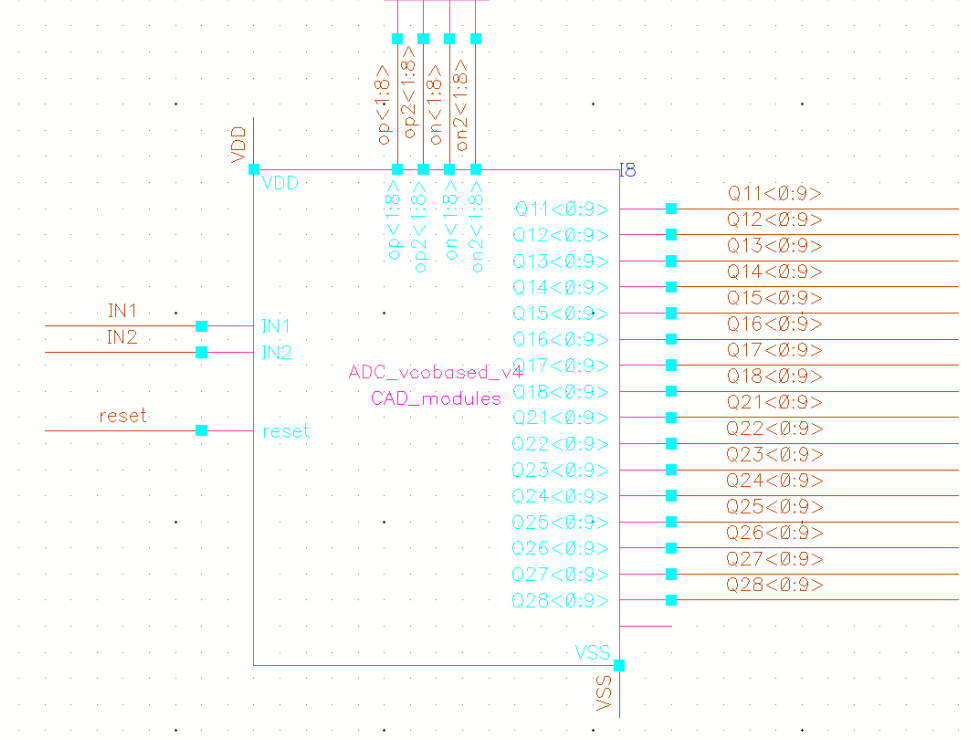
**Block diagram**

The block diagram representation of the design is as follows:



Figure 1: Architecture of VCO-based ADC with AMPSE

**Signal list**



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Signal Pins | Direction  (I/O) | Type  (supply, ground, analog current, analog voltage, digital voltage) | Max Voltage  (core, IO or max voltage) | Specification |
| VDD | I | Supply | Core | Power Supply, 1.0 V |
| VSS | I | Ground | Core | Ground |
| IN1, IN2 | I | Analog voltage | Core | Differential Analog Input |
| reset | I | Digital voltage | Core | Reset |
| Qij<0:9> | O | Analog voltage | Core | Outputs |
| op,op2,on,on2 | T | Analog voltage | Core | Test points |

**Design Hierarchy**

The tabular description below corresponds to design hierarchy.

|  |  |  |  |
| --- | --- | --- | --- |
| Category | Cell Name | Description | Figure |
| ADC\_vcobased\_v4 | VCO\_analogin\_cmlbuffer\_v2 | Top level | Figure. A1 |
| VCO\_Dtype2\_65 | Pseudo differential VCO | Figure. A2 |
| counter\_verilogA | VerilogA counter | Code A3 |
| diff2sing\_v1 | Differential to single ended | Figure. A4 |
| VCO\_Dtype2\_65 | VCO\_type2\_65 | VCO single output | Figure. A5 |
| Testbench | test\_VCO65\_v4 | Testbench for VCO based ADC | Figure. A6 |

**Test Bench**

|  |  |
| --- | --- |
| Cell Name | Note |
| test\_VCO65\_v4 | Transient simulation for   1. locking time evaluation; 2. SNDR; 3. SFDR; 4. … |
|  |  |

**Appendix**

Figure. A1

A screenshot of a computer

Description automatically generated

Figure. A2

A picture containing building

Description automatically generated

Code. A3:

// VerilogA for CAD\_modules, counter\_verilogA, veriloga

`include "constants.vams"

`include "disciplines.vams"

`define SIZE 10

module counter\_verilogA(out, clk);

inout clk;

electrical clk;

output [`SIZE-1 :0] out;

electrical [`SIZE-1 :0] out;

parameter integer setval = 0 from [0:(1<<`SIZE)-1];

parameter real vtrans\_clk = 0.6;

parameter real vtol = 0; // signal tolerance on the clk

parameter real ttol = 0; // time tolerance on the clk

parameter real vhigh = 1.2;

parameter real vlow = 0;

parameter real tdel = 30p;

parameter real trise = 30p;

parameter real tfall = 30p;

parameter integer up = 0 from [0:1]; //0=increasing 1=decreasing

parameter integer stepsize = 3;

integer outval;

analog begin

@(initial\_step("static","ac")) outval = setval;

@(cross(V(clk)-vtrans\_clk,1,vtol,ttol))

outval = (outval +(+up- !up)\*stepsize)%(1<<`SIZE);

generate j (`SIZE-1 , 0) begin

V(out[j]) <+ transition (!!(outval &(1<<j))\*vhigh+!(outval&(1<<j))\*vlow,tdel,trise,tfall);

end

end

endmodule

Figure A.4:

A close up of a red light at night

Description automatically generated

Figure A.5:

A screenshot of a computer

Description automatically generated

Figure A.6:

A picture containing light, outdoor

Description automatically generated

AMPSE Modules descriptions

|  |  |  |
| --- | --- | --- |
| Module Name | Class name in Netlist\_Database.py | Class name in AMPSE\_Graph.py |
| VCO | VCOSpice | VCO |
| Input Buffer | INBUF2Spice | INBUF2 |

*All the regression files are in /regfiles*

VCO:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| parameters | min | max | step | Description |
| wnnn(nm) | 200 | 1200 | 10 | Width of NMOS |
| fnnn | 2 | 20 | 1 | # of fingers of NMOS |
| wppp(nm) | 200 | 1200 | 10 | Width of PMOS |
| fppp | 2 | 20 | 1 | # of fingers of PMOS |
|  |  |  |  |  |

|  |  |
| --- | --- |
| Metrics | Description |
| power | Power consumption (W) |
| vcm | Input Common mode (V) |
| vfs | Input full scale (V) |
| noise | Noise of the VCO (Hz2) |
| freq[1:8] | Interpolated frequency at linspace(-vfs, +vfs,8)+vcm (Hz) |

Input Buffer:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| parameters | min | max | step | Description |
| multi | 1 | 20 | 1 | Buffer multiplier |
| fing\_in | 1 | 50 | 1 | # of fingers of Input NMOS |
| l\_ttt (nm) | 60 | 400n | 10 | Length of tail NMOS |
| fing\_ttt | 1 | 50 | 1 | # of Fingers of tail NMOS |
| VCM (V) | 0.55 | 0.9 | 0.01 | VCM of buffer |
| wppp | 200n | 1200n | 10n | Width of PMOS in VCO |
| fppp | 2 | 20 | 1 | # of fingers of PMOS in VCO |

|  |  |
| --- | --- |
| Metrics | Description |
| power | Power consumption (W) |
| gain | Differential Gain of buffer (V/V) |
| bandwidth | Buffers bandwidth (Hz) |
| outvcm | Output VCM (V) |
| AVCM | Common mode rejection ratio (dB) |
| kickback | Kickback effect from the VCO (dB) |
| irn | Input referred noise (uV2) |
| out[1:4] | Interpolated output voltage at (-0.3, +0.3,4)+VCM |



Figure 1-AMPSE Modular Linking Graph