Changes from last revision

|  |  |  |
| --- | --- | --- |
| Date | User | Edits |
| 12/28/2019 | Soumya Mahapatra | Specifications; Schematic and description of testbench; Design examples; |

Subsystem or block descriptions

|  |  |
| --- | --- |
| Design name | Clock Divider in TSMC 65nm CMOS |
| The Top-level cell name | TB\_CK\_Divider.scs |
| Designer | Shiyu Su |
| Tested & Documented By | Soumya Mahapatra |
| Organization | University of Southern California |

**Overview**

*This circuit block is a clock divide by 2 circuit which produces both the in-phase and quadrature-phase clock signals with half the frequency of that of the applied input differential sinusoidal signal. It comprises of two D-latches realized using current steering logic which contain a differential pair and a regenerative pair. These D-latches are connected in negative feedback in a master-slave configuration which results in a D-flip flop producing clock signals of half-frequency.*

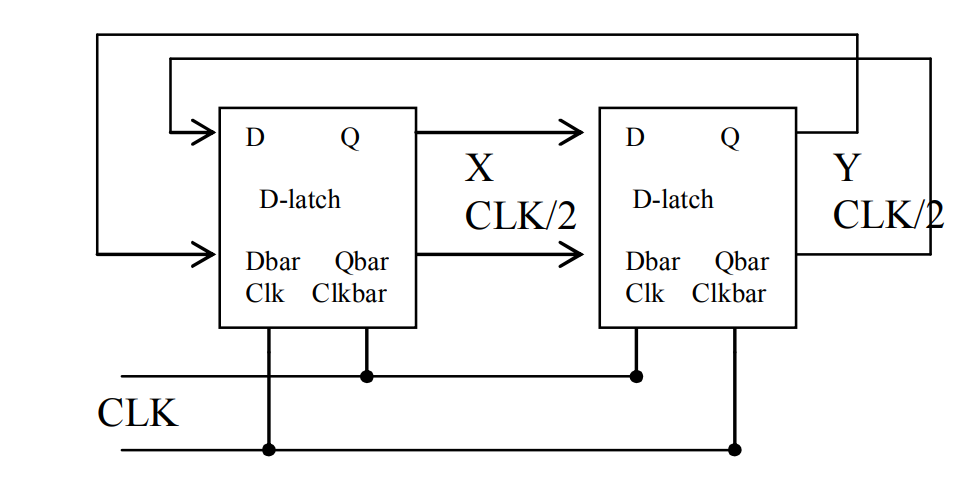
*This clock divider is intended to produce a 6 GHz output clock signal for driving subsequent blocks employing current mode logic (CML).*

**Block Specifications and Compliance**

|  |  |  |  |
| --- | --- | --- | --- |
| Spec Name | Min | Max | Note |
| Output Frequency (GHz) | 5.99 | 6.01 | Input Frequency = 12 GHz |
| Output Clock High Voltage Level (mV) | 600 | 900 | \ |
| Output Clock Low Voltage Level (mV) | 200 | 300 | \ |
| Power Consumption (mW) | 1 | 3 | \ |

**Block diagram**

The block diagram representation of the design is as follows:



**Figure 1:** Architecture of the Clock Divider with AMPSE (X & Y denote the I & Q clock signals)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Main analog modules | Regression models | | | |
| Clock Divider | model\_ckdiv65.json | reg\_ ckdiv65h5 | scX\_ ckdiv65.pkl | scY\_ ckdiv65.pkl |

***Signal list***

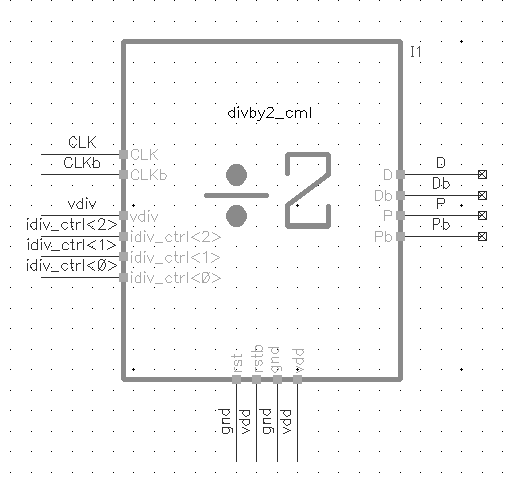


Figure 2: Symbol of the Top-Level of the Clock Divider

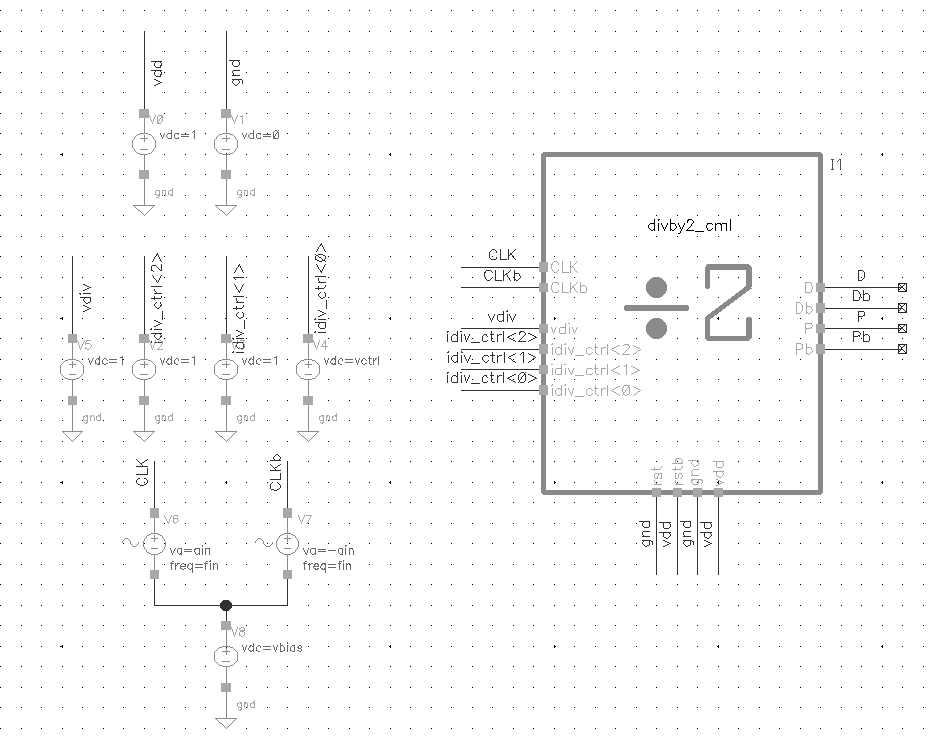
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Signal Pins | Direction  (I/O) | Type  (supply, ground, analog current, analog voltage, digital voltage) | Max Voltage  (core, IO or max voltage) | Specification |
| vdd | I | Supply | Core | Power Supply, 1.0 V |
| gnd | I | Ground | Core | Ground |
| CLK, CLKb | I | Analog voltage | Core | Differential Input Clock (sine, 12 GHz) |
| idiv\_ctrl<2:0> | I | Digital voltage | Core | Bias Tail Current Control Bits |
| rst,rstb | I | Digital voltage | Core | Reset – active low signal for clock divider |
| D,Db | O | Analog voltage | Core | I- phase differential clock o/p |
| P,Pb | O | Analog voltage | Core | Q- phase differential clock o/p |
| vdiv | I | Analog voltage | Core | Setting Biasing Voltage of Tail Current |

**Design Hierarchy**

The tabular description below corresponds to design hierarchy:

|  |  |  |  |
| --- | --- | --- | --- |
| Category | Cell Name | Description | Figure |
| Clock\_Divider | divby2\_cml\_latch | CML D-latch | Figure. A1 |
| Clock\_Divider | divby2\_cml\_tail | Tail Current Source of D-latch | Figure. A2 |

**Test Bench**

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**Figure 3:** The Test Bench Used for the top-level Clock Divider

|  |  |  |
| --- | --- | --- |
| Cell Name | Note | |
| test\_CK65 | Transient simulation for   1. Output Clock Frequency 2. Output Clock High Value 3. Output Clock Low Value 4. Input Amplitude Requirement | DC simulation for:   1. Power Consumption |

**Simulations (test\_** **CK65):**

|  |  |  |  |
| --- | --- | --- | --- |
| Conditions/parameters | Values | Conditions/parameters | Values |
| Process corner | TT | idiv\_ctrl<2:0> | 111 |
| Temperature(°C) | 27 | W\_input\_diff\_pair (μm) | 1 |
| vdd(V) | 1 | W\_intermediate\_tail (μm) | 4 |
| Input amplitude(V) | 100m | W\_tail (μm) | 2.5 |
| Input common mode voltage | 500m | Load Resistor (ohms) | 560 |
| vdiv | 1 | rst | 0 |

After running several simulations in ADEXL, we obtain the dataset which was used for training the regressor. After that, we get the candidate values of the parameters and the list of the expected metrics per module in order to achieve the required specs and their given constraints. Three different design cases are explored and the results obtained are tabulated below:

**Case 1: Fosc = 6 GHz**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Clock Divider Parameters** | | **Clock Divider Metrics** | | |
| W\_ip\_diff (μm) | 0.92 | **Overall Achieved Metrics** | **Generated using AMPSE** | **Rechecked using Cadence Virtuoso®** |
| W\_int\_tail (μm) | 4.32 | Power Consumption (W) | 3.56m | 3.204m |
| W\_tail (μm) | 2.8 | Output Amplitude High(V) | 867.3m | 848.1m |
| Res (ohms) | 568 | Output Amplitude Low (V) | 223.1m | 206.7m |
| LSB of I\_ctrl | 1 | Output Frequency (GHz) | 5.95 | 6.133 |

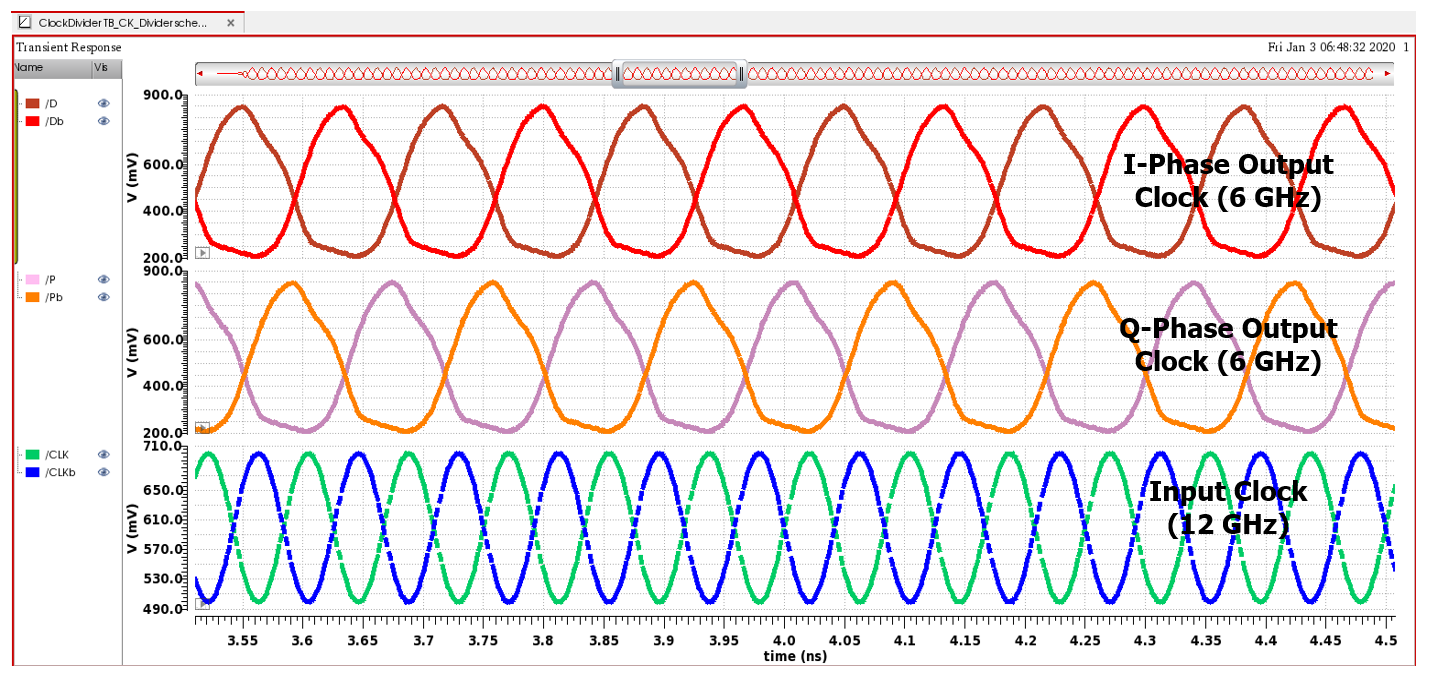
**Case 2: Fosc = 9 GHz**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Clock Divider Parameters** | | **Clock Divider Metrics** | | |
| W\_ip\_diff (μm) | 1.15 | **Overall Achieved Metrics** | **Generated using AMPSE** | **Rechecked using Cadence Virtuoso®** |
| W\_int\_tail (μm) | 2.93 | Power Consumption (W) | 3.73m | 3.145m |
| W\_tail (μm) | 2 | Output Amplitude High(V) | 852.1m | 836.3m |
| Res (ohms) | 487 | Output Amplitude Low (V) | 373.3m | 329.8m |
| LSB of I\_ctrl | 1 | Output Frequency (GHz) | 8.91 | 9.05 |

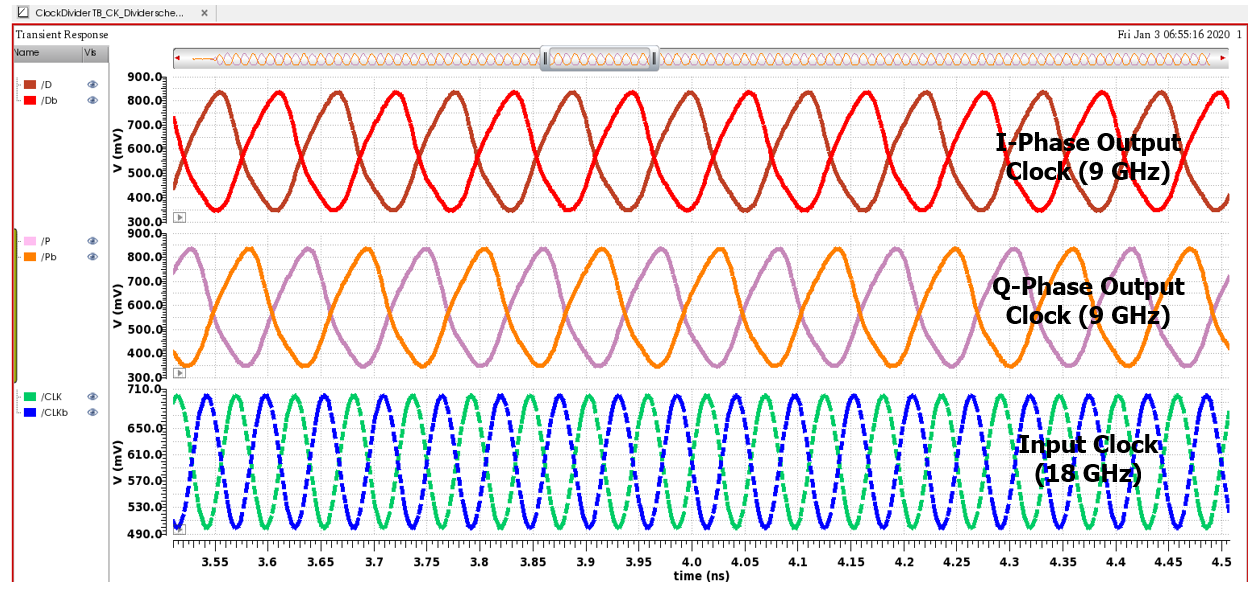
**Case 3: Fosc = 12 GHz**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Clock Divider Parameters** | | **Clock Divider Metrics** | | |
| W\_ip\_diff (μm) | 0.53 | **Overall Achieved Metrics** | **Generated using AMPSE** | **Rechecked using Cadence Virtuoso®** |
| W\_int\_tail (μm) | 3.5 | Power Consumption (W) | 3.183m | 2.789m |
| W\_tail (μm) | 2 | Output Amplitude High(V) | 839.2m | 824.5m |
| Res (ohms) | 604 | Output Amplitude Low (V) | 294.1m | 269.4m |
| LSB of I\_ctrl | 1 | Output Frequency (GHz) | 12.16 | 12.0 |

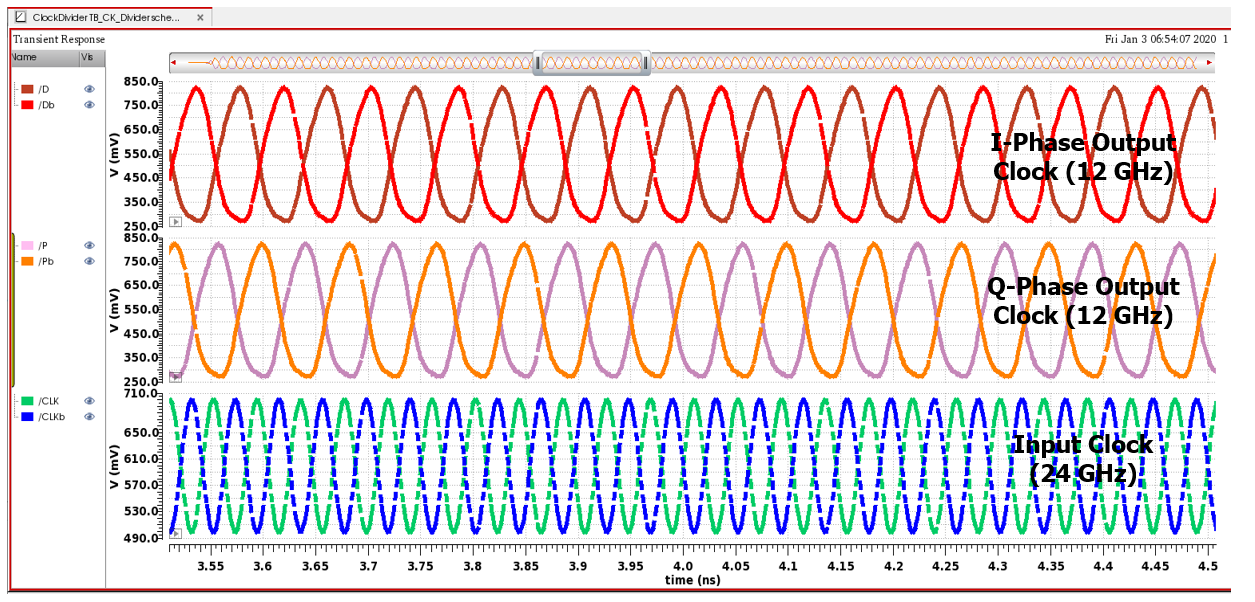
The resulted metrics out from Cadence seems to give a quite matched result from the AMPSE.



**Figure 4:** Tranisent Simulation for the top-level Clock Divider @ Fosc = 6 GHz

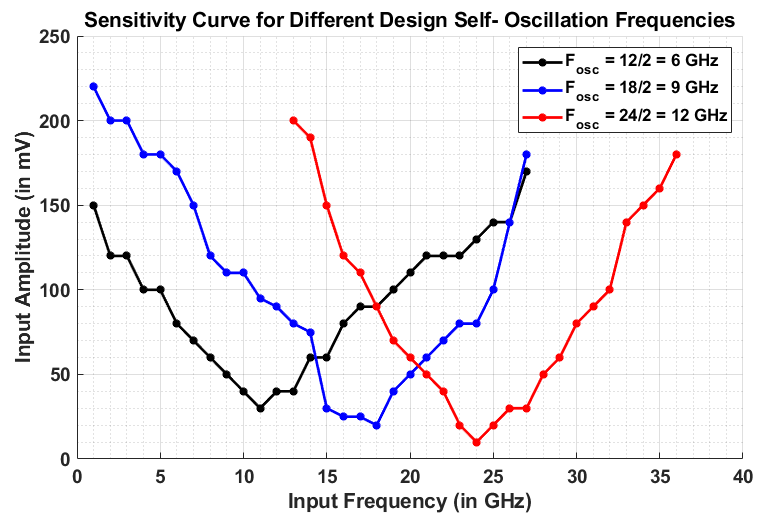


**Figure 5:** Tranisent Simulation for the top-level Clock Divider @ Fosc = 9 GHz

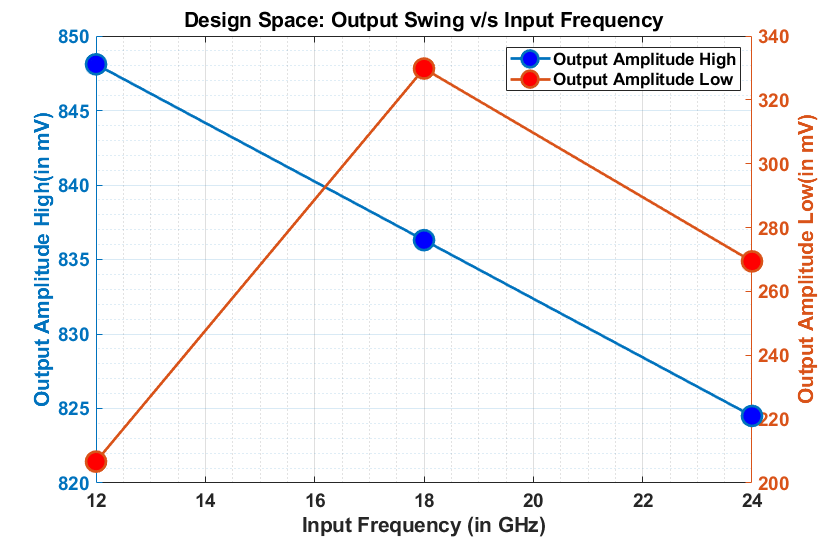


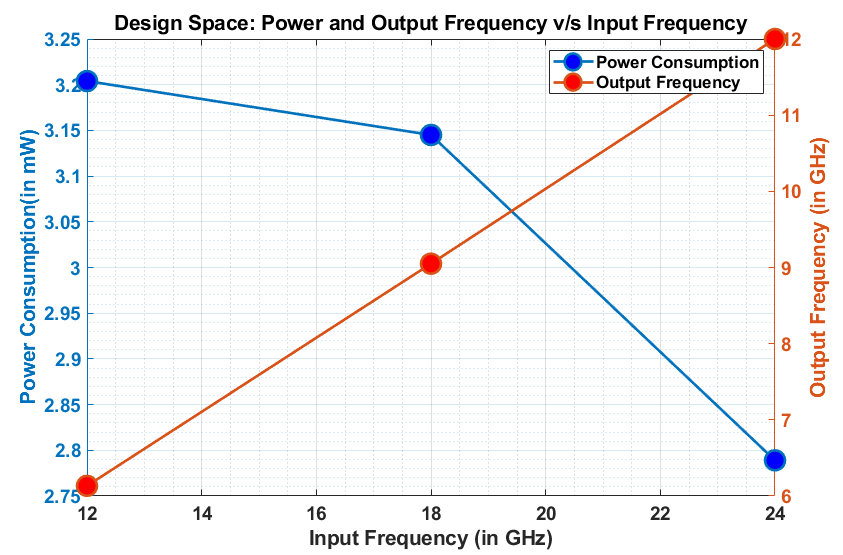
**Figure 6:** Tranisent Simulation for the top-level Clock Divider @ Fosc = 12 GHz

For plotting the input amplitude v/s input frequency characteristics of the clock divider circuit, parametric simulation was carried out to determine the minimum value of input amplitude which is required to make the clock divider work reliably to produce a half-frequency clock at the output.

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**Figure 7:** Sensitivity Curve of the Clock Divider for different self-oscillation frequency

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**Figure 7:** Design Space Exploration and achieved specs for different cases

**TIME-EFFICIENCY OF AMPSE FOR THIS DESIGN:**

(1) **2175 points** for coarse search of different design self-oscillation frequencies (~ 12 secs each)

(2) **4950 points** for fine optimization of specs around the desired design frequency (~ 30 secs each)

Total design time for exhaustive SPICE simulations = 2175\*0.2 + 4950\*0.5 min = **2910 min** (for 1 design)

Total design time for AMPSE (regressor + AMPSE graphs) = 1 + 0.2 min = **1.2 min** (for 1 design)

**AMPSE is around 2400x more time-efficient than regular parametric-sweep based optimization!**

**Appendix**

The schematics of the two modules used within the Clock Divider are shown below

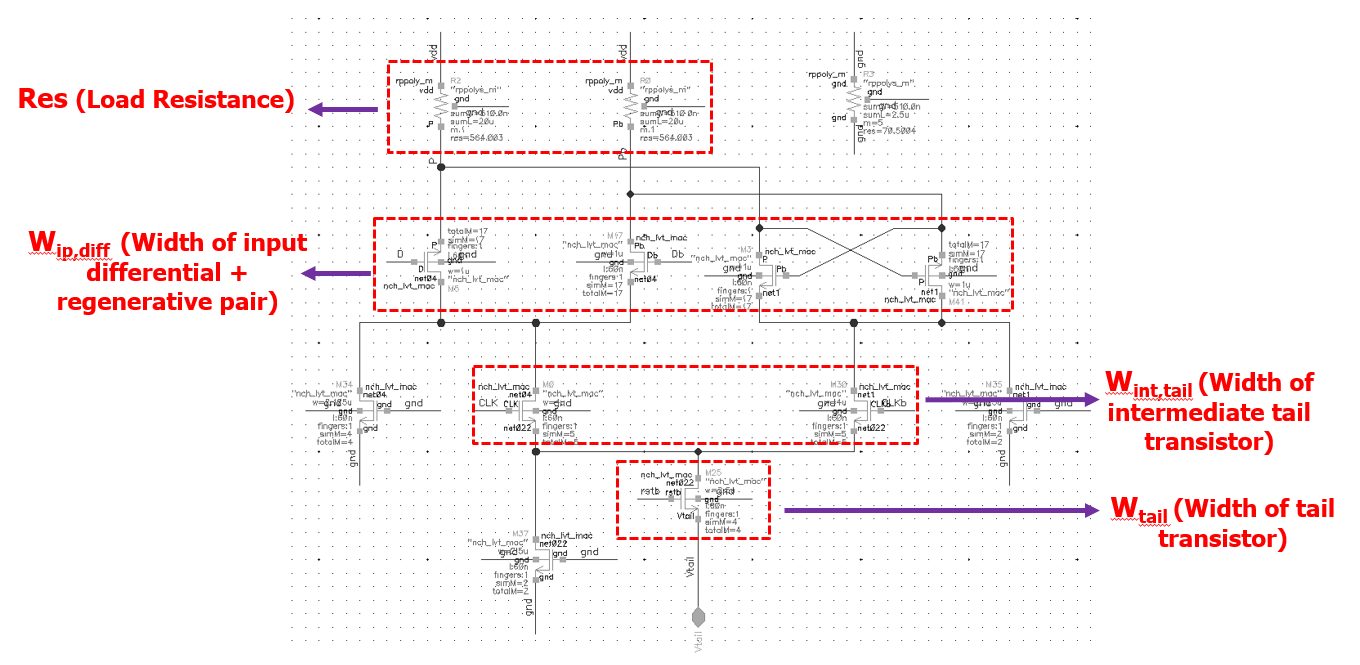


Figure A.1: The Circuit Schematic of the D-latch

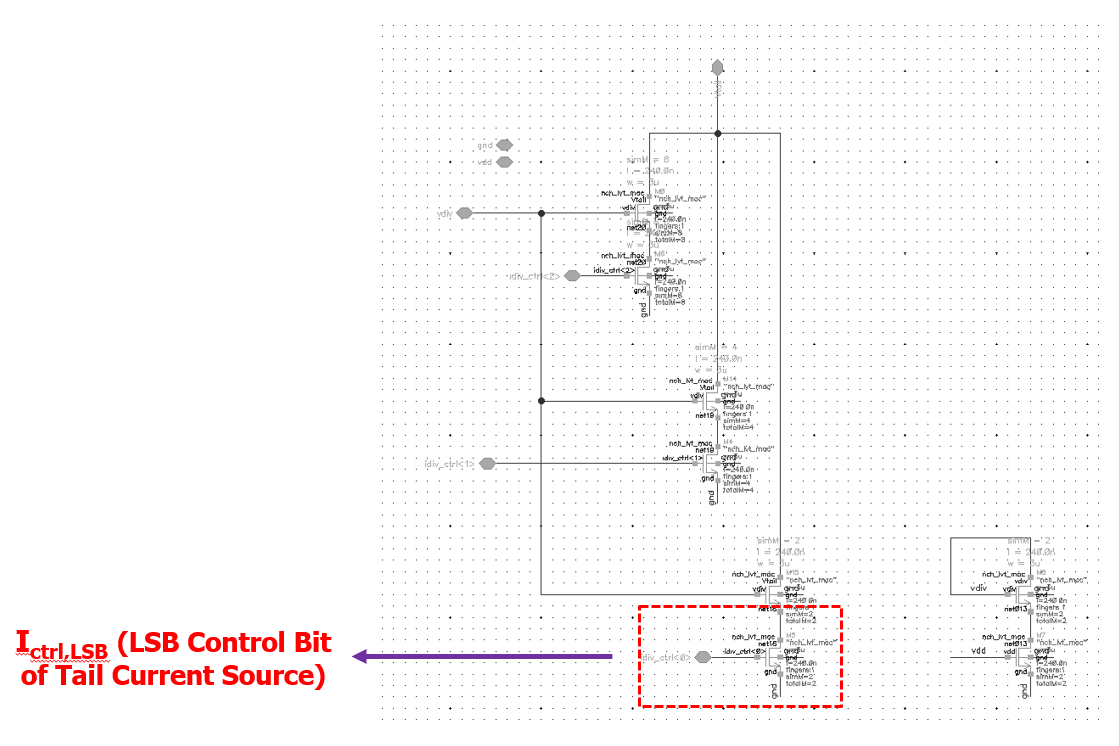


Figure A.2: The Circuit Schematic of the Tail Current Source

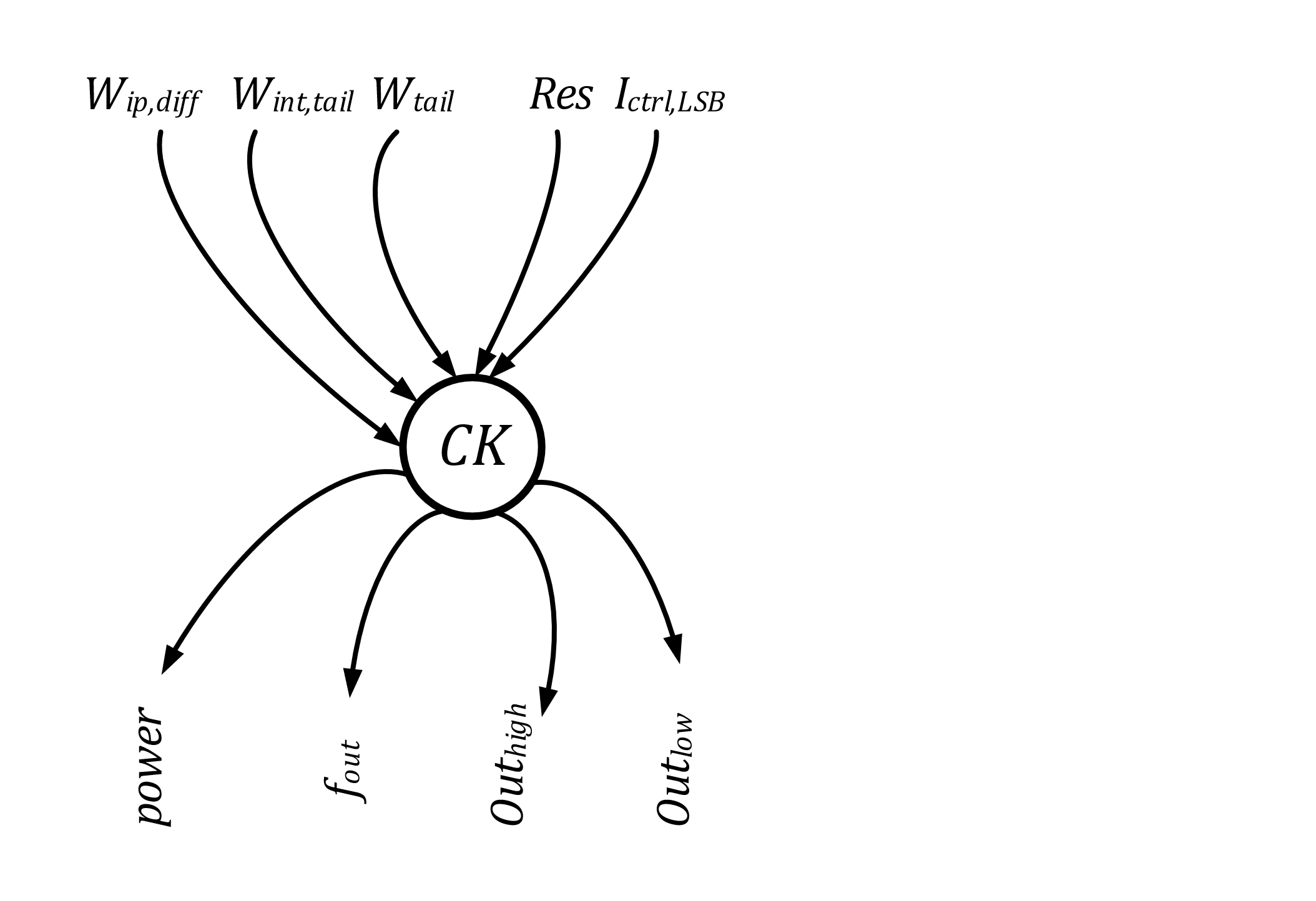
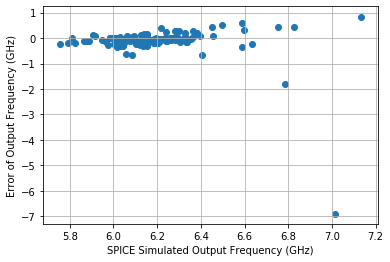
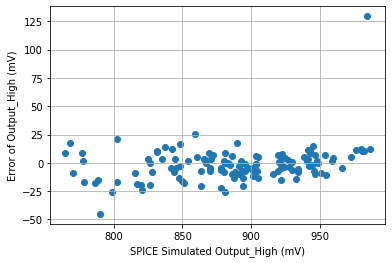
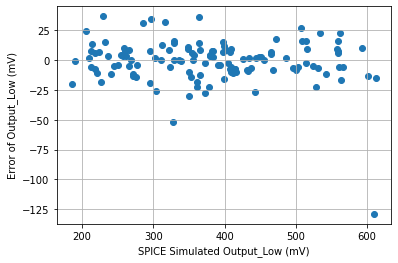


Figure A.3: The Graph Used to Model the Block

**The error range of the Clock Divider Model:**







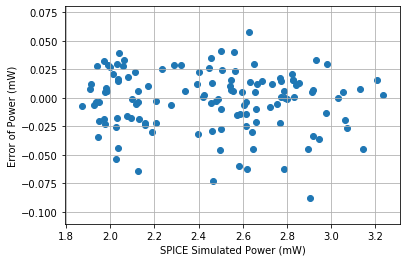


Figure A.4: The Error in Different Metrics of the Clock Divider