Changes from last revision

|  |  |  |
| --- | --- | --- |
| Date | User | Edits |
| 12/27/2019 | Qiaochu Zhang | Specifications; Schematic and description of testbench; Design examples; |
|  |  |  |

Subsystem or block descriptions

|  |  |
| --- | --- |
| Design name | Digital to Time Converter (DTC) in TSMC 65nm CMOS |
| The Top-level cell name | tb\_DTC\_PNinj\_final.scs |
| Designer | Qiaochu Zhang |
| Organization | University of Southern California |

**Overview**

*A DTC receives digital codes and converts to delay (analog signal). Current mode logic buffers and switched capacitors are used in the circuit.*

**Block Specifications and Compliance**

|  |  |  |  |
| --- | --- | --- | --- |
| Spec Name | Min | Max | Note |
| Sampling rate (MS/s) | 1 | 100 |  |
| Gain (ps) | 100 | 200 | Delay when all caps are attached |
| Offset (ps) | 100 | 200 | Delay when no cap is attached |
| Rise Time (ps) | 50 | 100 | - |
| VDD (Volt) | 1 | 1 | 1 Volt VDD |

**Block diagram**

The block diagram representation of the design is as follows:

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Figure 1: Architecture of DTC with AMPSE

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Main analog modules | Regression models | | | |
| DTC 1st stage | model\_tb\_DTC\_PNinj.json | reg\_tb\_DTC\_PNinj.h5 | scX\_tb\_DTC\_PNinj.pkl | scY\_tb\_DTC\_PNinj.pkl |
| DTC 2nd stage | model\_tb\_DTC\_2nd\_stage.json | reg\_tb\_DTC\_2nd\_stage.h5 | scX\_tb\_DTC\_2nd\_stage.pkl | scY\_tb\_DTC\_2nd\_stage.pkl |

***Signal list***

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Figure 2: Symbol of the Top-Level of the DTC

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Signal Pins | Direction  (I/O) | Type  (supply, ground, analog current, analog voltage, digital voltage) | Max Voltage  (core, IO or max voltage) | Specification |
| DTC\_vdd | I | Supply | Core | Power Supply, 1.0 V |
| DTC\_gnd | I | Ground | Core | Ground |
| REF\_inj\_in+,  REF\_inj\_in- | I | Analog voltage | Core | Analog input signal |
| REF\_inj\_out+,  REF\_inj\_out- | O | Analog voltage | Core | Analog output signal |
| dtc\_gain\_m<5:0>  dtc\_gain<33:0> | I | Digital voltage | Core | DTC gain tuning bits |
| dtc\_offset\_m<5:0>  dtc\_offset\_m\_2<4:0> | I | Digital voltage | Core | DTC offset tuning bits |
| phi\_df\_frac\_retimed<63:0> | I | Digital voltage | Core | DTC input code |
| PN\_CML\_bias\_300u\_pside | I | Analog current | Core | CML bias current |
| PN\_inj\_bias\_100u\_pside | I | Analog current | Core | CML bias current |
| PN\_CML\_bias\_pside\_small | I | Analog current | Core | CML bias current |

**Design Hierarchy**

The tabular description below corresponds to design hierarchy:

|  |  |  |  |
| --- | --- | --- | --- |
| Category | Cell Name | Description | Figure |
| DTC | DTC1 | Digital controlled delay cell | Figure. A1 |
| DTC2 | CML buffer | Figure. A2 |

**Test Bench**

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Figure 3: The Test Bench Used for the top-level DTC

|  |  |  |
| --- | --- | --- |
| Cell Name | Note | |
| tb\_DTC\_PNinj | Transient simulation for   1. DTC gain 2. DTC offset of 1st stage 3. Rise time of 1st stage | ------ |
| tb\_DTC\_2nd\_stage | Transient simulation for   1. DTC offset of 2nd stage 2. Rise time of 2nd stage | ------ |

**Simulations (tb\_DTC\_PNinj\_final):**

|  |  |  |  |
| --- | --- | --- | --- |
| Conditions/parameters | Values | Conditions/parameters | Values |
| Process corner | TT | dtc\_gain\_m | 32 |
| Temperature(°C) | 27 | PN\_CML\_bias\_pside\_small | 30u |
| VDD(V) | 1 | PN\_CML\_bias\_300u\_pside | 240u |
| phi\_df\_frac\_retimed | 50 | PN\_inj\_bias\_100u\_pside | 100u |
| fref | 40M | dtc\_offset | 32 |
| dtc\_gain | 32 |  |  |

After running the different modules regressors and building the graph of the whole block, we get the candidate values of the parameters and the list of the expected metrics per module in order to achieve the required specs and their given constraints.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| AMPSE Design Example - 1 | | | | | |
| Parameters | | Metrics from AMPSE | | Metrics from SPICE | |
| nf\_dif | 16 | DTC Gain (ps) | 169 | DTC Gain (ps) | 176 |
| res | 2777 | DTC Offset (ps) | 177.6 | DTC Offset (ps) | 193.7 |
| nf\_load | 13 | Rise Time (ps) | 50 | Rise Time (ps) | 89 |
| nf\_cap | 18 |  |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| AMPSE Design Example - 2 | | | | | |
| Parameters | | Metrics from AMPSE | | Metrics from SPICE | |
| nf\_dif | 18 | DTC Gain (ps) | 140 | DTC Gain (ps) | 138.2 |
| res | 2227 | DTC Offset (ps) | 165 | DTC Offset (ps) | 172.5 |
| nf\_load | 18 | Rise Time (ps) | 64 | Rise Time (ps) | 87.3 |
| nf\_cap | 18 |  |  |  |  |

**Appendix**

The schematics of the two modules used within the are shown below

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Figure A.1: The Circuit Schematic of the DTC 1st stage

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Figure A.2: The Circuit Schematic of DTC 2nd stage

AMPSE Modules descriptions

|  |  |  |
| --- | --- | --- |
| Module Name | Class name in Netlist\_Database.py | Class name in AMPSE\_Graph.py |
| DTC1 | DTC1\_spice | DTC1 |
| DTC2 | DTC2\_spice | DTC2 |

*All the regression files are in /regfiles*

DTC1:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameters | min | max | step | Description |
| nf\_cap | 10 | 21 | 1 | Number of fingers of capacitors |
| nf\_load | 10 | 21 | 1 | Number of fingers of load transistor |
| res | 2000 | 4000 | 100 | Resistance |
| nf\_dif | 10 | 21 | 1 | Number of fingers of differential pair |

|  |  |
| --- | --- |
| Metrics | Description |
| delay | Delay when all caps are attached |
| delay0 | Delay when no cap is attached |
| trf\_full | Rise time when all caps are attached |
| trf\_zero | Rise time when no cap is attached |

DTC2:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameters | min | max | step | Description |
| trf | 100ps | 300ps | 10ps | Rise time of the signal from the previous stage |
| nf\_load | 10 | 21 | 1 | Number of fingers of load transistor |
| res | 2000 | 4000 | 100 | Resistance |
| nf\_dif | 10 | 21 | 1 | Number of fingers of differential pair |

|  |  |
| --- | --- |
| Metrics | Description |
| delay | Delay when all caps are attached |
| delay0 | Delay when no cap is attached |
| trf\_full | Rise time when all caps are attached |
| trf\_zero | Rise time when no cap is attached |

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Figure A.3: The Graph Used to Model the Two Modules Together