**Module:** Pseudo-differential VCO type1 (used in VCO-based ADC)

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**Module Description:** Pseudo-differential VCO utilizes five resistor based cross-coupled inverters and ring-oscillator based topology. The architecture has 10 different nodes positive and negative side and one input.

**Top Cell Name:** VCO\_Dtype1\_65

**Technology:** TSMC 65nm CMOS

**PINS:**

|  |  |
| --- | --- |
| Pin Lists |  |
| VDD | Supply Voltage |
| VSS | ground |
| Vbias | Input voltage node |
| on<1:5> | Five output from the negative side VCO |
| op<1:5> | Five output from the positive side VCO |

**Schematic Netlists:** VCO5\_type1.scs

**Schematic figures:**

A picture containing wall, hanging, photo, white

Description generated with very high confidence

A screenshot of a cell phone

Description generated with very high confidence

**Testbenches:** VCO5\_type1\_test.scs

**Parameters:**

|  |  |
| --- | --- |
| Parameters | Symbols |
| NMOS transistors width (m) |  |
| NMOS transistors # of fingers |  |
| PMOS transistors width (m) |  |
| PMOS transistors # of fingers |  |
| Resistors (ohm) |  |

**Metrics:**

|  |  |
| --- | --- |
| Metrics | Symbols |
| Maximum input range at pin vbias (V) | Input |
| Power Consumption (mW) | Power |
| Minimum VCO frequency (Hz) | Fmin |
| Maximum VCO frequency (Hz) | Fmax |

**Neural Network Model:**

**The H5 file:** reg\_vco65.h5

**The Json File:** model\_vco65.json

**The Input Normalization File:** scX\_vco65.pkl

**The Output Standardization File:** scY\_vco65.pkl

**The input characterization range of the Model:**

|  |  |
| --- | --- |
| Design parameters |  |
| Symbols | Characterization Range |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
| VDD | 1 V |

**The estimation error over the metrics:**







