



in collaboration with



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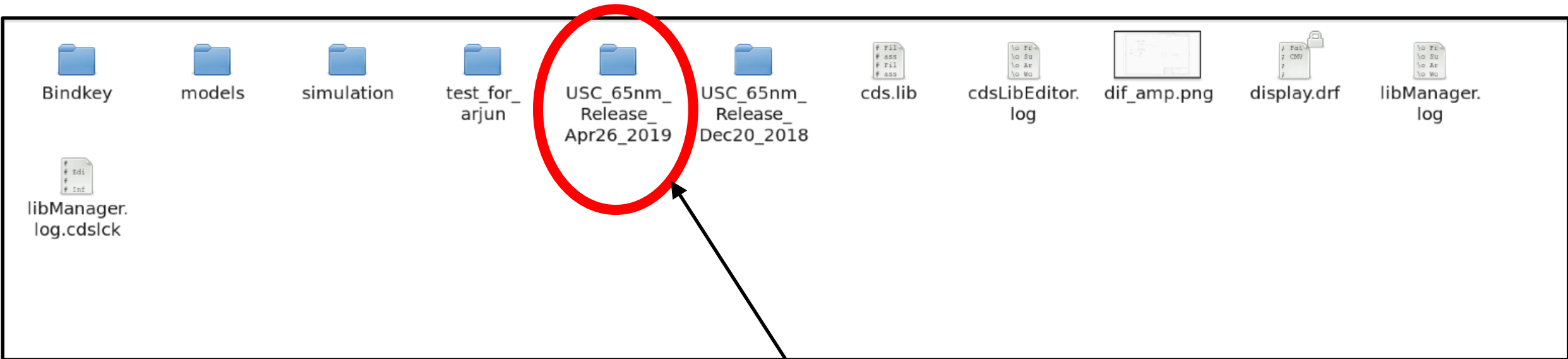
Simulating KGD: GF65nm SAR ADC

IMPORTANT NOTES REGARDING RULE FILES FOR THE LAYOUT:

- The runset, DRC, LVS, PEX Calibre files are not included in the repository.
- It is left to the details of the user's installation of Calibre to set these up.
- There is nothing design specific to get Calibre DRC and PEX going.

Simulating KGD: GF65nm SAR ADC

1) Copy the library to /workarea_GF55



Testbenches may be found in April 2019 release folder.



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https://github.com/USCPOSH/AMS_KGD/tree/master/ADC/SAR_ADC/GF65LPe

Simulating KGD: GF65nm SAR ADC

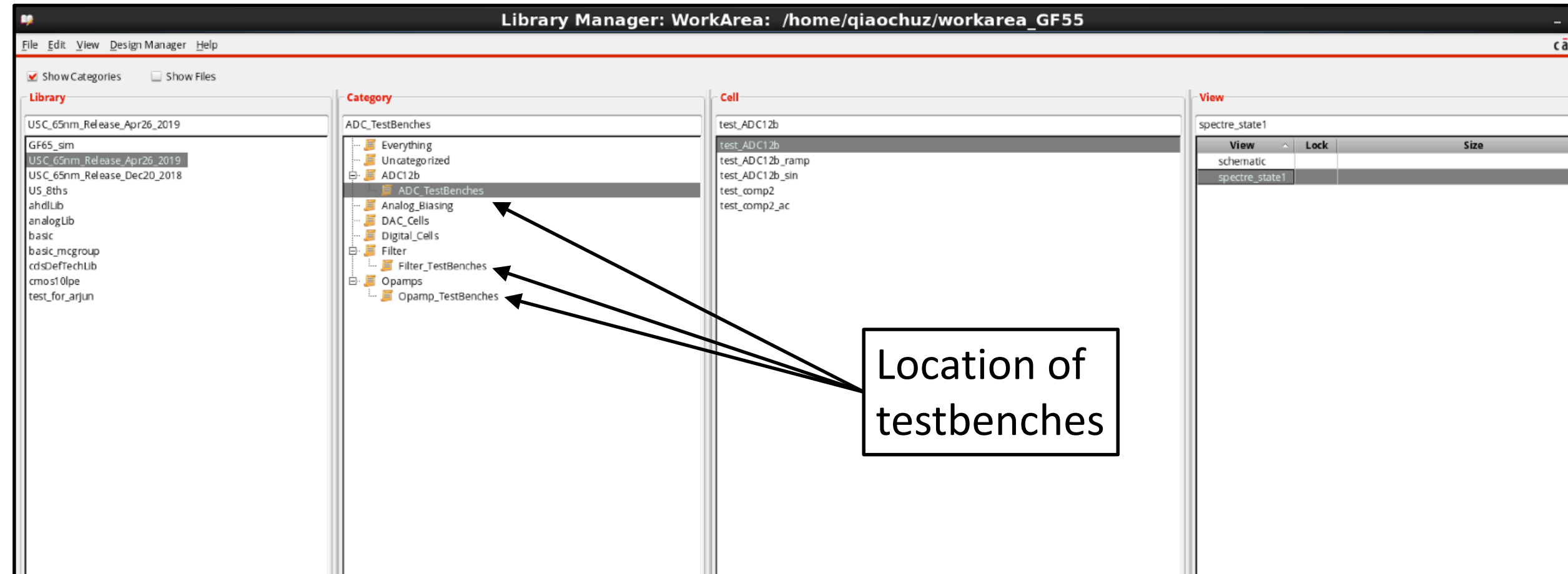
2) Add the library to cadence search path

- Open cds.lib in /workarea_GF55
- Add the line shown below

```
cds.lib x
1 # File Created by  at Sat Mar 23 16:31:07 2019
2 # assisted by CdsLibEditor
3 # File Created by Praveen Sharma at Fri Oct 12 18:14:38 2012
4 # assisted by CdsLibEditor
5
6 # Standard libs
7 DEFINE analogLib /home/Cadence/IC616/tools.lnx86/dfII/etc/cdslib/artist/analogLib
8 DEFINE basic /home/Cadence/IC616/tools.lnx86/dfII/etc/cdslib/basic
9 DEFINE basic_mcgroup /shares/commonIP/basic_mcgroup
10 DEFINE US_8ths /home/Cadence/IC616/tools.lnx86/dfII/etc/cdslib/sheets/US_8ths
11 DEFINE ahdlLib /home/Cadence/IC616/tools.lnx86/dfII/samples/artist/ahdlLib
12 DEFINE USC_65nm_Release_Dec20_2018 /home/qiaochuz/workarea_GF55/USC_65nm_Release_Dec20_2018
13 DEFINE USC_65nm_Release_Apr26_2019 /home/qiaochuz/workarea_GF55/USC_65nm_Release_Apr26_2019
14
```

Simulating KGD: GF65nm SAR ADC

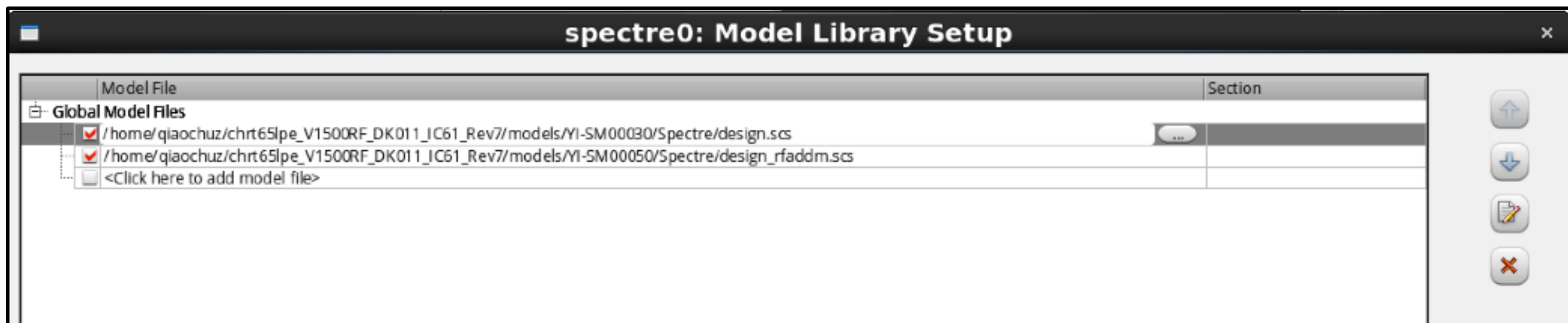
3) Open design and find testbenches under corresponding categories



Simulating KGD: GF65nm SAR ADC

4) Change the path of model file

- Open ADE L
- Click Setup -> Model Libraries
- Find the location of your model file



5) Click simulation button!