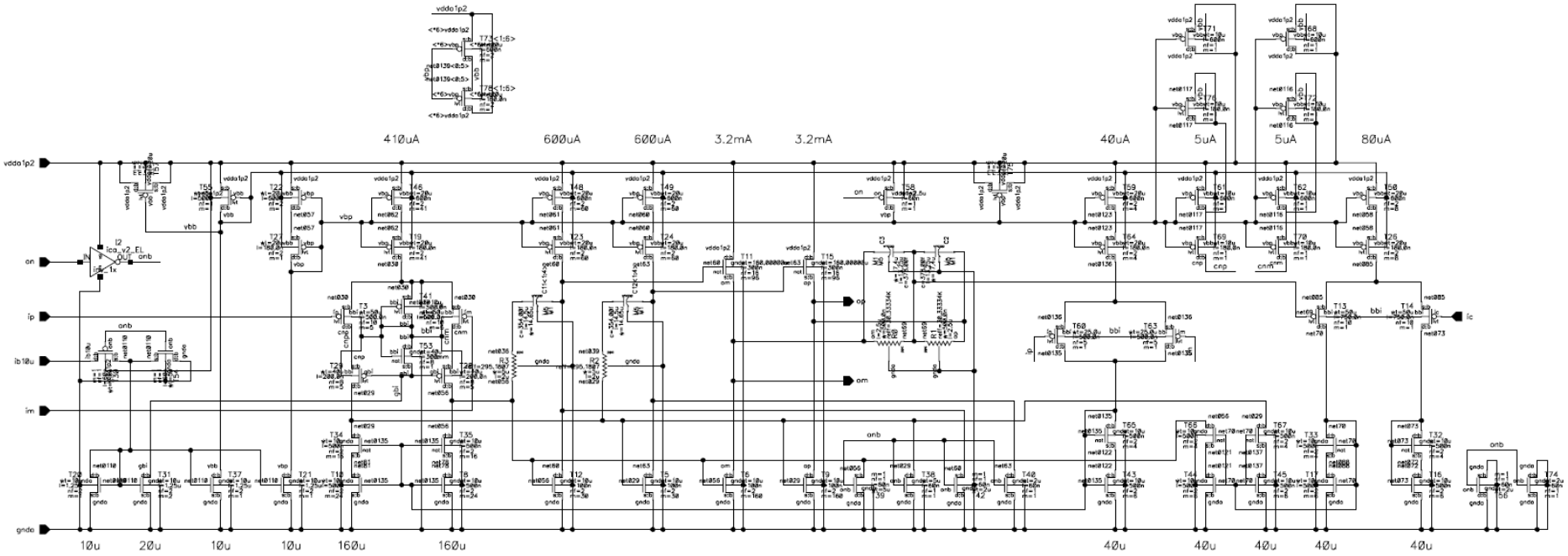
GF65 to PTM65 Conversion

Description

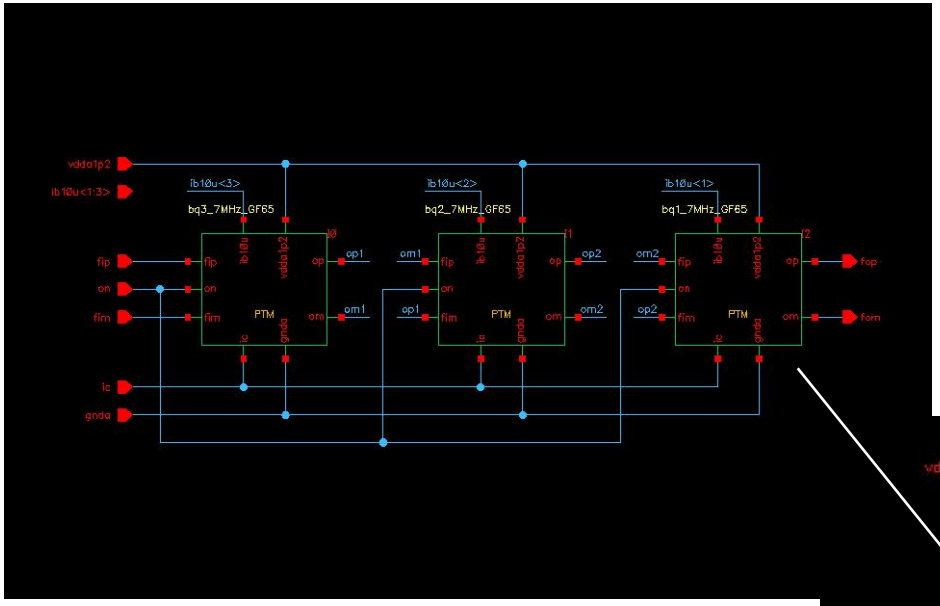
- 10-bit linearity OPAMP and 6-pole triple-biquad 7-MHz Anti-Alias Filter (AAFilter) designed, simulated at 39 PVT corners, fabricated and measured in GF65 process.
- Problem: Transition above to PTM65
- PTM65 is bulk mosfet, bsim4v5 model decks, ***with no binning*** => Multifinger device layout parasitics and strain-related device performance variation is *NOT* captured.
  - Has only one nfet and one pfet device model
  - Has no process corner other than typical
    - Limited utility for translation to practical, fabricable designs with acceptable yield in foundry process
  - No resistor or capacitor devices. GF65 has resistors with different tempco and different capacitor models (MOM, MIM, Varactor).
    - Ideal passives used in PTM design.
  - GF65 design uses regular Vt NFET, thin-oxide native NFET and Low-Vt PFET
- Solution Approach
  - To preserve OPAMP architecture, we “create” a thin-oxide native-nfet PTM model which is a reduced Vt version of existing PTM65 model.
  - We preserve geometry parameters of each transistor in the schematic as we migrate from GF65 to PTM65 for estimated extrinsic device parasitics.
  - We maintain ***multiplicity*** of devices in PTM65 OPAMP schematic as in GF65 schematic.
  - Wiring capacitance and resistance is not included or estimated in GF65 or PTM65 schematic.
  - Created PTM65 device library in Cadence for schematic capture and simulation.

OPAMP Schematic designed in GF65

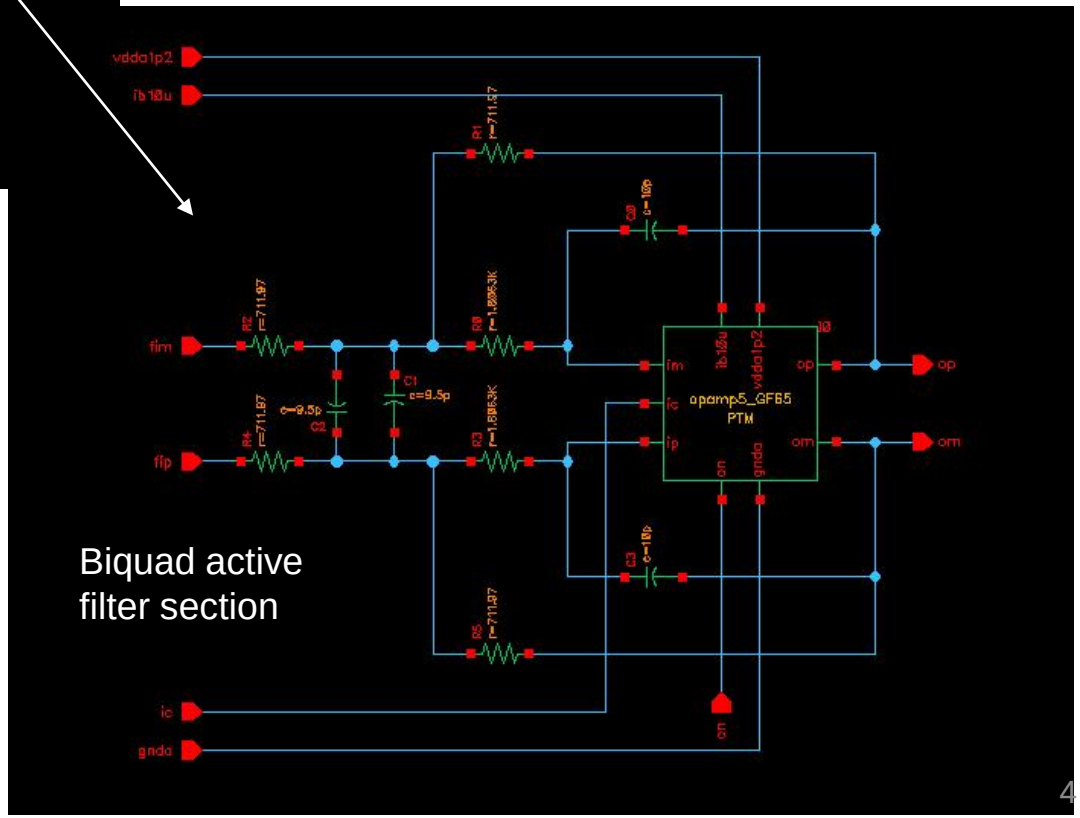
- Multi Stage, differential input, differential output OPAMP with common-mode feedback control circuit designed and validated in GF65 process technology: Design comprises of 87 transistors including subcircuits.



OPAMP-based, differential input, differential output, Six-pole Triple-Biquad 7MHz AAFilter



Six-pole triple-biquad 7MHz AAFilter



Biquad active filter section

Comparison Summary at Nominal PVT corner

Opamp	GF65, GF65Bias	PTM65+PTM65 Native Fets
Open-loop gain (dB)	79.24	76.12
Fu (MHz)	150	99.18
Phase Margin (degrees)	53.08	50.14
6-pole AA-filter		
DC gain (dB)	-0.005631	-0.004844
f_3dB (MHz)	7.079	7.244
f_50dB (MHz)	18.47	18.33
IM3 from DFT Plot (dB)	62.08	66.86
Estimated Linearity in Bits from IM3	10.52	11.31
Peaking in Ac-plot (dB)	0.0056	0.61
Integrated Output(Input) Noise Voltage 10Hz to 100MHz (uVrms)	144.20	167.10
Avg. Power (mW)	30.14	29.45

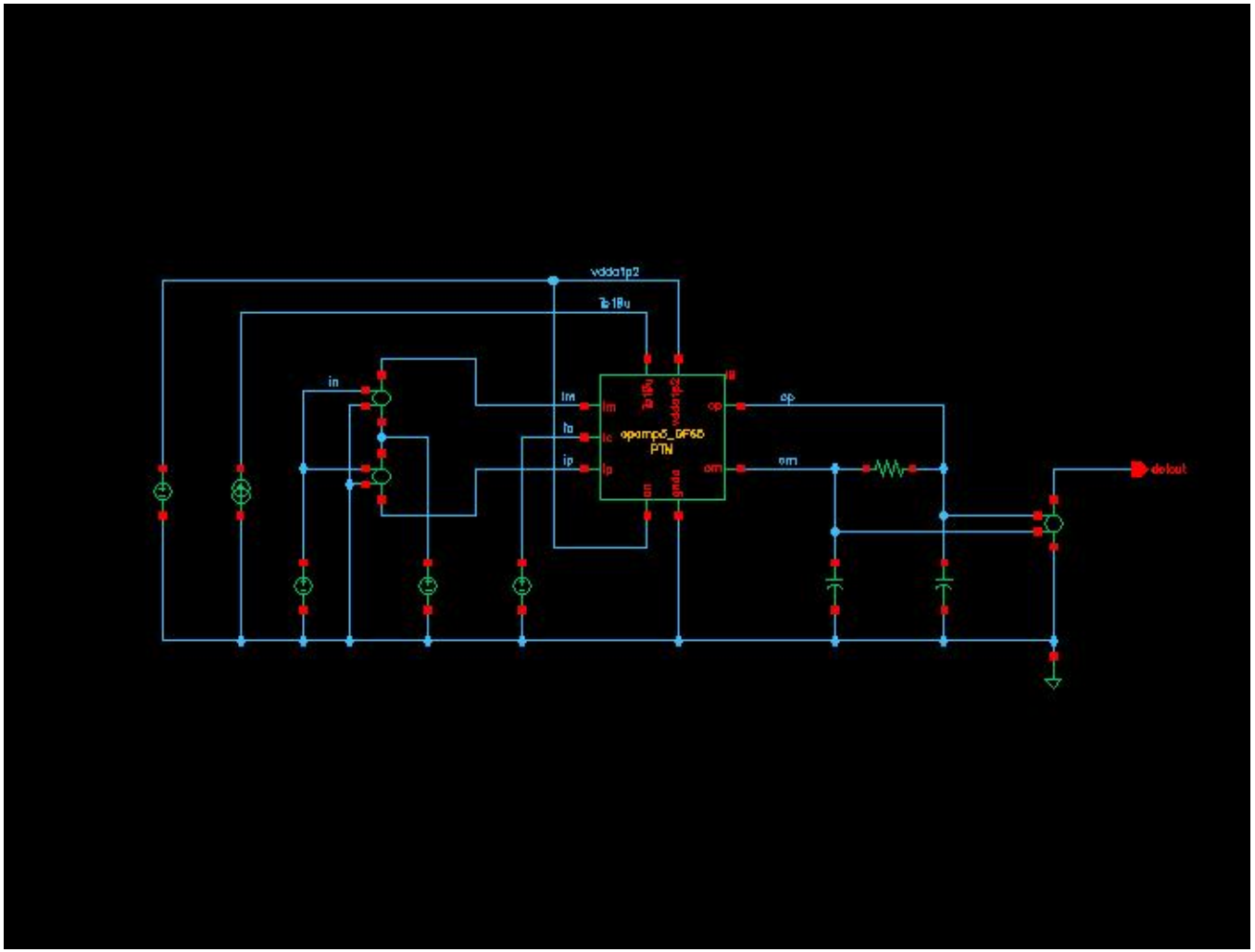
- PTM65 transistors have higher FET model diffusion capacitance parameters than GF65
  - Reduced open-loop bandwidth and phase-margin
  - Increased peaking in closed-loop response (0.61 dB vs. 0.0056dB for GF65 AAFilter)
- PTM65 transistors have lower rds => reduced open-loop gain
- Available PTM65 transistors have lower threshold voltage than GF65 => slightly more headroom for schematic that uses GF65 devices.
  - Third harmonic IM suppression in two-tone simulation is 66.86 dB (11.31 bits) for PTM65 AA-Filter instead of 62.08 dB (10.52 bits) for GF65 AAFilter.

Why are the results so close without redesign ?

- Closed-loop design with design objectives determined by passive devices has reduced sensitivity to open-loop component variations
- Open-loop design will be more exposed (e.g. traditional digital circuits)
- Increasingly constrained process design “box” with decreasing feature size
    - Transistor models across foundries (including PTM) will be reasonably close for the same device (transistor) architecture. Differences are likely to be within 20%, which is large enough for make or break (put at risk) high-volume IC designs
        - IC Designs are usually platform designs of an entire product family to amortize mask and fab costs across wafer-programmable parts.
            - Increases design cost
            - Decreases power efficiency to make some other product design metric or vice-versa, which is why the 20% is important in general.
    - At the end of Moore’s law, the ultimate differentiation will be via *super-custom silicon* – *co-design of transistor and circuit*, which could be seen as a logical extension of POSH.
        - Co-design is about adjusting required transistor small-signal or dc-parameters to achieve a desired analog result without revolutionary device architecture change. E.g. High rds “Analog” transistor for super, power-efficient analog front-end

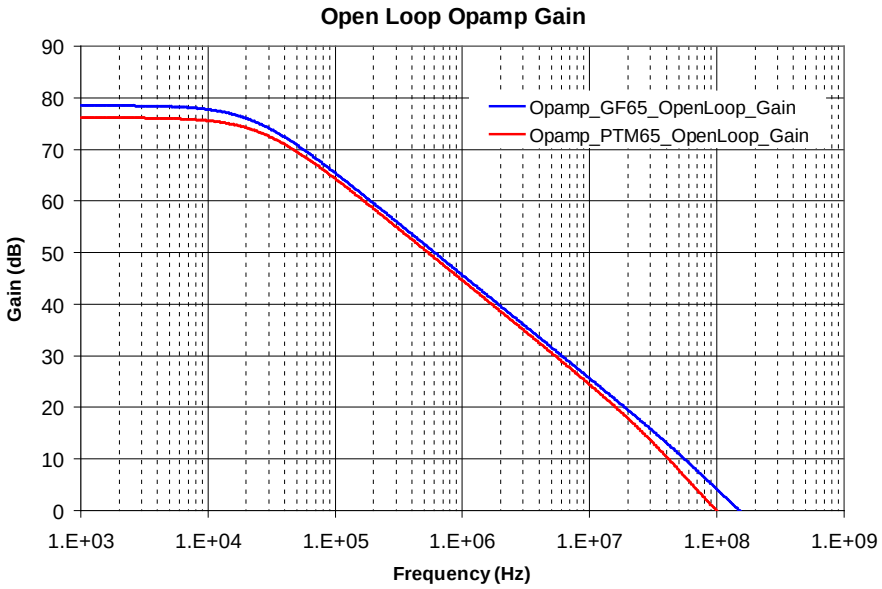
- PTM is missing the variety of devices available in modern foundries, which are required to make analog (and to a lesser extent, digital) designs successful in digital, fine feature-size processes.
    - Recommend funding revamped, up-to-date PTM models.
    - Comprehend newer devices such as vertically stacked, gate-all-around (GAA) nano-sheet transistors (sub 3-nm process technology)

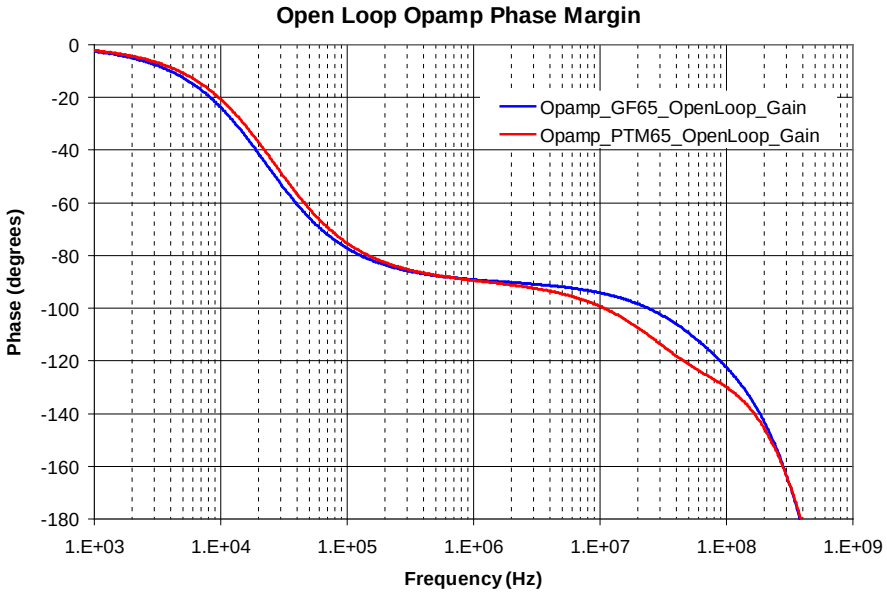
OPAMP Test Schematic



- Open-loop OPAMP Test Schematic
- Differential Input, Differential Output
- Ideal Input Bias Current in Test Schematic

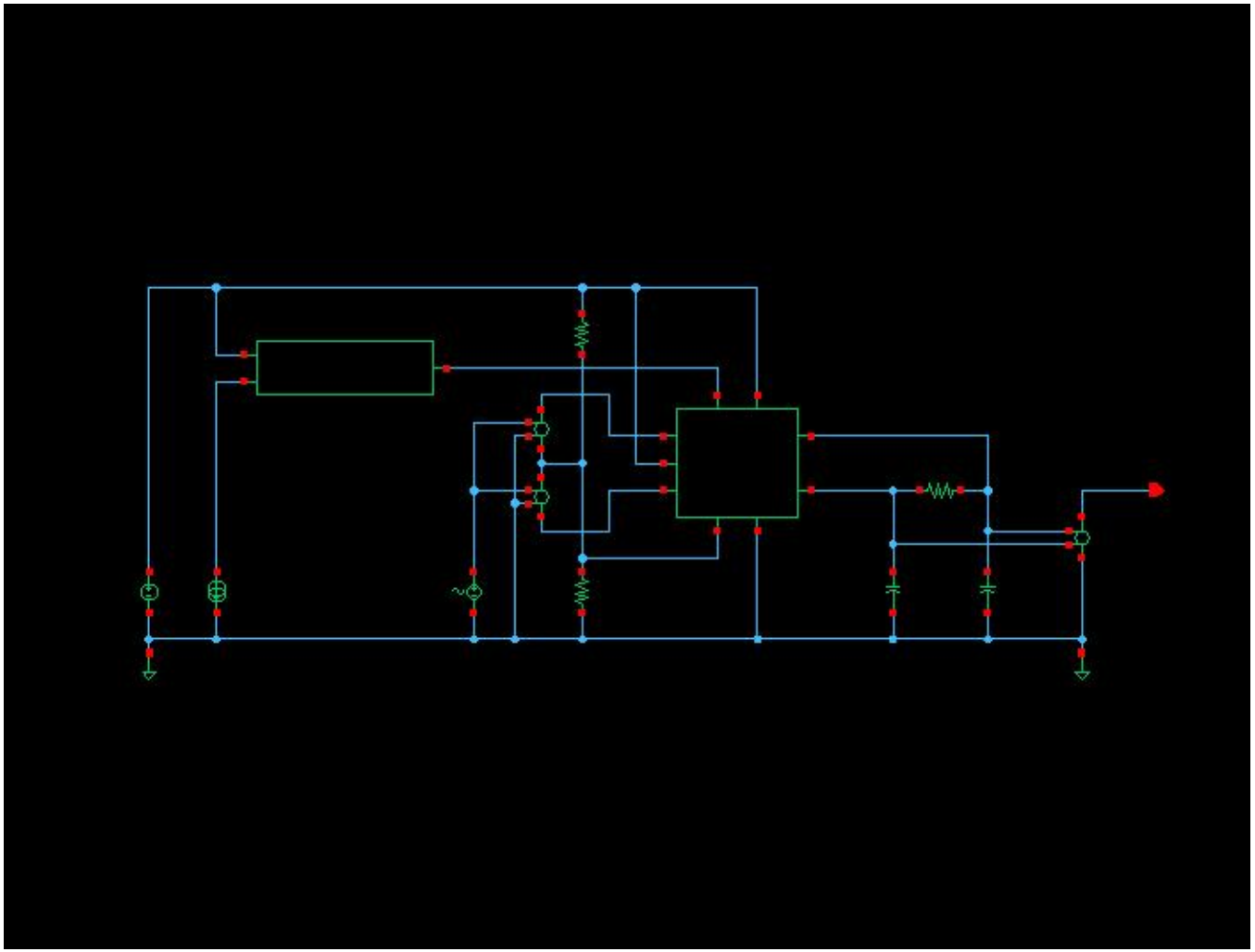
Comparison of GF65 and PTM65 Open Loop OPAMP Gain and Phase Margin





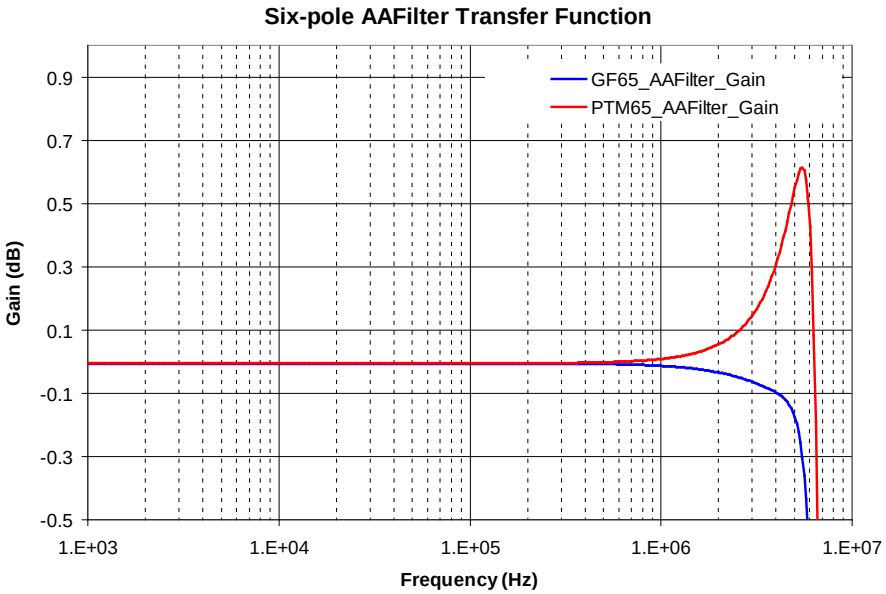
- Nominal schematic (with estimated device parasitics) simulation conditions: TT, 1.2V, 27C
  - Device parasitics correspond to geometry parameters of each MOSFET in schematic.
  - No estimated wiring or layout-related parasitics in schematic.
  - Reduced Phase-Margin of PTM65 OPAMP (red curve) results in peaking in closed-loop AAFIlter frequency response.

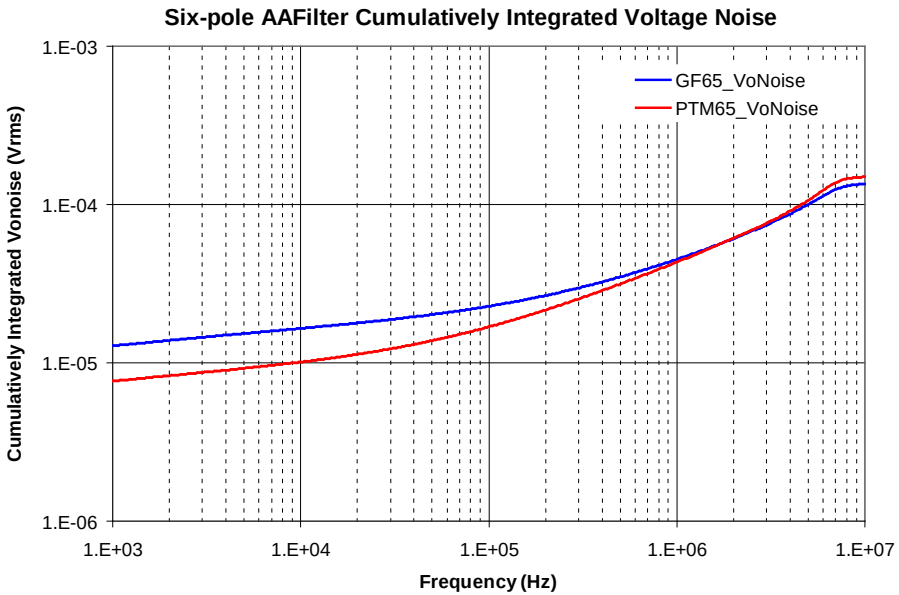
Six-Pole, 7MHz, >10-bit Linearity AAFilter



- Six-pole 7-MHz triple-biquad AAFilter Test Schematic
- Differential Input, Differential Output
- Current-mirror supplies bias current to OPAMPs in AAFilter

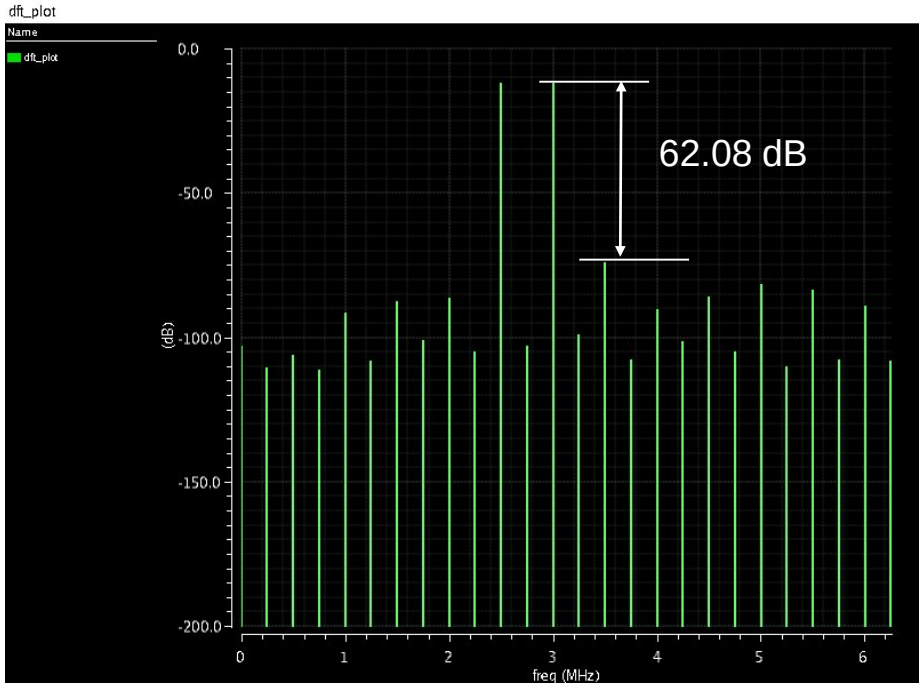
Comparison of Transfer Functions



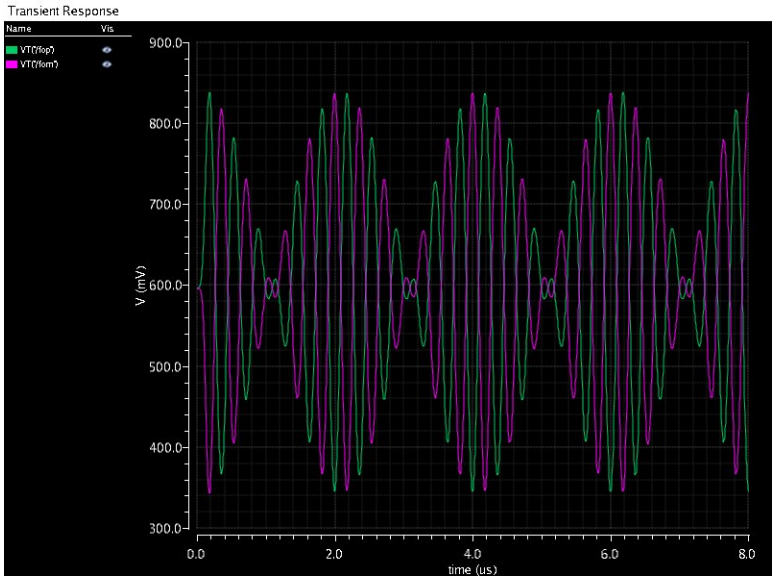


Reduced Phase Margin of PTM65 OPAMP causes peaking in closed-loop response

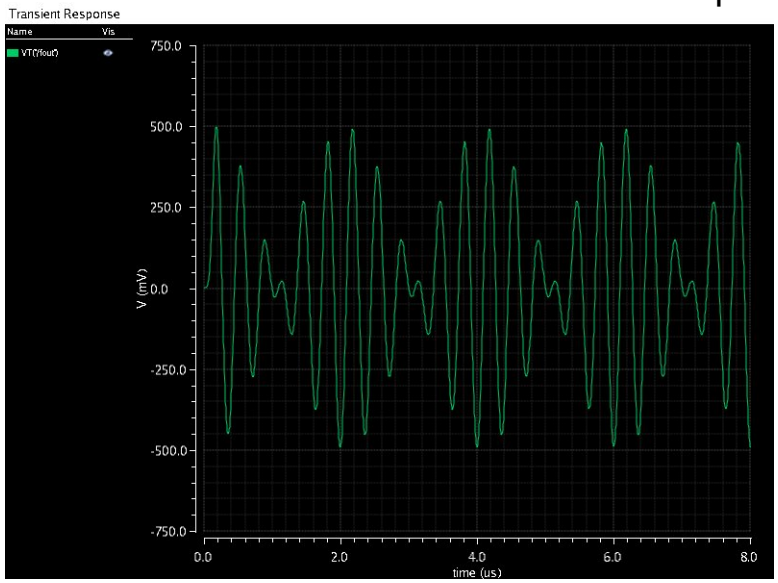
Simulated Two-Tone Test of GF65 AAFilter Schematic



DFT of Two-Tone Test, with 2.5 and 3 MHz sine-wave Input signals, each having 250mV amplitude.

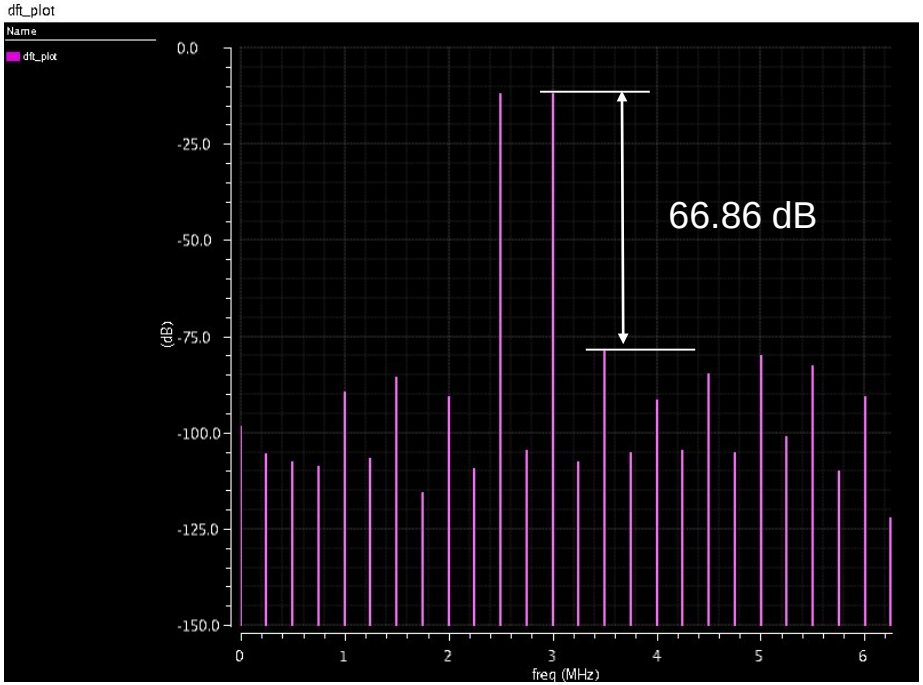


Transient Waveform at Plus and Minus Outputs



Differential Output transient waveform

Simulated Two-Tone Test of PTM65 AAFilter Schematic



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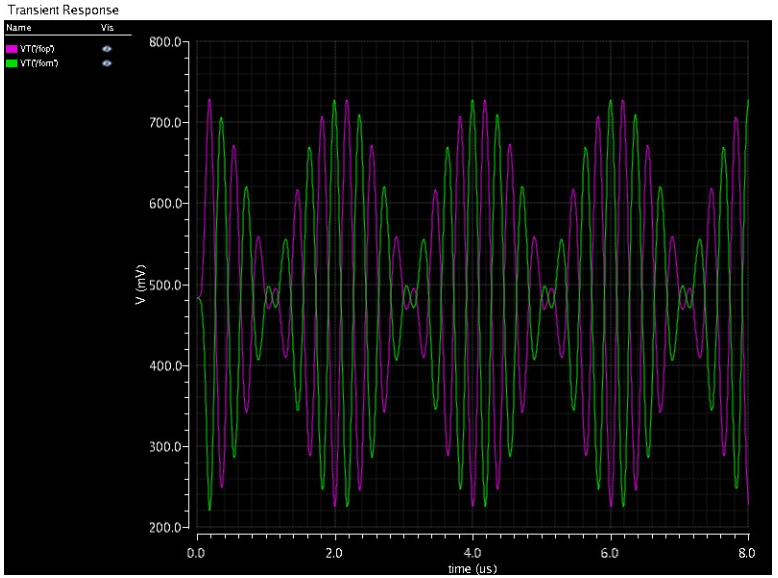
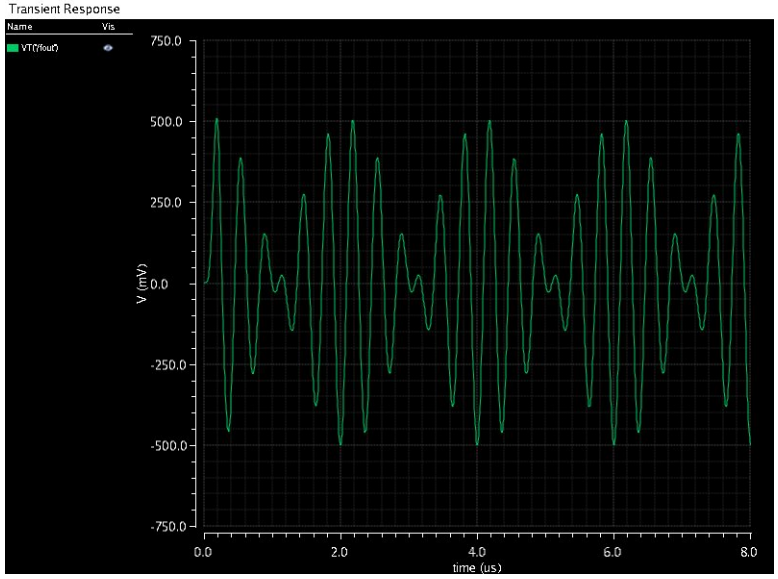


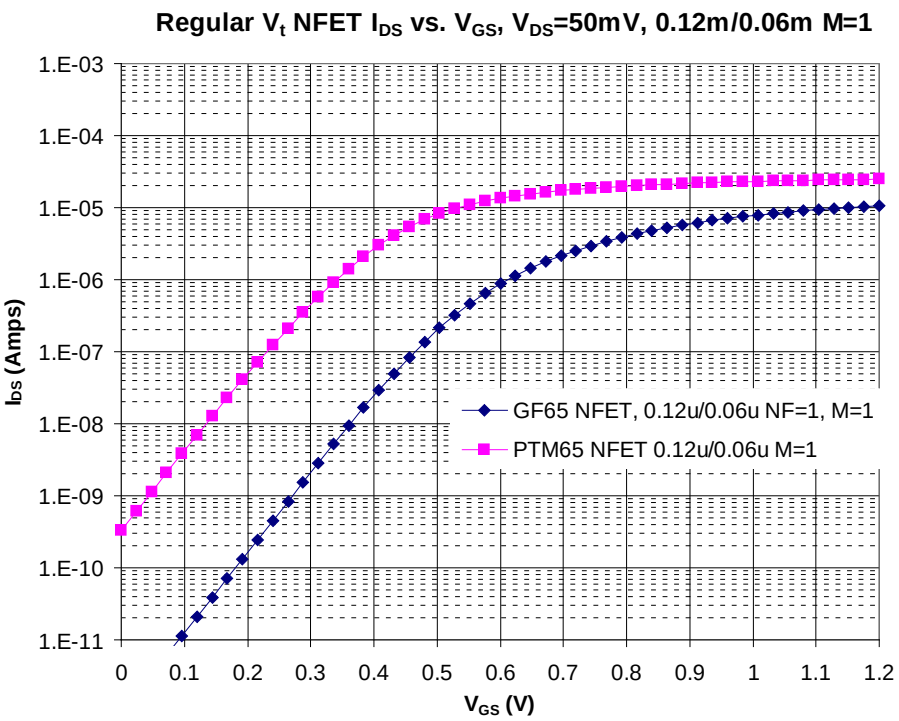
Transient Waveform at Plus and Minus Outputs



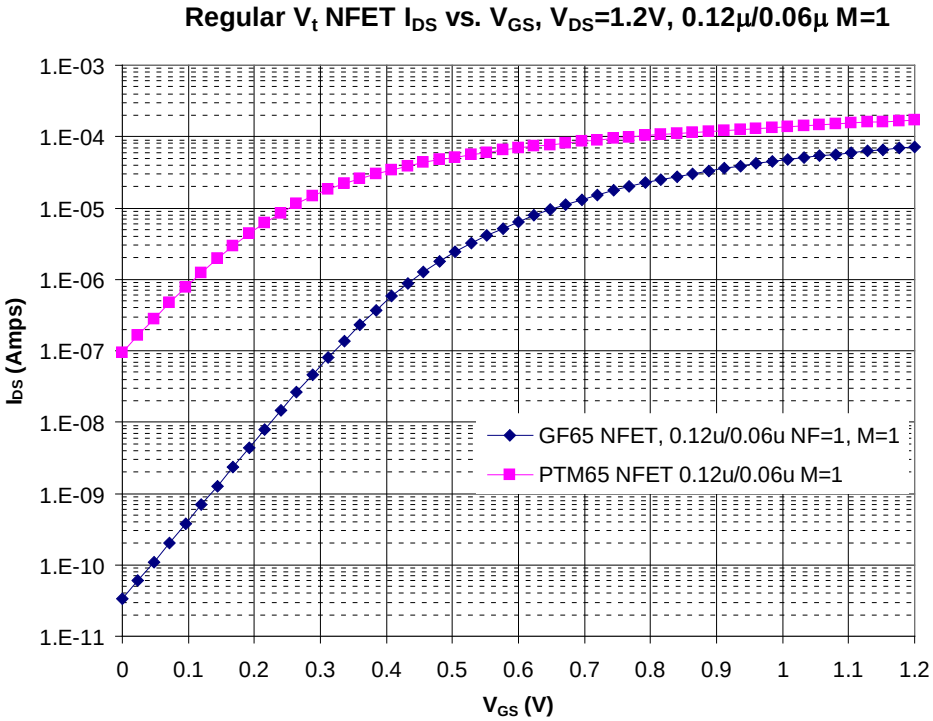
Differential Output transient waveform

NFET Device Comparison

I_{DS} vs V_{GS} for 0.12u/0.06u M=1 NFET

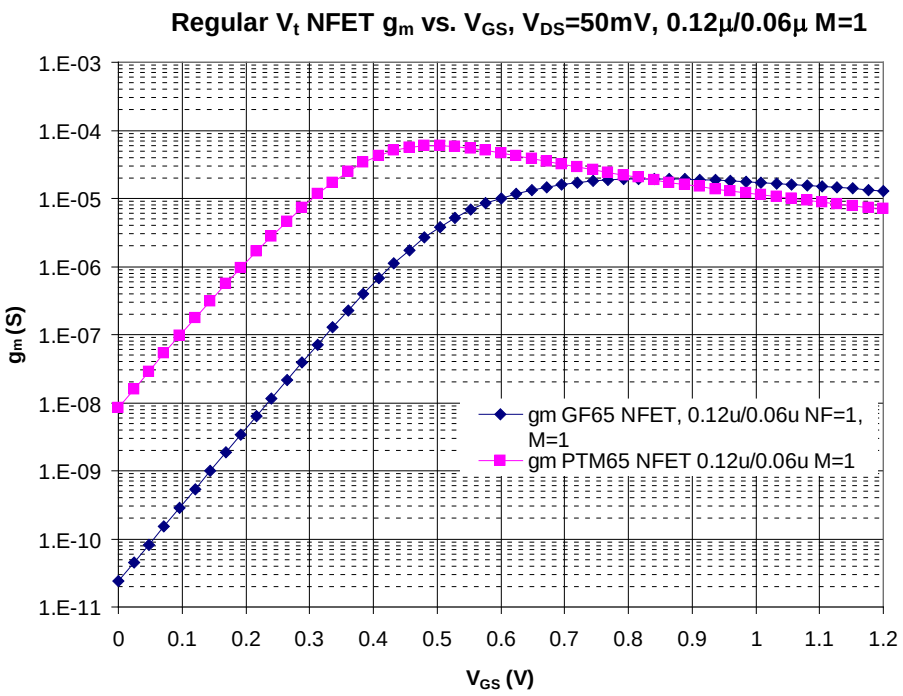


Estimate Vtlin at Vds=50 mV, Vbs=0V using IDS = 0.1uA * (W/L) per CCM

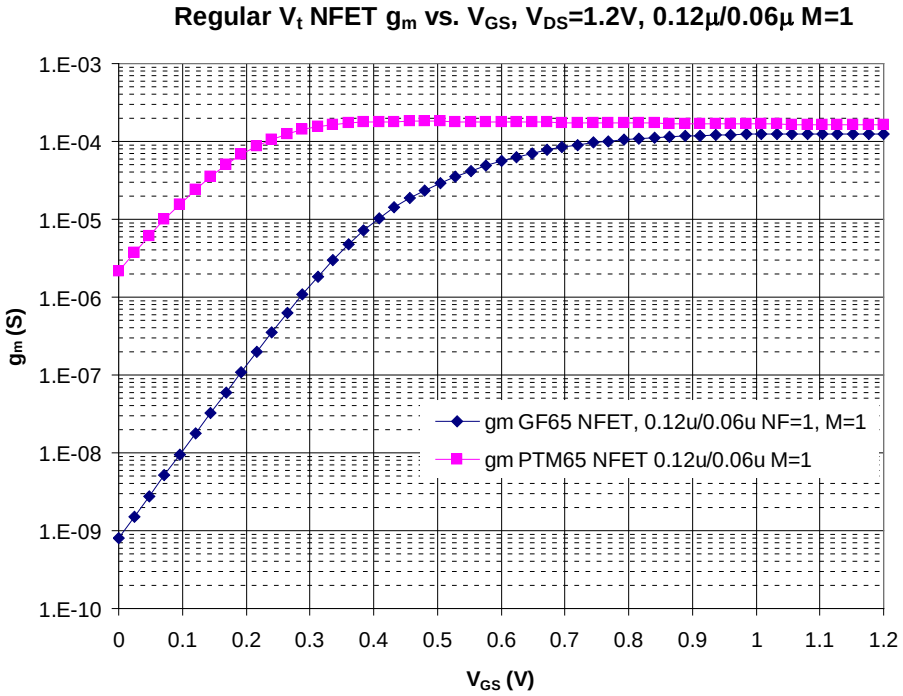


Estimate Vtsat at Vds=1.2 V, Vbs=0V using IDS = 0.1uA * (W/L) per CCM

g_m vs V_{GS} for 0.12u/0.06u M=1 NFET

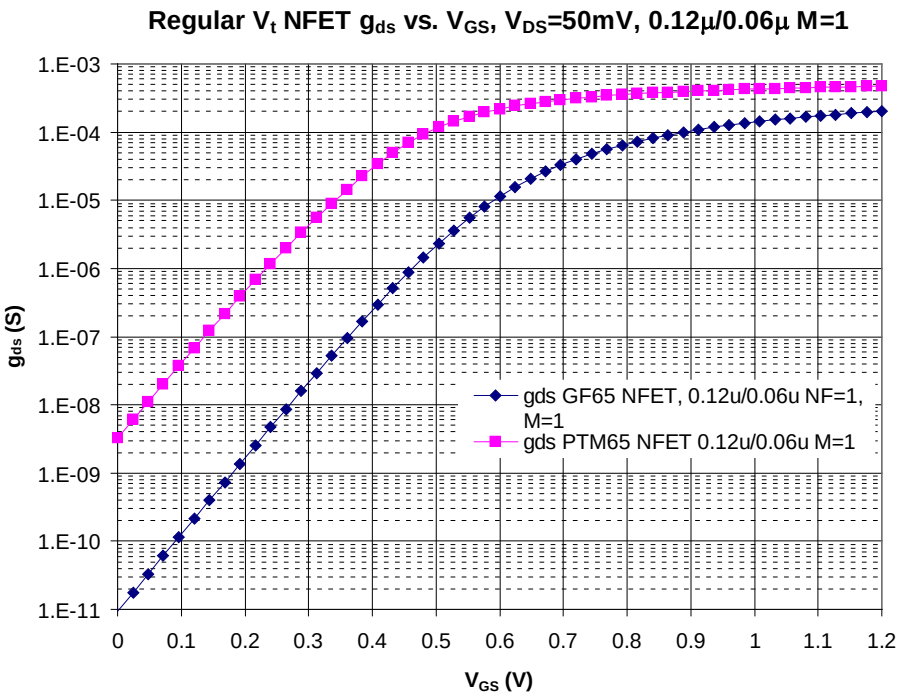


V_{DS} = 50 mV, V_{BS} = 0V, Varying V_{GS}



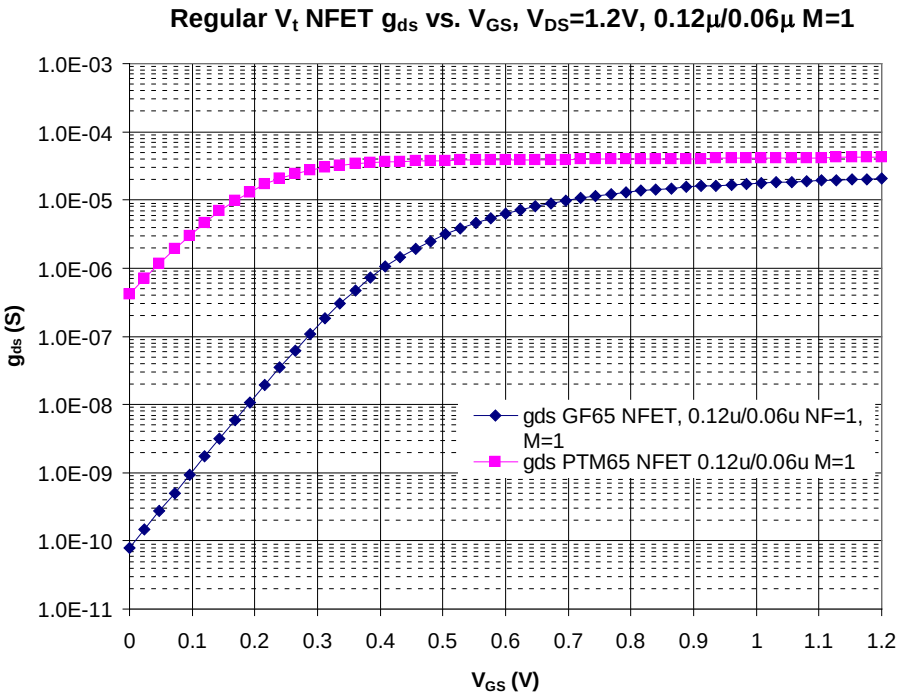
V_{DS} = 1.2 V, V_{BS} = 0V, Varying V_{GS}

g_{ds} vs V_{GS} for 0.12u/0.06u M=1 NFET



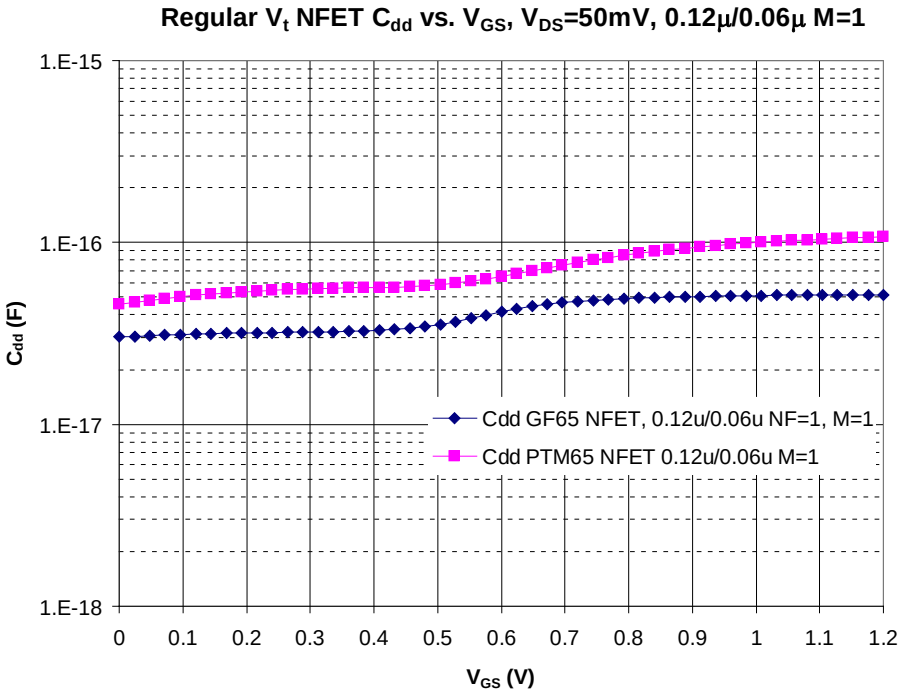
V_{DS} = 50 mV, V_{BS} = 0V, Varying V_{GS}

Lower is better.



V_{DS} = 1.2 V, V_{BS} = 0V, Varying V_{GS}

C_{dd} vs V_{GS} for 0.12u/0.06u M=1 NFET



V_{DS} = 50 mV, V_{BS} = 0V, Varying V_{GS}

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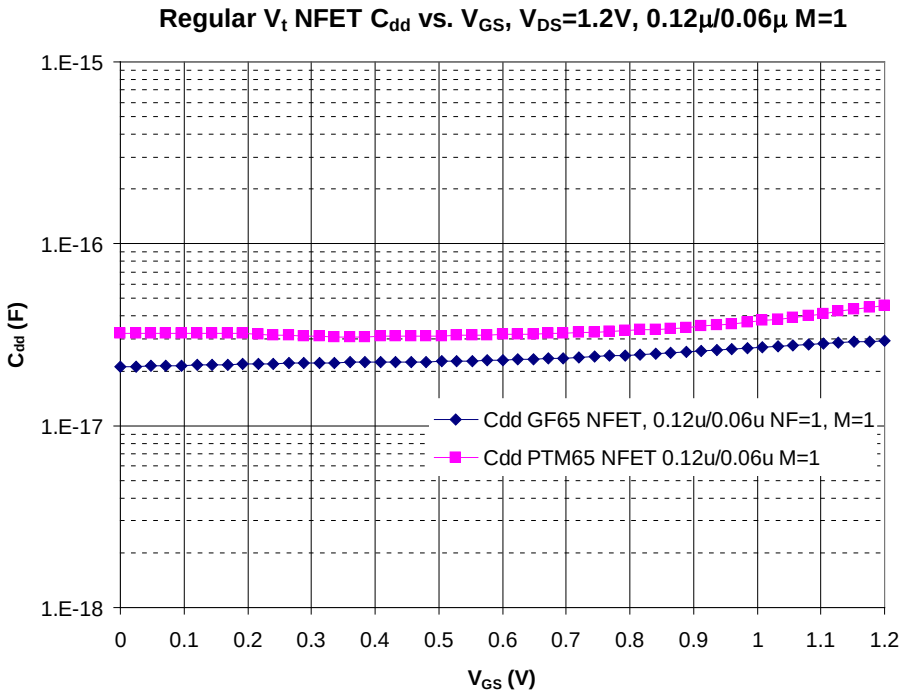
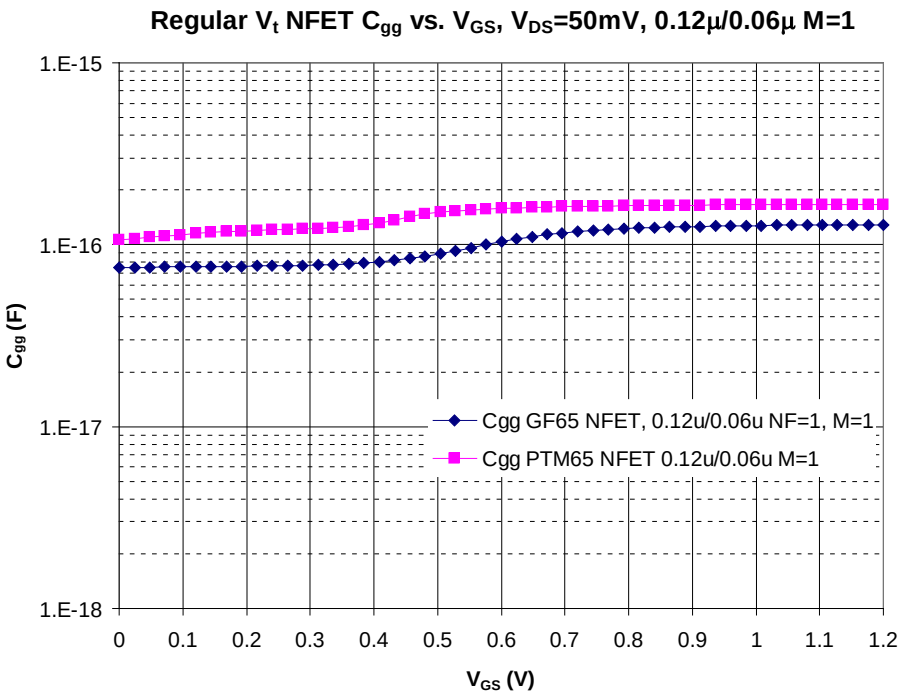


V_{DS} = 1.2 V, V_{BS} = 0V, Varying V_{GS}

C_{gg} vs V_{GS} for 0.12u/0.06u M=1 NFET



V_{DS} = 50 mV, V_{BS} = 0V, Varying V_{GS}

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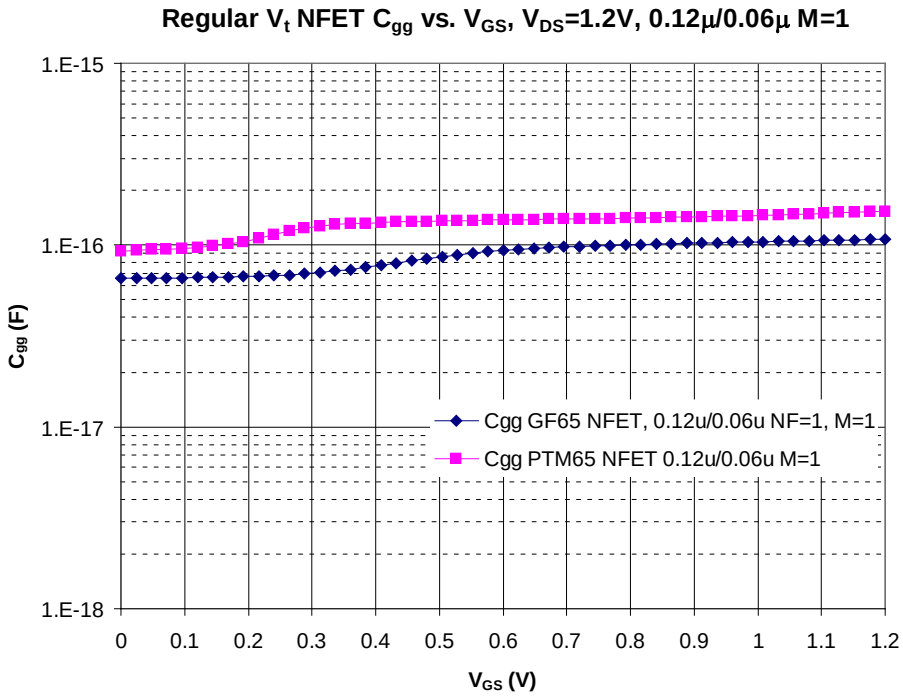
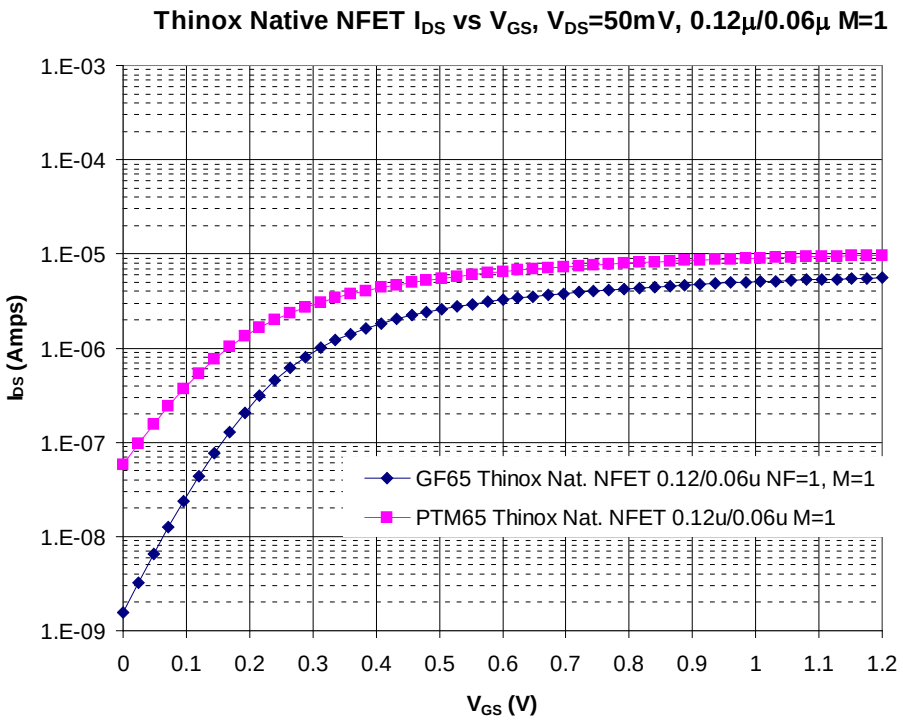
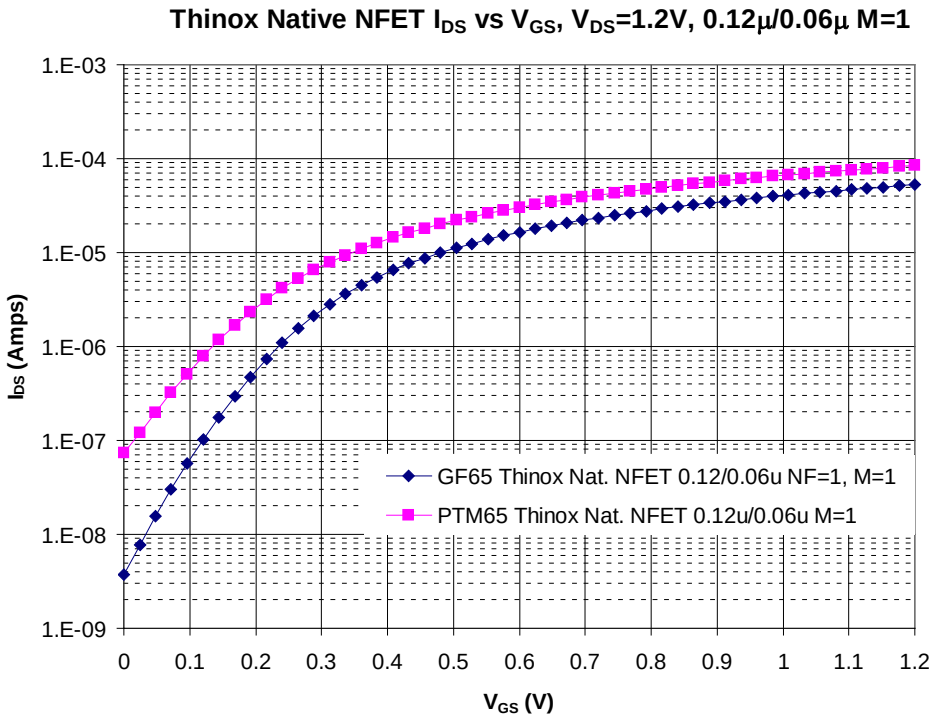


V_{DS} = 1.2 V, V_{BS} = 0V, Varying V_{GS}

Thin Oxide Native NFET Device Comparison

I_{DS} vs V_{GS} for 0.12u/0.06u M=1 ThinOx Native NFET

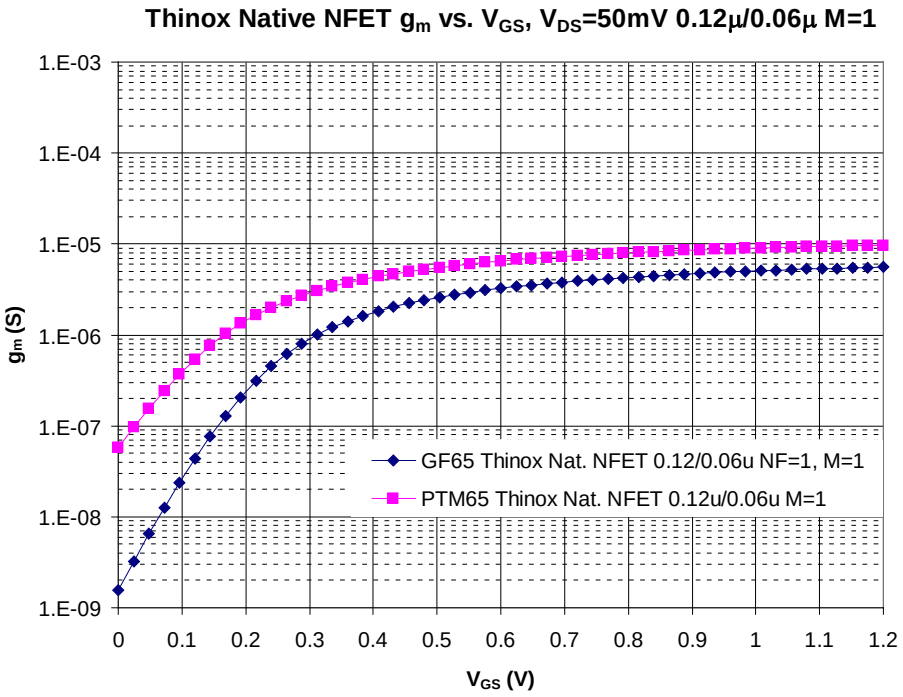




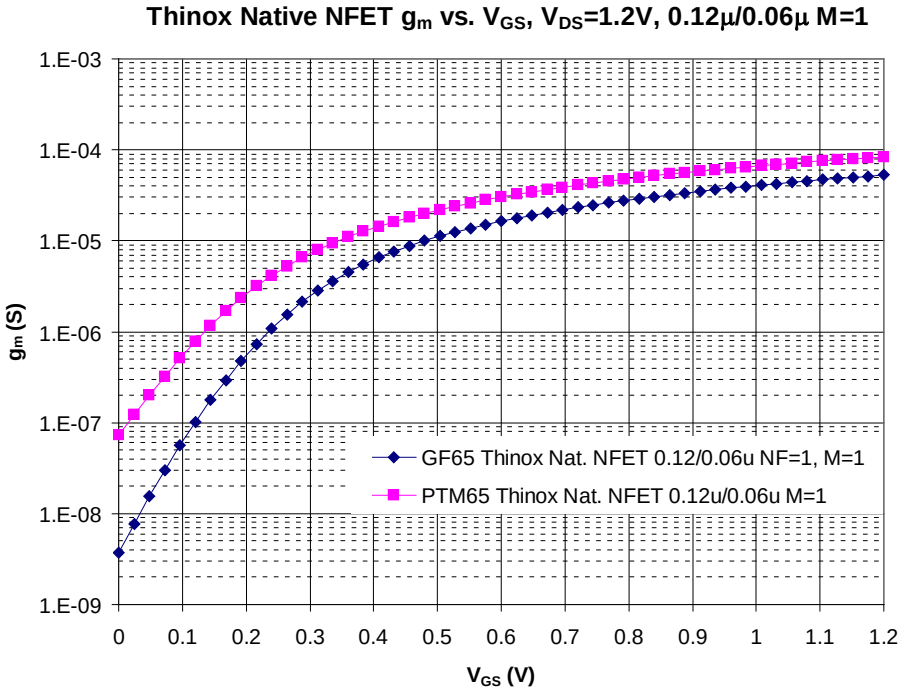
Estimate Vtlin at Vds=50 mV, Vbs=0V using IDS = 0.1uA * (W/L) per CCM

Estimate Vtsat at Vds=1.2 V, Vbs=0V using IDS = 0.1uA * (W/L) per CCM

g_m vs V_{GS} for 0.12u/0.06u M=1 ThinOx Native NFET

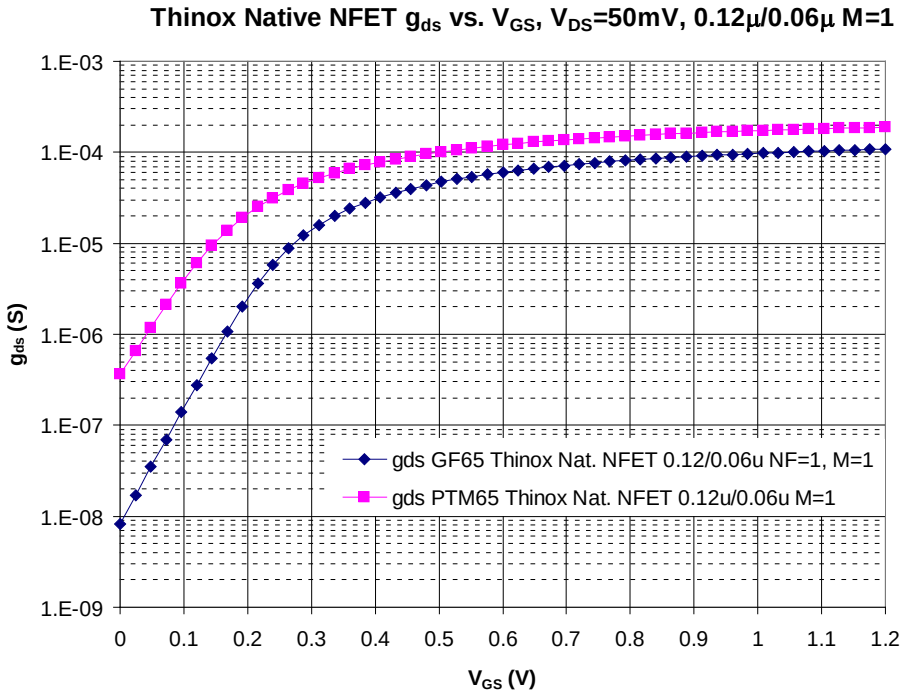


V_{DS} = 50 mV, V_{BS} = 0V, Varying V_{GS}



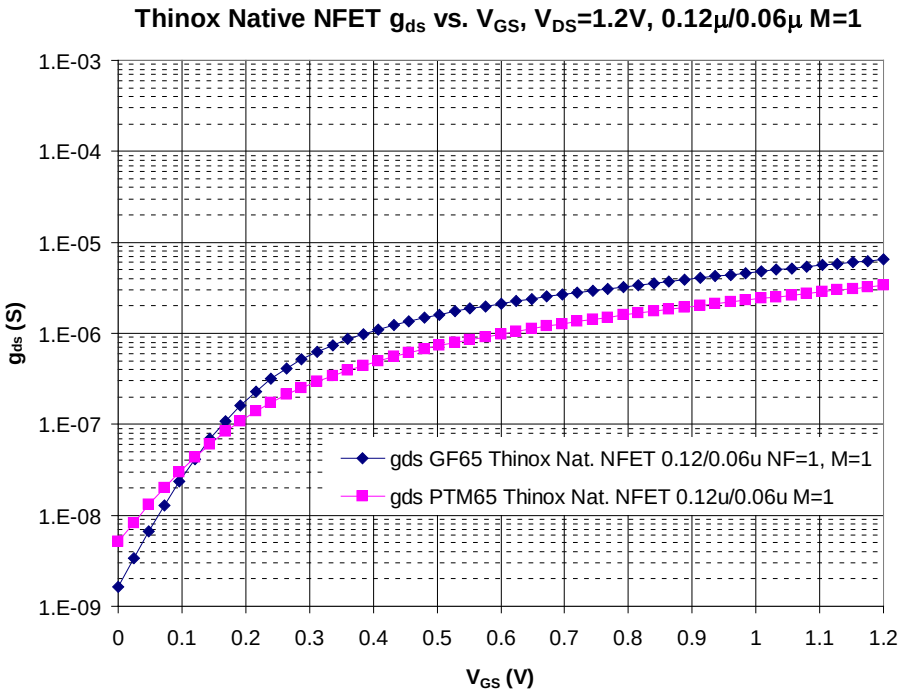
V_{DS} = 1.2 V, V_{BS} = 0V, Varying V_{GS}

g_{ds} vs V_{GS} for 0.12u/0.06u M=1 ThinOx Native NFET



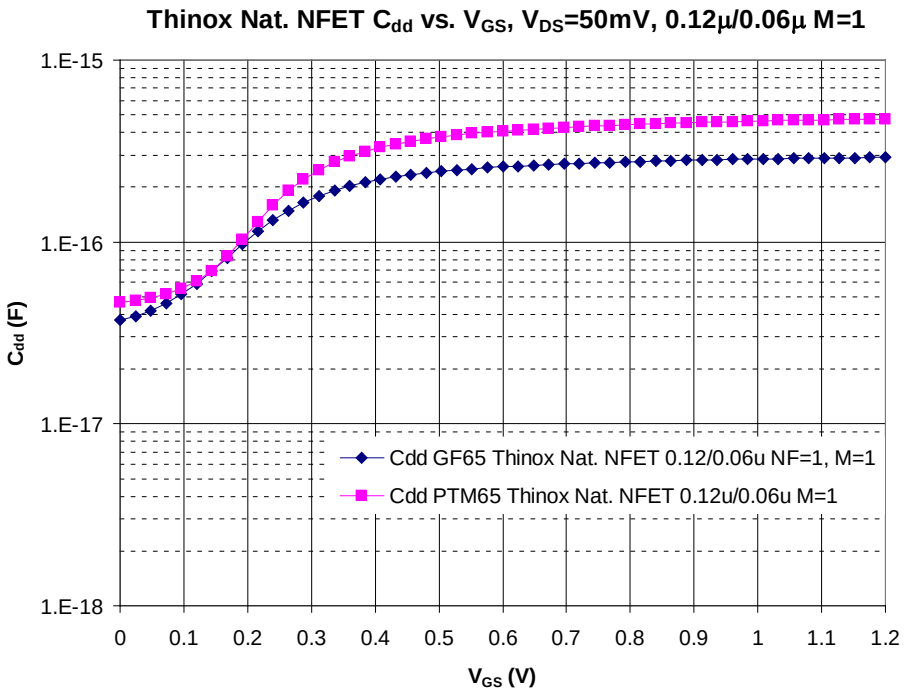
V_{DS} = 50 mV, V_{BS} = 0V, Varying V_{GS}

Lower is better.



V_{DS} = 1.2 V, V_{BS} = 0V, Varying V_{GS}

C_{dd} vs V_{GS} for 0.12u/0.06u M=1 ThinOx Native NFET



V_{DS} = 50 mV, V_{BS} = 0V, Varying V_{GS}

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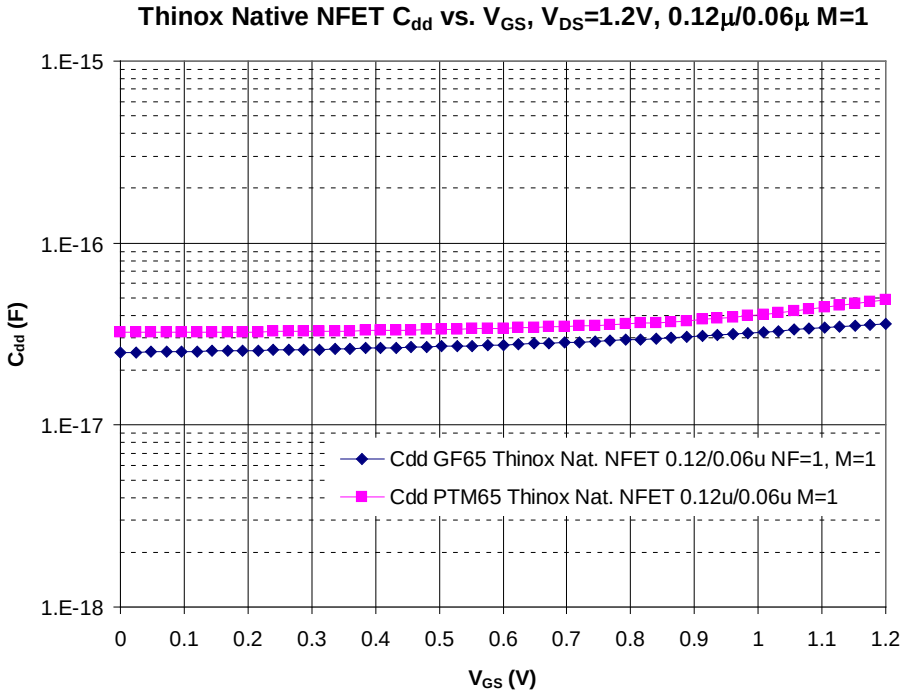
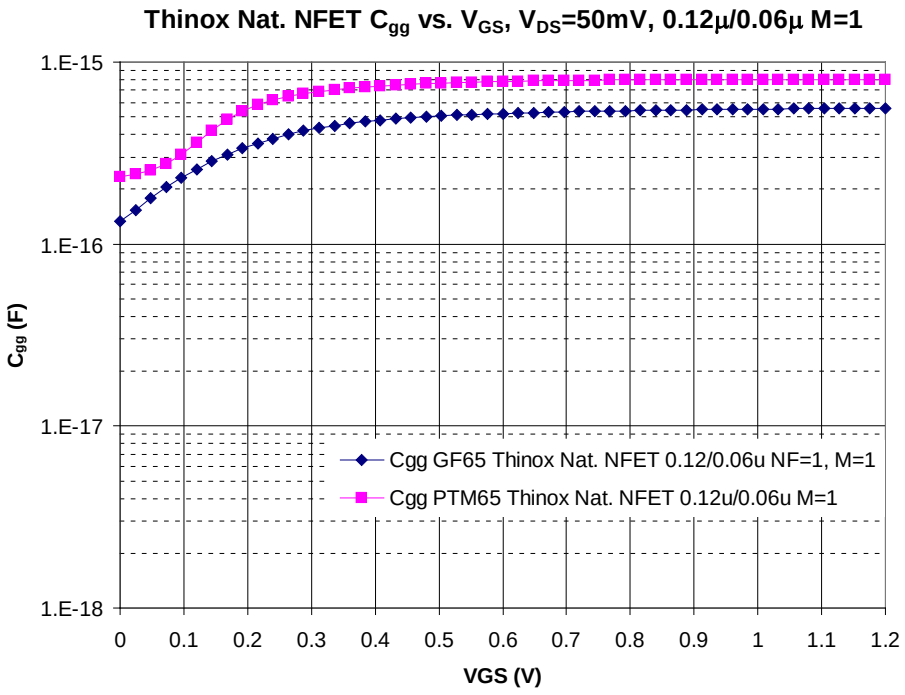


V_{DS} = 1.2 V, V_{BS} = 0V, Varying V_{GS}

C_{gg} vs V_{GS} for 0.12u/0.06u M=1 ThinOx Native NFET



V_{DS} = 50 mV, V_{BS} = 0V, Varying V_{GS}

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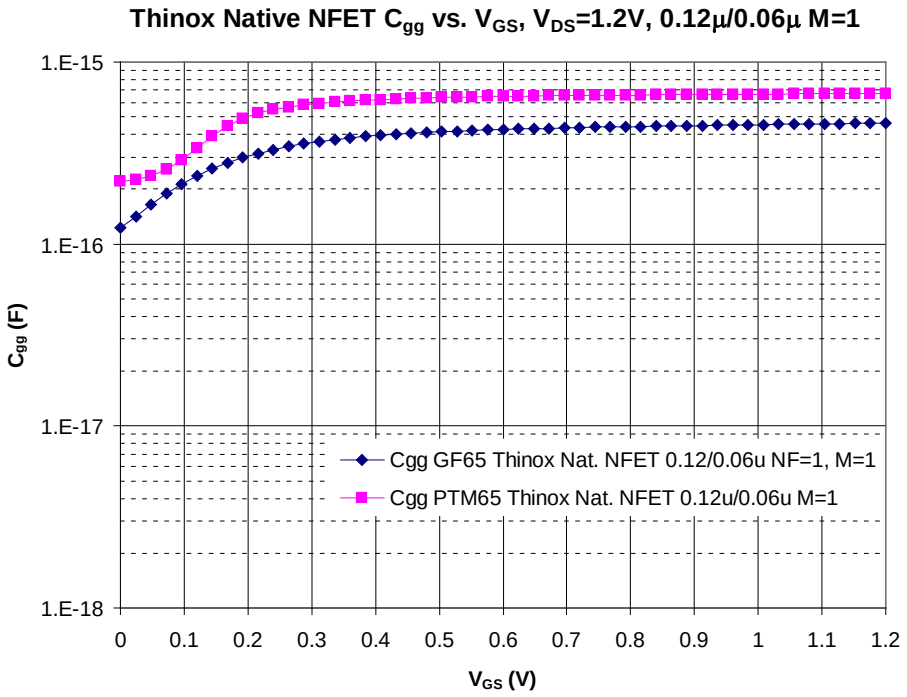

V_{DS} = 1.2 V, V_{BS} = 0V, Varying V_{GS}