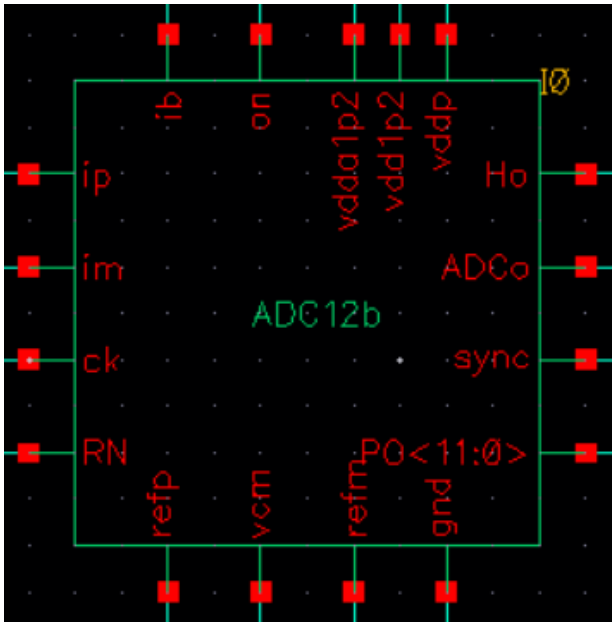
GF65nm 12b SAR ADC

ADC Simulation Results

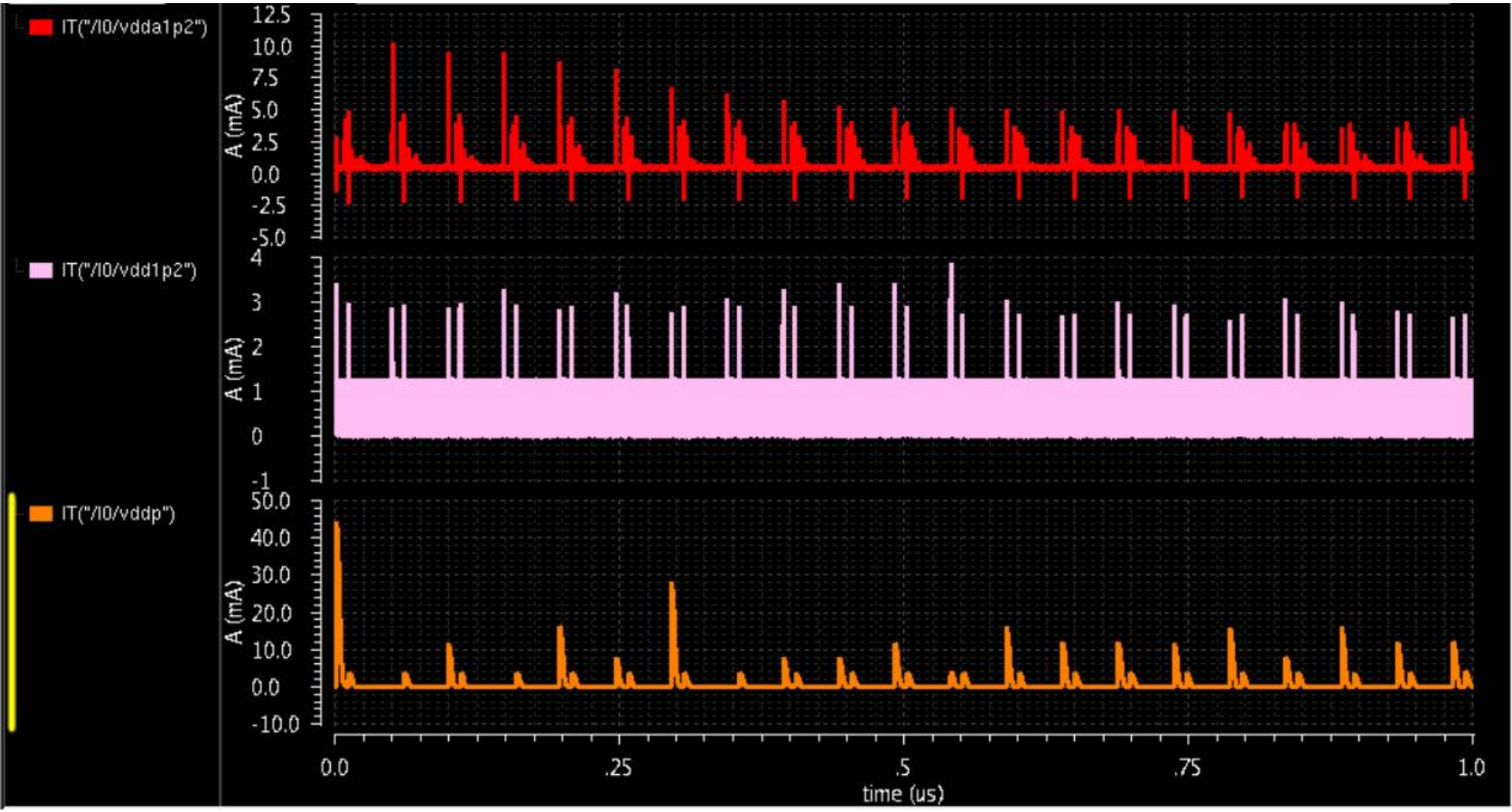
Test Benches provided in submission library

ADC pin out definitions



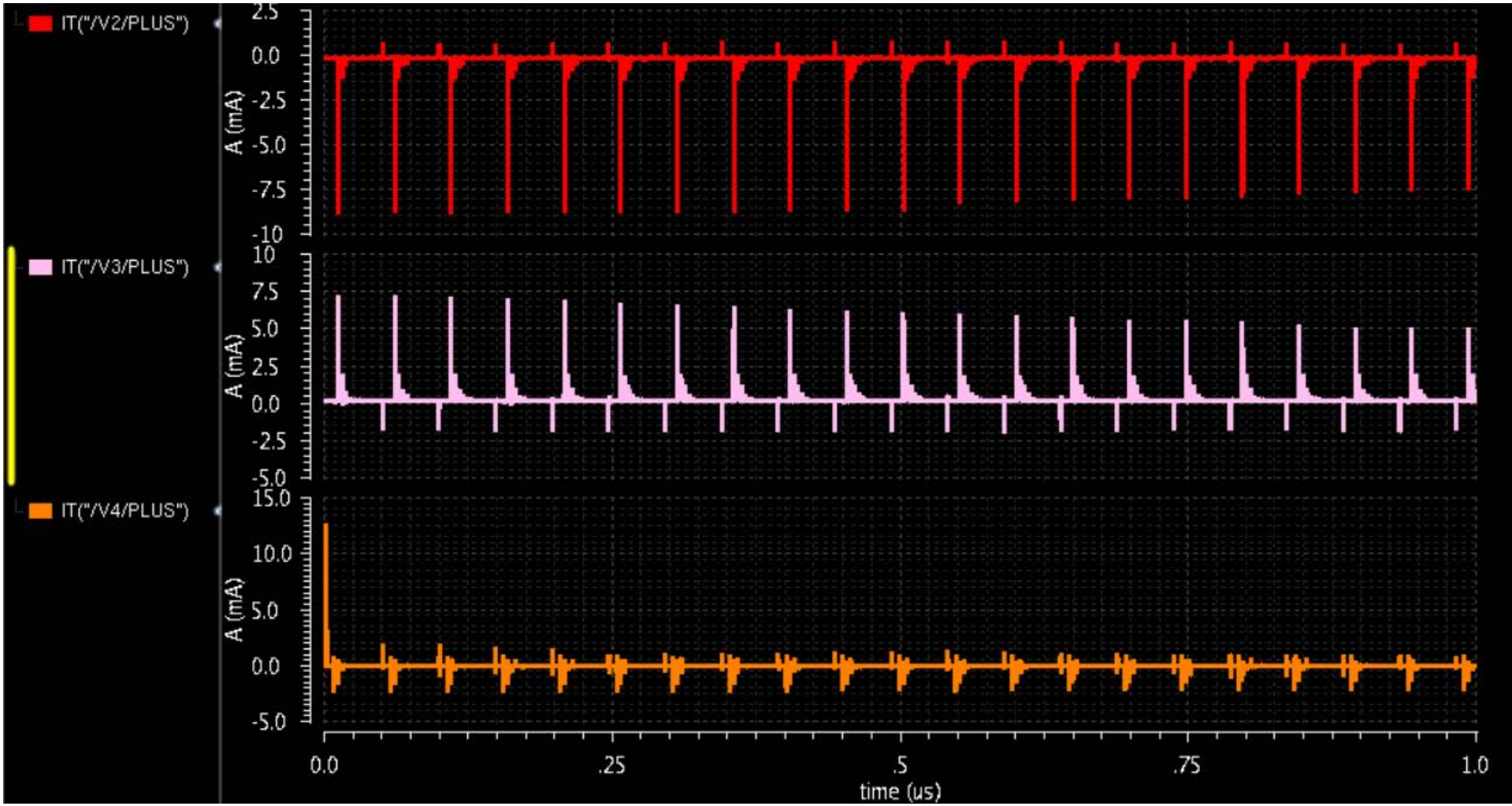
- ip & im: differential input; on: logic 1 to turn on ADC
- ck: clock input (sampling rate x 14); RN: logic 0 to reset ADC
- refp & refm: differential reference inputs (refp = 1.2V & refm = 0V)
- vcm: common-mode input (set to 0.6V)
- gnd: ground; vdda1p2: 1.2V analog supply; vddd1p2: 1.2V digital supply; vddp = 1.2V output pad driver supply; ib: current bias input (10uA source to ib)
- Ho: serial data sync signal; ADCo: ADC serial data output starting after Ho (Both Ho & ADCo need LVDS drivers (not included))
- sync: sync signal for parallel output; PO<11:0>: 12-bit parallel ADC output starting at the falling edge of sync (max 10pF at outputs for 20MS/s)

Test Bench test_ADC12b (I): supply current



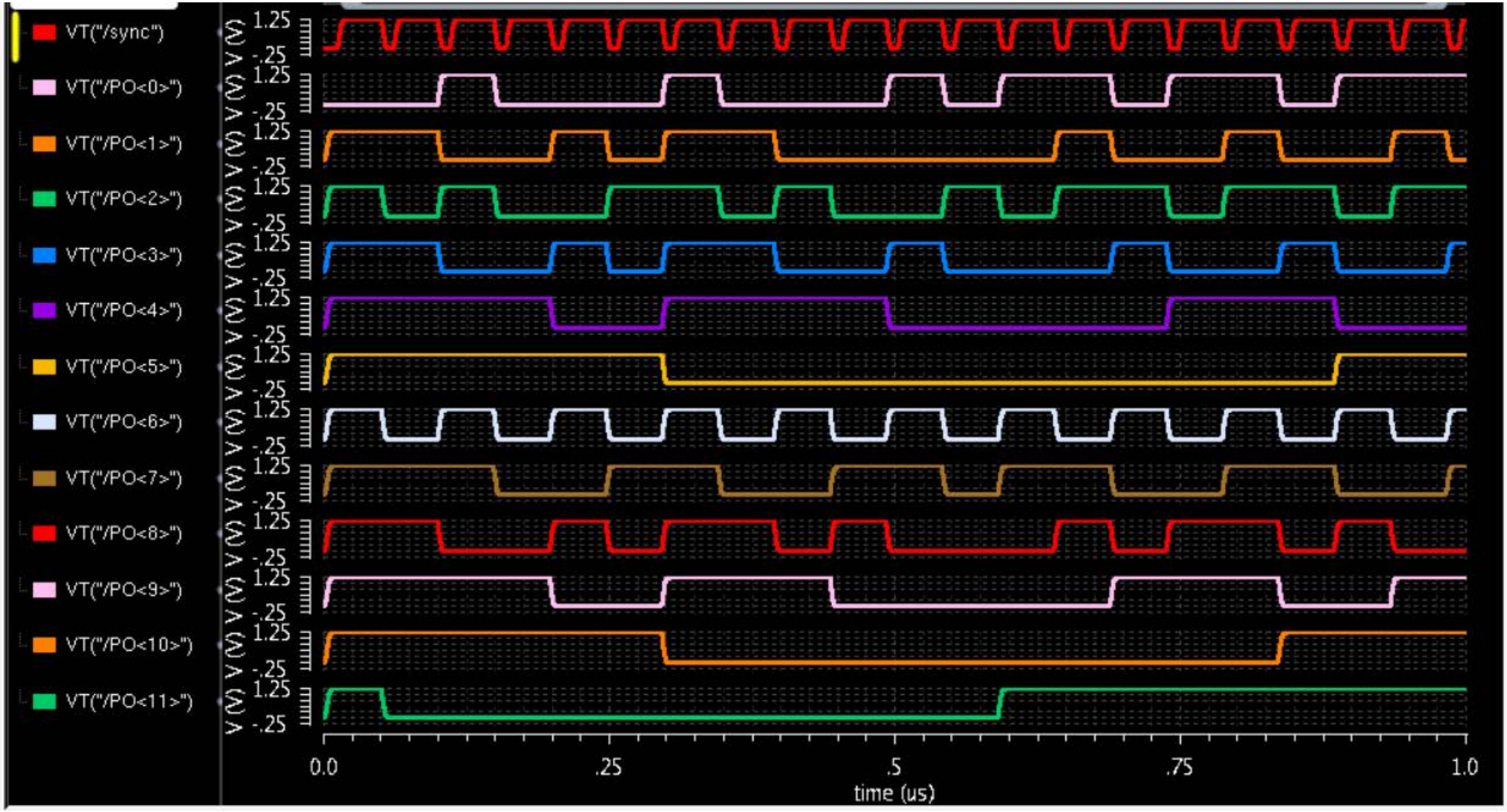
- Schematic: test_ADC12b
- Sampling rate ~ 20MS/s (sample period = 14 x 3.5ns), Vdd = 1.2V
- Top – analog supply current (avg. = 483.4uA); middle – digital supply current (avg. = 93.1uA); bottom – output driver supply current (avg. = 1.024mA)

test_ADC12b (II): current drawn by references



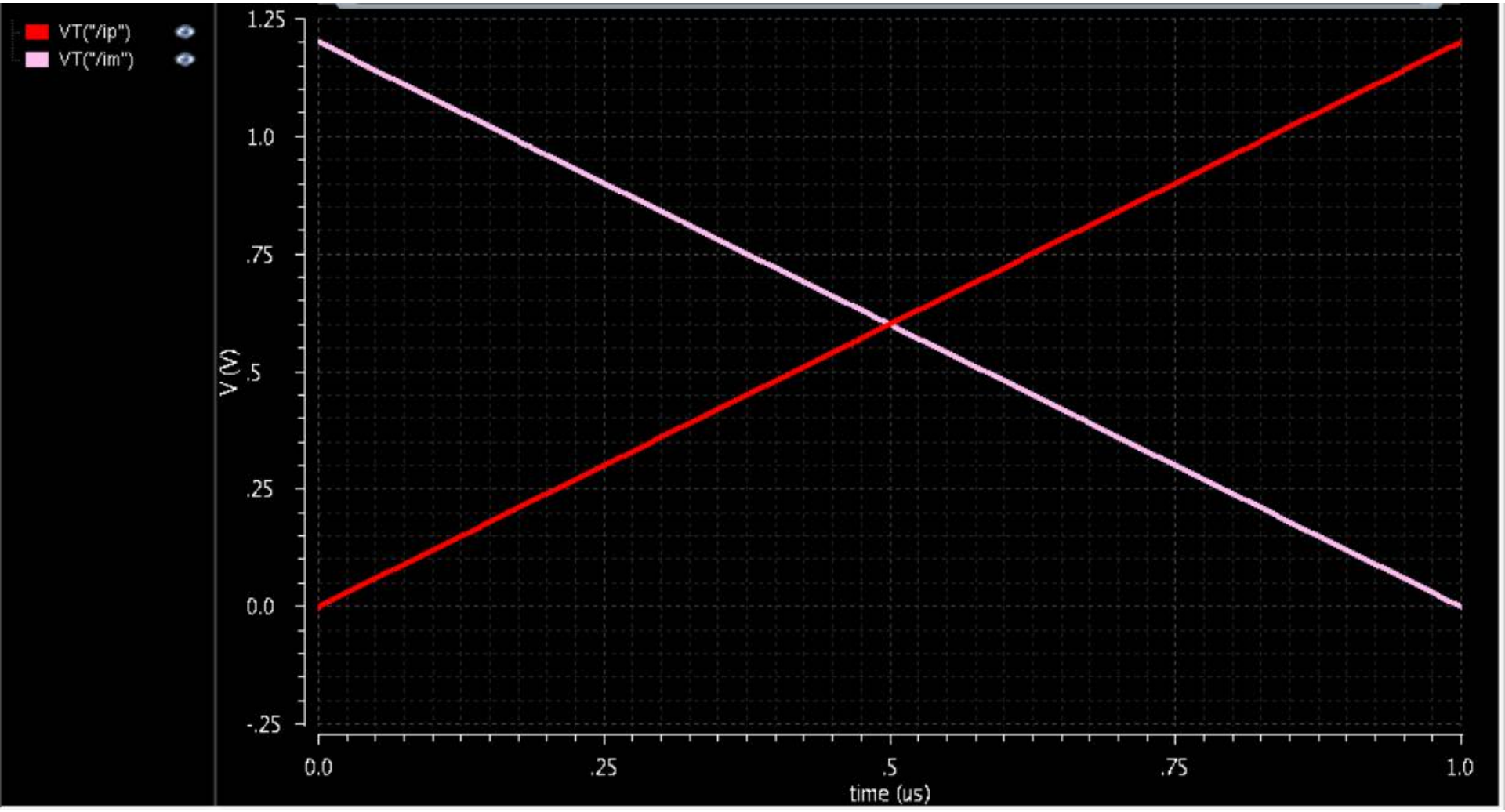
- Top – refp (avg. = 189.3uA); middle – vcm (avg. = 196.2uA); bottom – refm (avg. = 1.2uA)

Test Bench test_ADC12b (III): sync & PO<11:1>

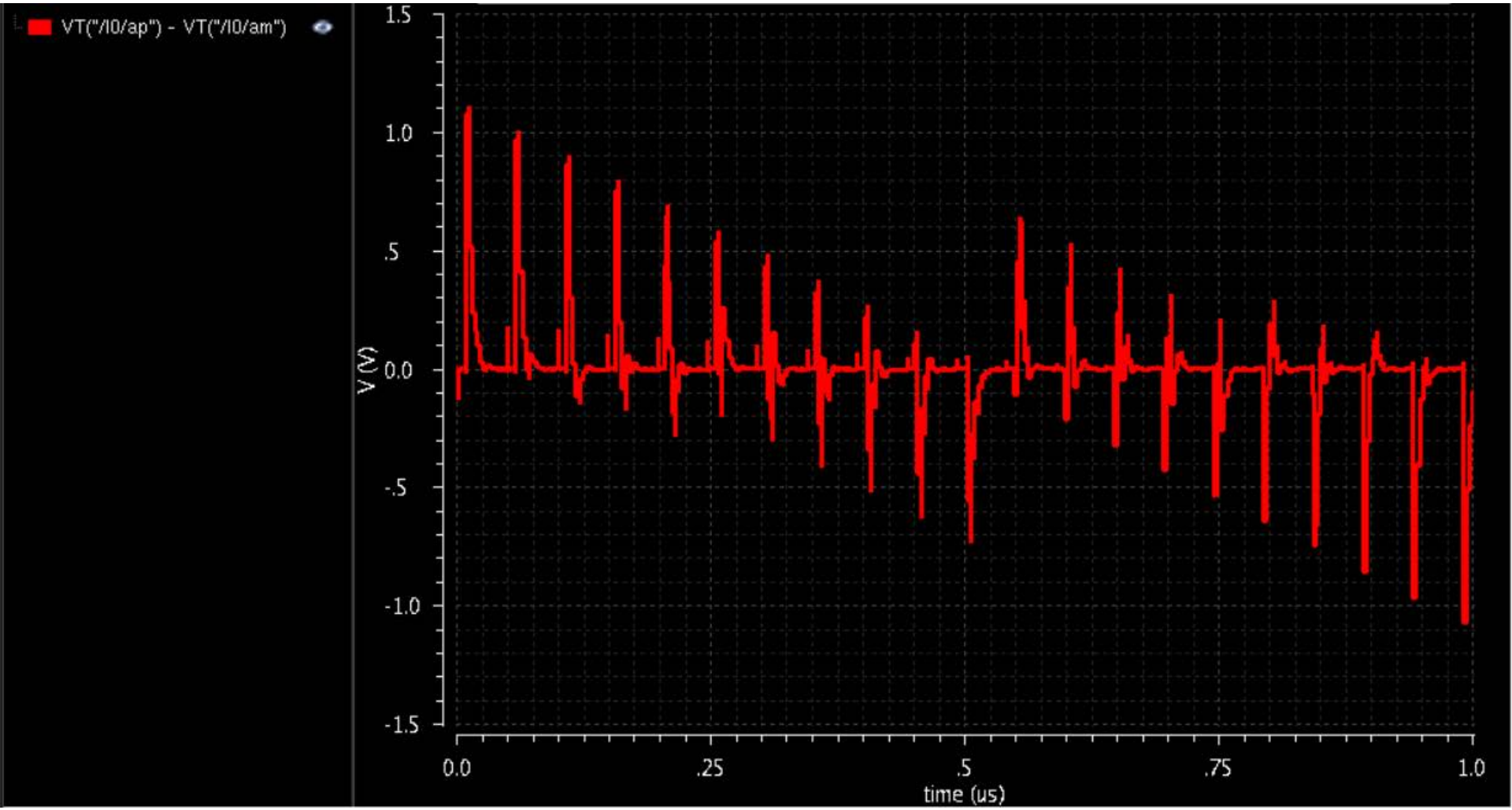


- Differential linear ramp down input from 1.2V to 0V from 0 to 1us (shown in next slide)
- Parallel outputs (PO<11:0>) and sync have 10pF cap loads

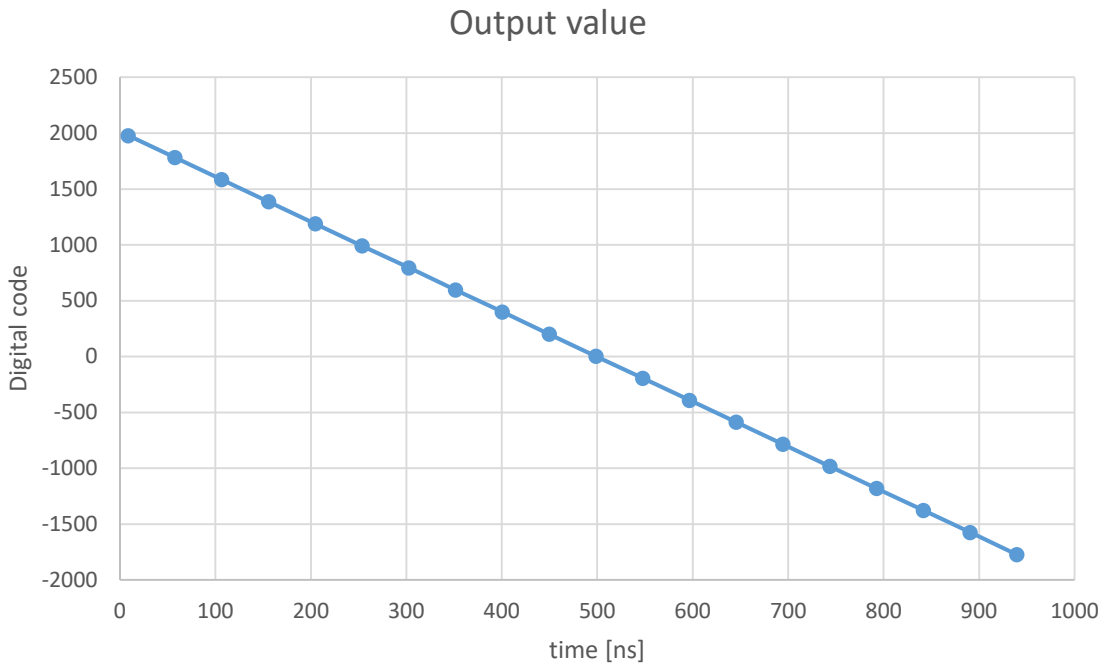
Test Bench test_ADC12b (IV): differential input



test_ADC12b (V): difference b/w comparator input

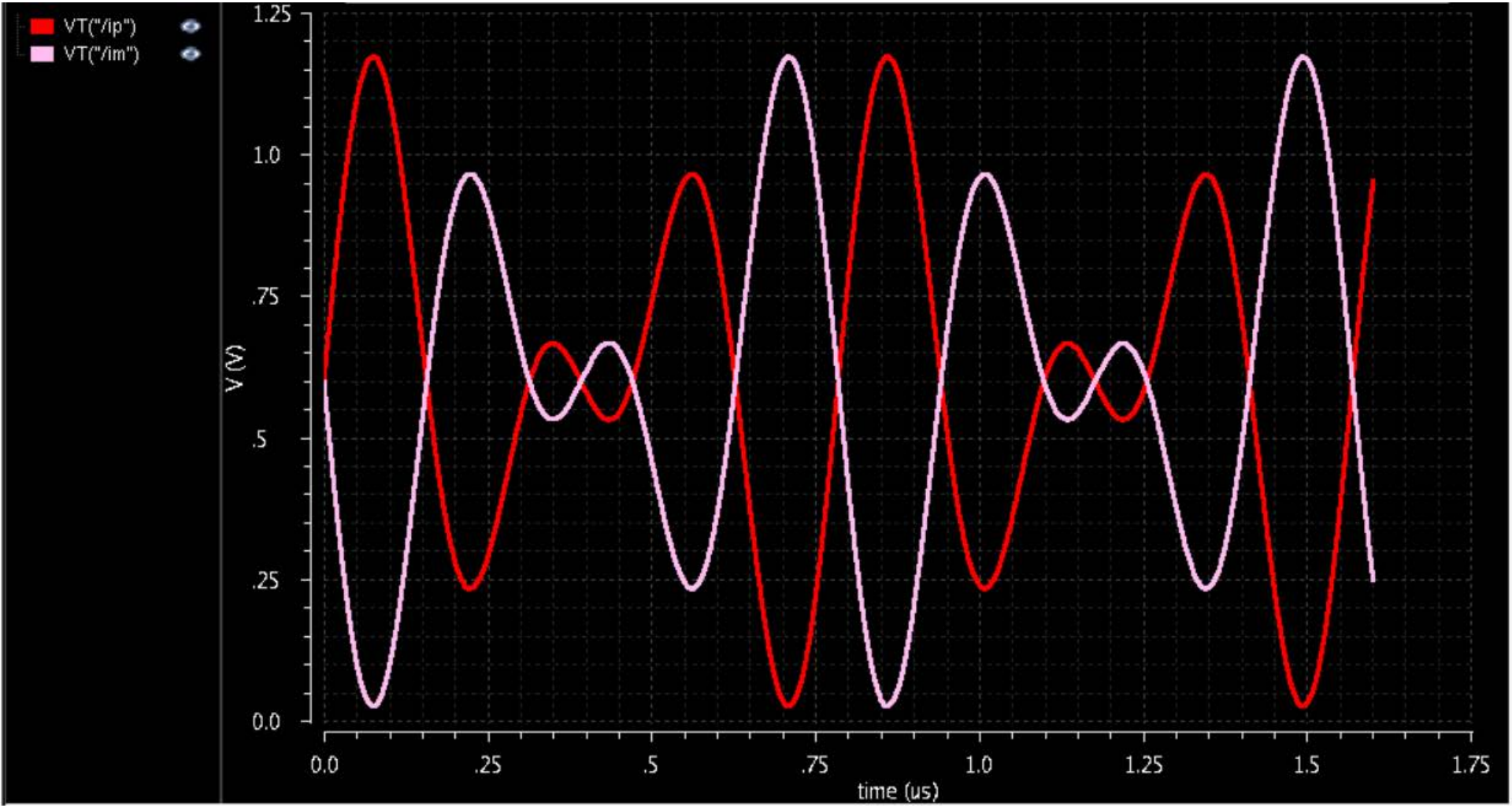


test_ADC12b (VI): reconstruction output



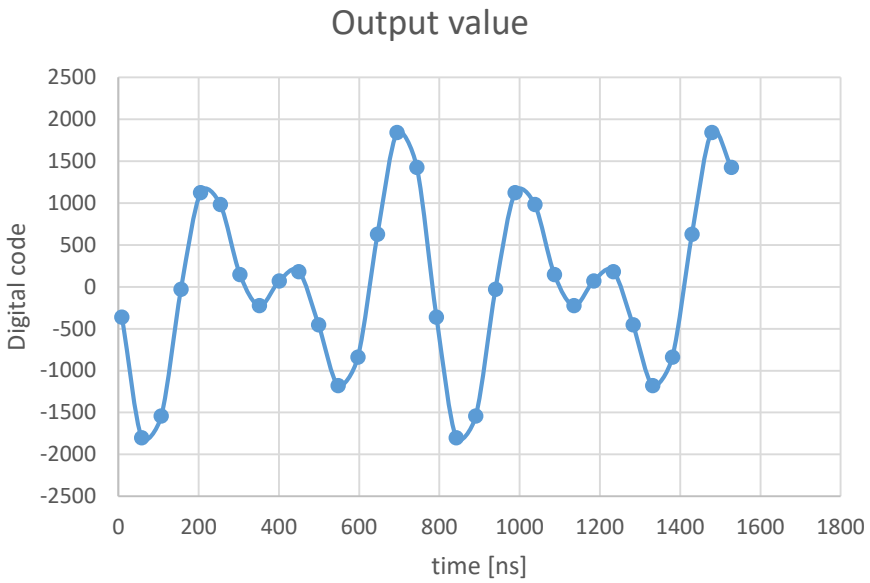
- Output = (1-2*PO<11>)*(2^10*PO<10> + … + 2^0*PO<0>)
- Refer to schematic for formula that calculates output from serial output data
- Linearity is within -0.79 LSB and +1.37 LSB (1 V_LSB ~ 0.586mV)

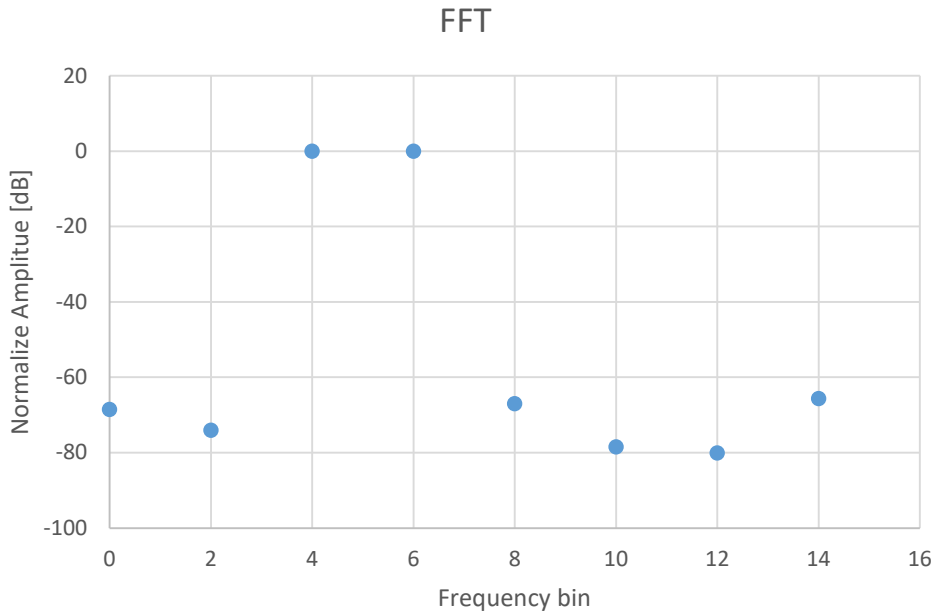
Test Bench test_ADC12b_sin (I): differential input



- Schematic: test_ADC12b_sin
- Sampling rate ~ 20MS/s (sample period = 14 x 3.5ns), Vdd = 1.2V
- Input frequencies: 4/(32 x 14 x 3.5ns) ~ 2.551MHz & 6/(32 x 14 x 3.5ns) ~ 3.827MHz with equal diff. amplitude (diff. peak value) = 600mV

test_ADC12b_sin (II): reconstruction output





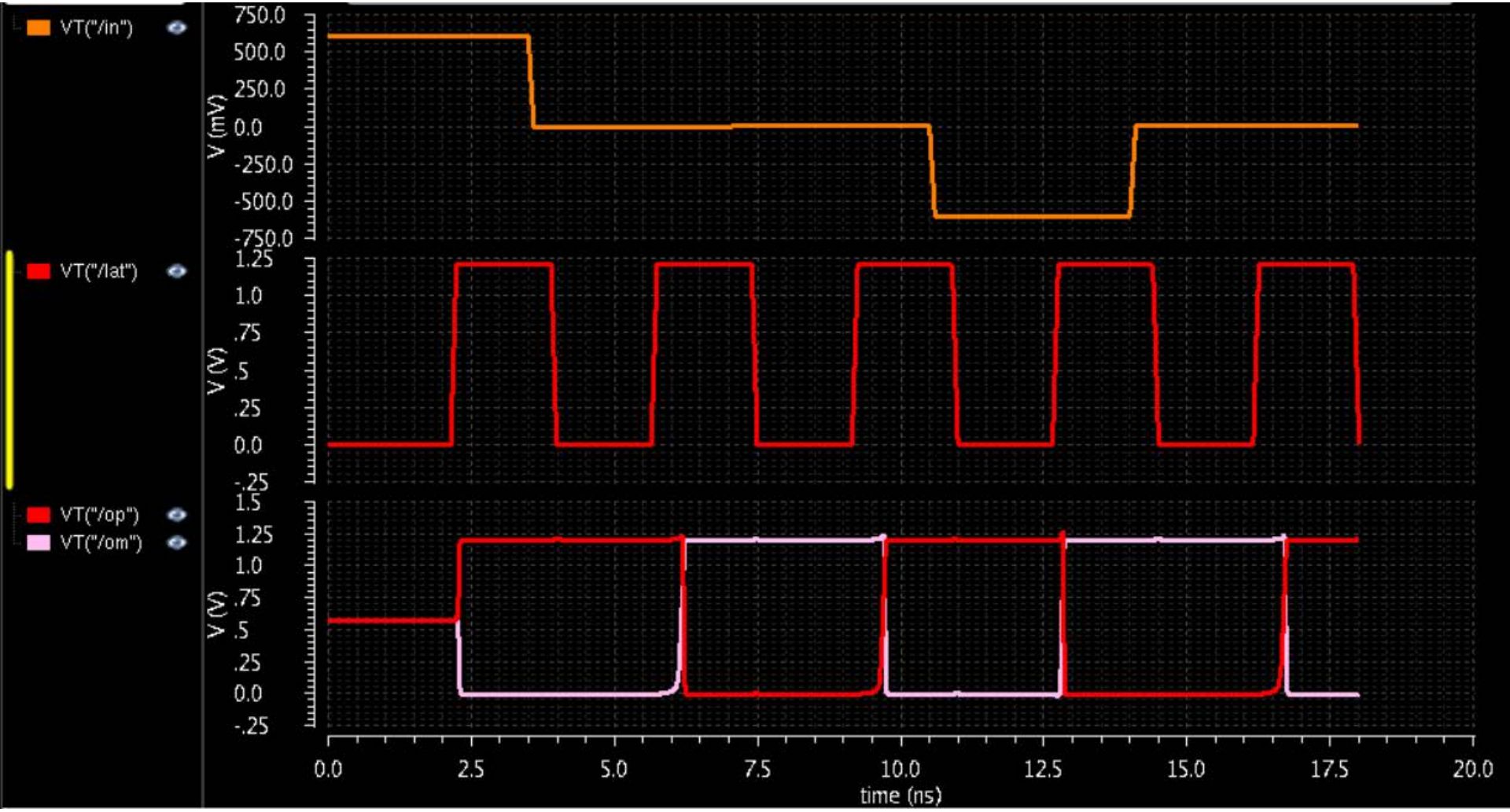
- Each frequency bin = 1/(32 x 14 x 3.5ns) ~ 637.755kHz
- IMD_3 < -66.98dB
- SNDR = 64.72 dB

GF65nm 12b SAR ADC

Comparator Simulation Results

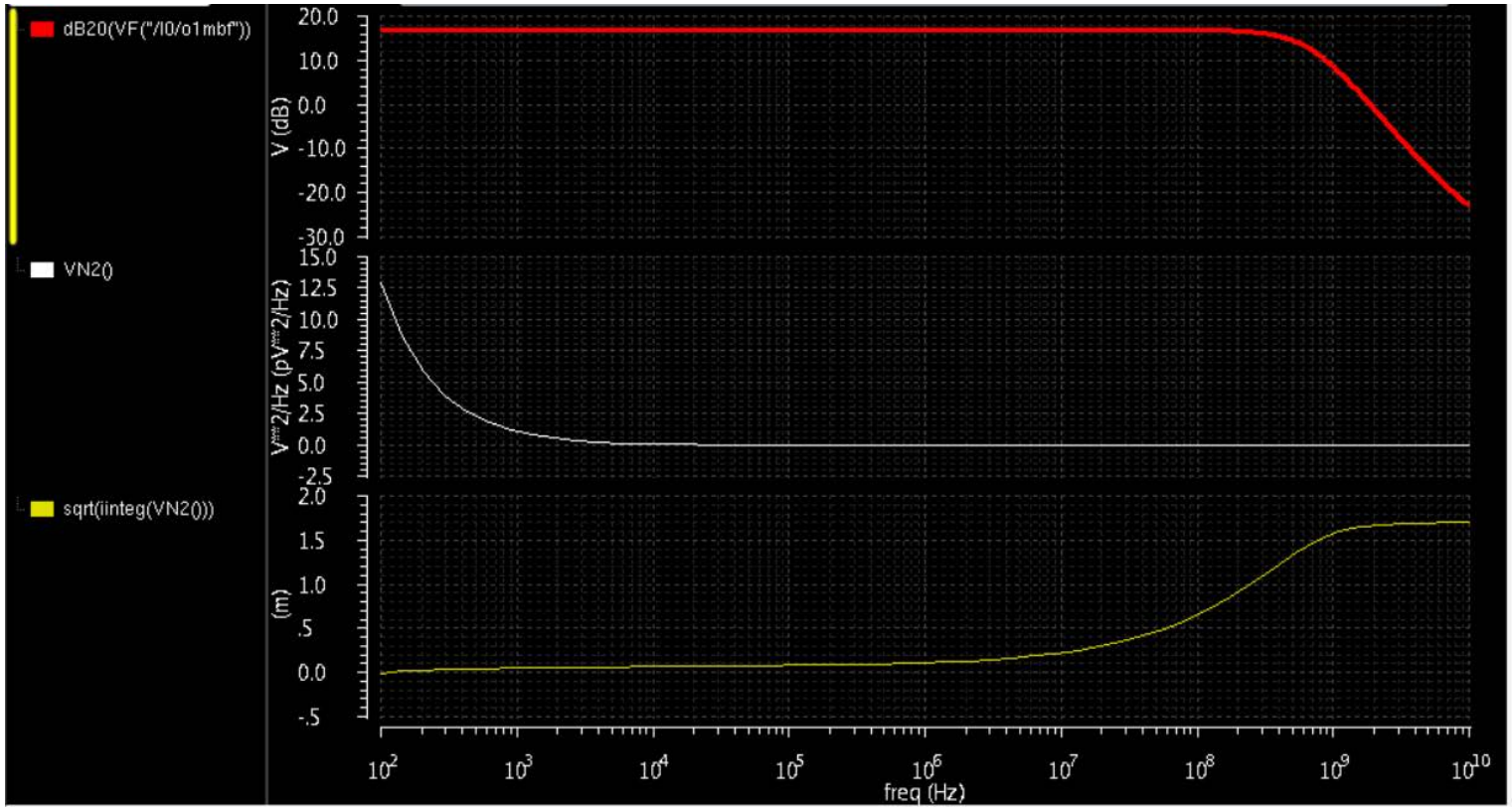
Test Benches provided in submission library

Comparator Sim. Setup (1): (**test_comp2**)



- ADC full range: -1.2V – 1.2V for 12-bit resolutions
- V_LSB = 2.4V/4096 = 0.586mV → simulated with ½ V_LSB
- Differential input values: 0.6V, -0.29mV, 0.29mV, -0.6V, 0.29mV
- Set signal “lat” to logic 1 to latch the outputs (op & om)

Comparator Sim. setup (2): (**test_comp2_ac**)



- Red – single-ended comparator pre-amp low frequency gain (diff. gain ~ 16.83dB + 6.02dB)
- Noise due to comparator latch can be ignored due to sufficient pre-amp gain
- White – output pre-amp noise power density vs. freq.
- Yellow – Integrated output pre-amp noise voltage vs. freq. (Total pre-amp output noise ~ 1.697mV)
- Pre-amp input referred noise = 1.697mV/(10^((16.83dB + 6.02dB)/20)) ~ 122uV < ½ V_LSB