Changes from last revision

Date	User	Edits
1/6/2020	Prof. Levi's Design Team	USC Release of PTM65 design from GF65 design

Subsystem or block descriptions

Design name	Six-pole 7MHz AAFilter in PTM65nm CMOS
The Top-level cell name	Aafilter_7MHz_PTM65_AllDevices
Designer	Prof. Levi's Design Team
Organization	University of Southern California

Overview

10 bit linearity Anti-Alias Filter with -3 dB bandwidth of 7 MHz. Originally designed, simulated at 39 PVT corners, fabricated and measured in GF65LPe process.

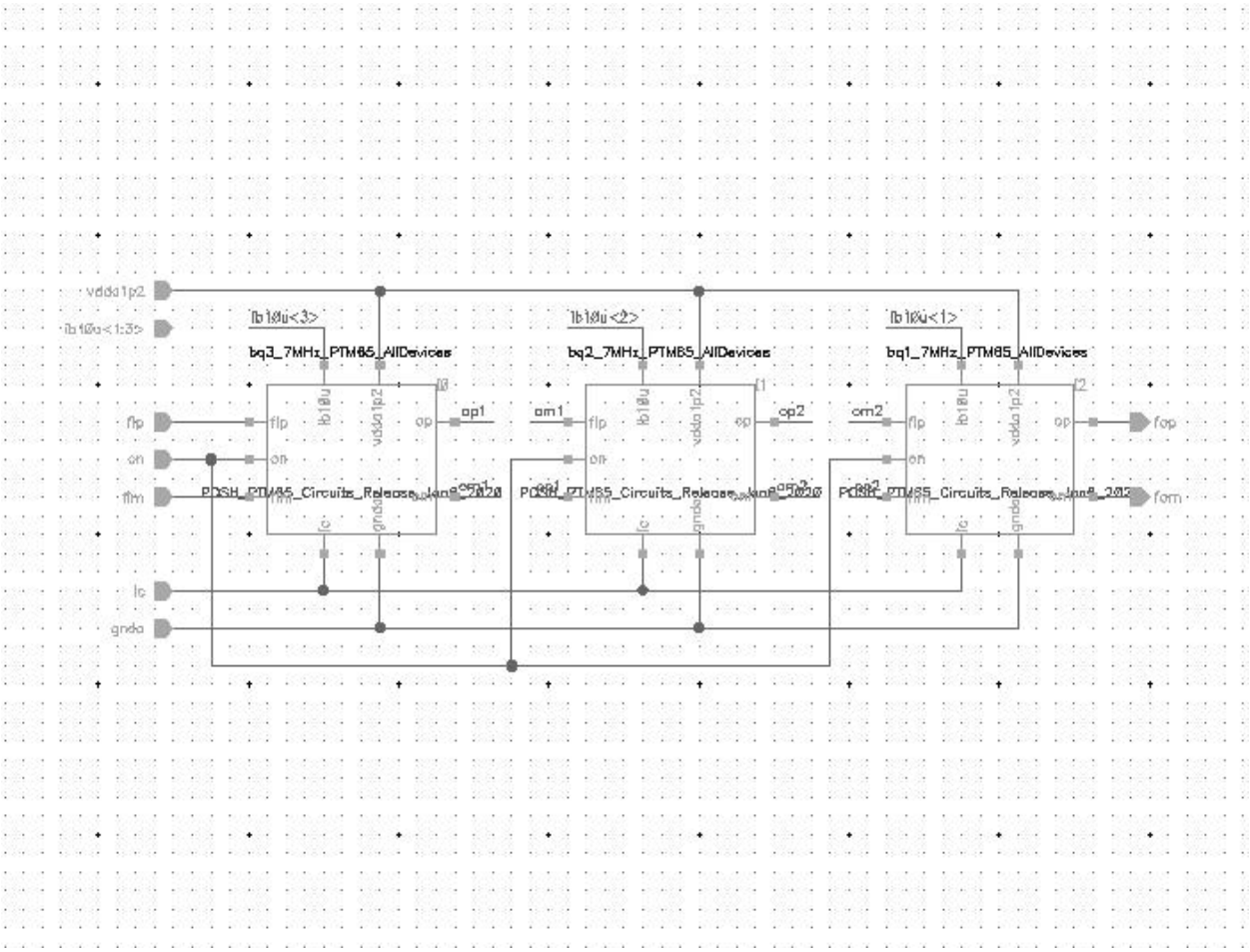
Block Specifications and Compliance

.

Spec Name	Nominal	Max	Note
DC gain (dB)	-0.004844	N/A	PTM65 has no process corners. Simulated at available corner, 27C, Vdd=1.2V
f_3dB (MHz)	7.244	N/A	PTM65 has no process corners. Simulated at available corner, 27C, Vdd=1.2V
f_50dB (MHz)	18.33	N/A	PTM65 has no process corners. Simulated at available corner, 27C, Vdd=1.2V
IM3 from DFT plot (dB)	66.86	N/A	PTM65 has no process corners. Simulated at available corner, 27C, Vdd=1.2V
Integrated	167.10	N/A	PTM65 has no process corners. Simulated at

Output (Input) Noise Voltage 10Hz to 100MHz (uVrms)			available corner, 27C, Vdd=1.2V
Power Consumption (mW)	29.45	N/A	Bias set by constant current source, see testbench called test_opamp5_PTM65_AllDevices.
Area (mm^2)	N/A	N/A	Only Schematic. No Design Rules available for PTM65.
VDD (Volt)	1.2V	N/A	

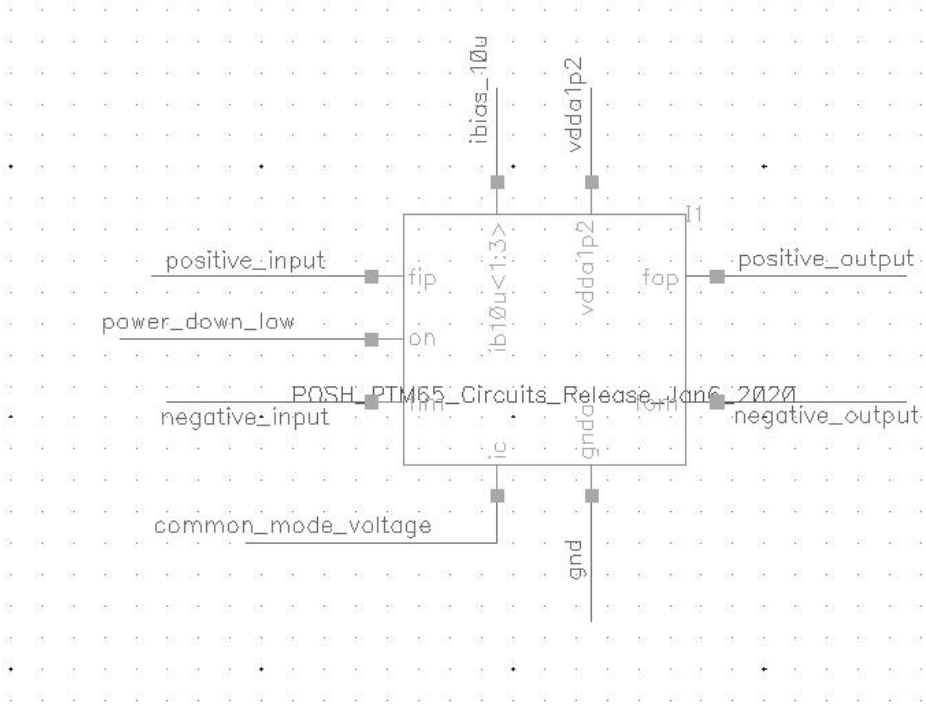
Block diagram



Cascade of three (3) differential-input, differential output opamp-based biquads to realize a six-pole 7 MHz filter. Filter has common-mode and power-down control.

Signal list

Symbol, pins and descriptions.



Signal Pins	Direction (I/O)	Type (supply, ground, analog current, analog voltage, digital voltage)	Max Voltage (core, IO or max voltage)	Specification
vdda1p2	I	Supply	Core	Power Supply, 1.2 V
Gnda	I	Ground	Core	Analog Ground
fip,fim	I	Analog voltage	Core	Differential Analog Input
fop,fom	I	Analog voltage	Core	Differential Analog Output
ic	I	Analog Voltage	Core	Common mode voltage control input
Ib10u<1:3>	I	Analog Current	Core	Bias current bus that is three wires wide.
on	I	Digital Voltage	Core	Power down active low

Design Hierarchy

Symbol, pins and descriptions.

None.

Test Bench

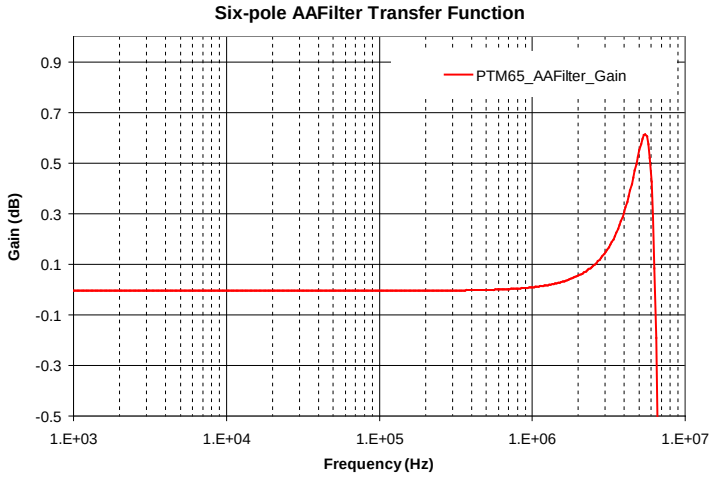
Testbench list, schematics, simulation conditions, simulation results and descriptions.

Cell Name	Note
test_aafilter_7MHz_PTM65_AllDevices	AC test for open-loop gain and phase-margin, DC operating point

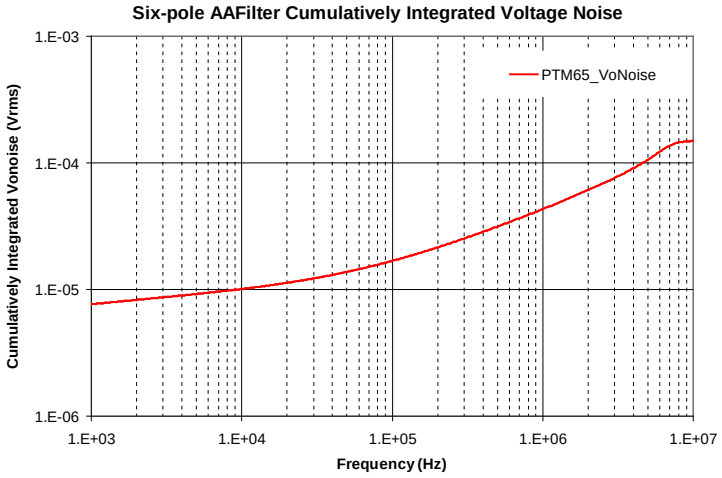
Simulations (test_aafilter_7MHz_PTM65_AllDevices):

Conditions	Values
Process corner	TT
Temperature (°C)	27
VDD (Volt)	1.2
Input amplitude	Two-tone test using 2.5 MHz and 3 MHz with amplitude 250mV
Input common mode voltage	0.6V

Open-loop gain



Cumulatively Integrated Output (Input) Noise



IM3 suppression from DFT