Changes from last revision

Date	User	Edits
1/6/2020	Prof. Levi's Design Team	USC Release of PTM65 design from GF65 design

Subsystem or block descriptions

Design name	OPAMP in PTM65nm CMOS
The Top-level cell name	Opamp5_PTM65_AllDevices
Designer	Prof. Levi's Design Team
Organization	University of Southern California

Overview

10bit linearity OPAMP. Originally designed, simulated at 39 PVT corners, fabricated and measured in GF65LPe process.

Block Specifications and Compliance

.

Spec Name	Nominal	Max	Note
Open-loop gain (dB)	76.12	N/A	PTM65 has no process corners. Simulated at available corner, 27C, Vdd=1.2V
Fu (MHz)	99.18	N/A	PTM65 has no process corners. Simulated at available corner, 27C, Vdd=1.2V
Phase Margin (degrees)	50.14	N/A	PTM65 has no process corners. Simulated at available corner, 27C, Vdd=1.2V
Power Consumption (mW)	9.82	N/A	Bias set by constant current source, see testbench called test_opamp5_PTM65_AllDevices.

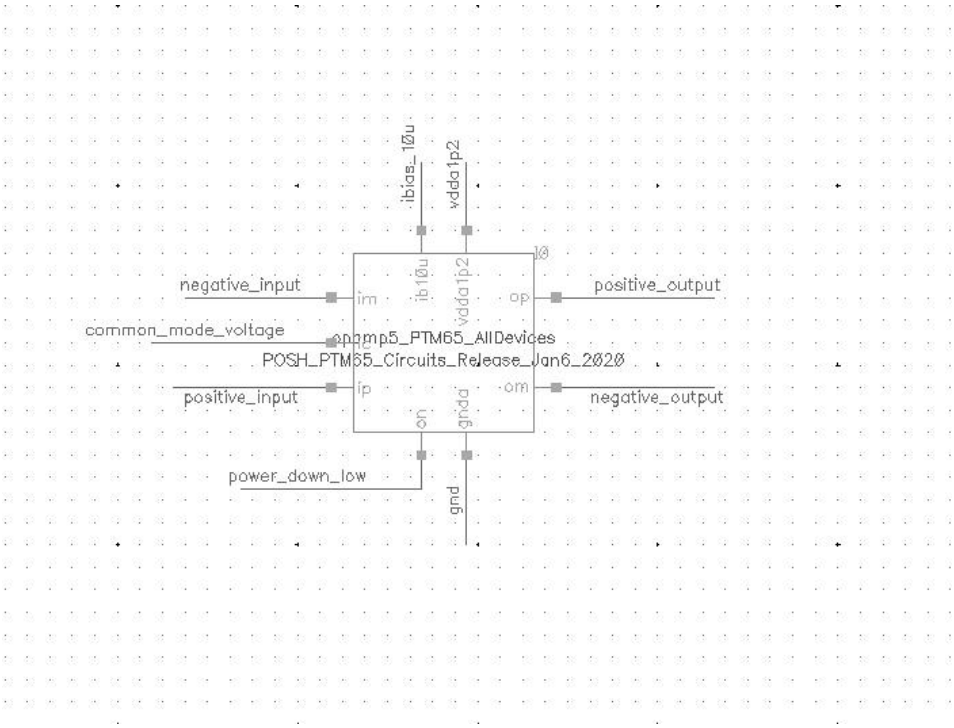
Area (mm^2)	N/A	N/A	Only Schematic. No Design Rules available for PTM65.
VDD (Volt)	1.2V	N/A	

Block diagram

Three-stage, differential-input, differential output opamp with common-mode feedback circuit. with power-down control.

Signal list

Symbol, pins and descriptions.



Signal Pins	Direction (I/O)	Type (supply, ground, analog current, analog voltage, digital voltage)	Max Voltage (core, IO or max voltage)	Specification
vdda1p2	I	Supply	Core	Power Supply, 1.2 V
Gnda	I	Ground	Core	Analog Ground
Ip,im	I	Analog voltage	Core	Differential Analog Input

Op,om	I	Analog voltage	Core	Differential Analog Output
vcm	I	Analog Voltage	Core	Common mode voltage control input
Ib10u	I	Analog Current	Core	Bias current
on	I	Digital Voltage	Core	Power down active low

Design Hierarchy

Symbol, pins and descriptions.

None.

Test Bench

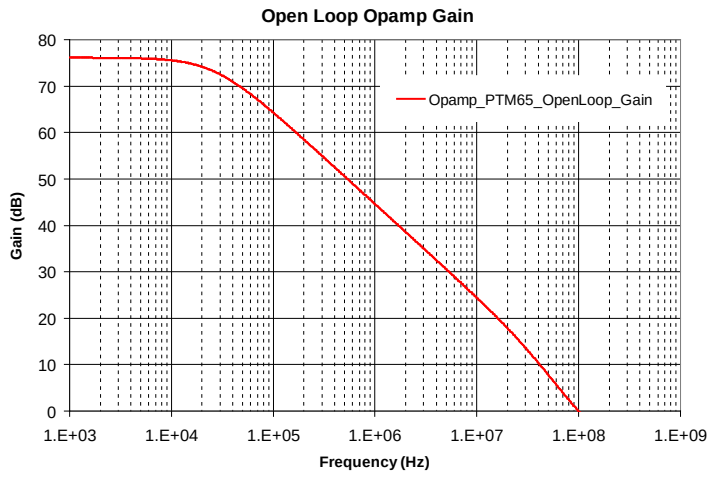
Testbench list, schematics, simulation conditions, simulation results and descriptions.

Cell Name	Note
test_opamp5_PTM65_AllDevices	AC test for open-loop gain and phase-margin, DC operating point

Simulations (test_opamp5_PTM65_AllDevices):

Conditions	Values
Process corner	TT
Temperature (°C)	27
VDD (Volt)	1.2
Input amplitude	Ac 1
Input common mode voltage	0.6V

Open-loop gain



Phase-Margin