KGD: 4-way Time-Interleaved Asynchronous SAR ADC in PTM 45nm CMOS

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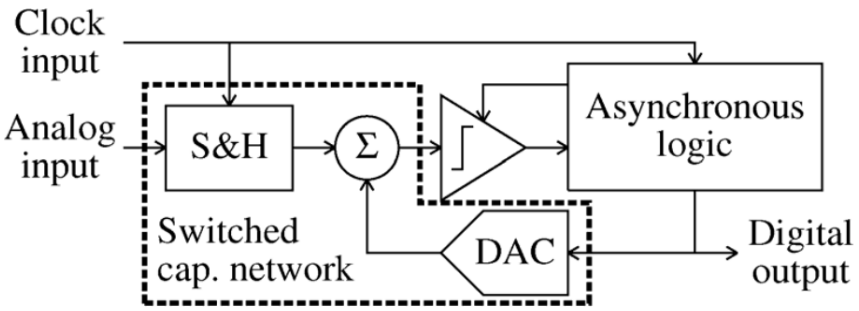
I. Introduction

In this design an 8-bit 1GS/s SAR ADC has been implemented.

SAR Architecture:



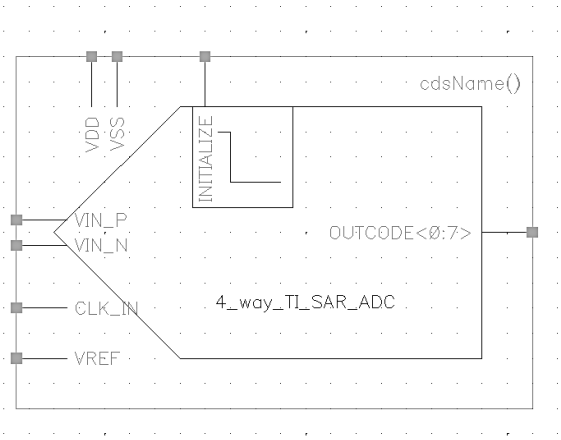
Architecture of Single SAR ADC

The major blocks in the design are:

- Clock generation
- Bootstrap sampler and Capacitive DAC
- Comparator
- SAR logic

Description:

The Top-level cell: chip_core_TI – An 8-bit 1GS/s 4-way Time-interleaved SAR ADC

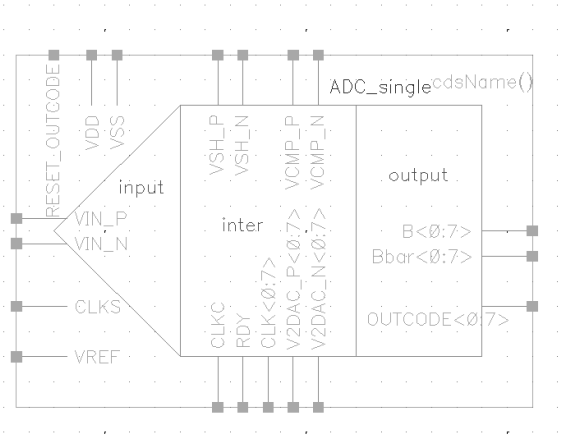


Pin Configuration:

Pin Name	Input or output	Specification

VDD	Input	Power Supply, 1.1V
VSS	Input	Ground
CLK_IN	Input	Input Clock 1GHz
VREF	Input	Reference voltage, 1V
INITIALIZE	Input	Initialize clock generation
VIN_P, VIN_N	Input	Differential input signal, common mode voltage 0.55V
OUTCODE<0:7>	output	8-bit output code

The Top-level cell: chip_core – An 8-bit 250MS/s SAR ADC

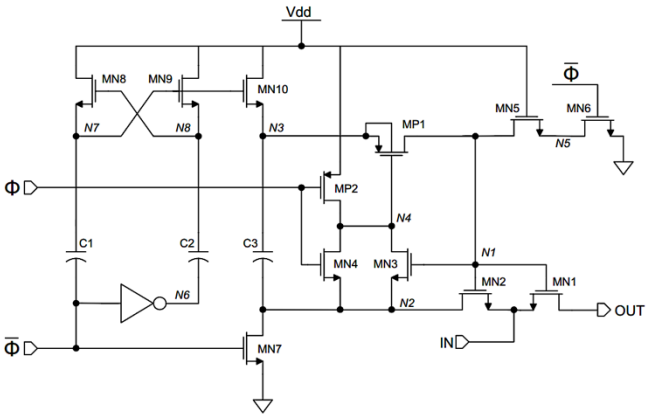


Pin Configuration:

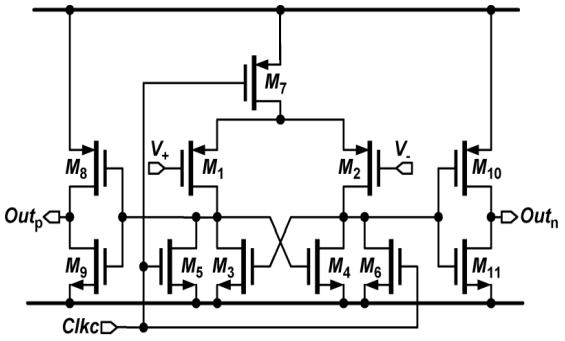
Pin Name	**Input or output**	**Specification**
VDD	Input	Power Supply, 1.1V
VSS	Input	Ground
CLK_S	Input	Input Clock 250MHz, 20% duty cycle
VREF	Input	Reference voltage, 1V
VIN_P, VIN_N	Input	Differential input signal, common mode voltage 0.55V
RESET_OUTCODE	Input	Reset output latch
OUTCODE<0:7>	output	8-bit output code

Schematic of cells

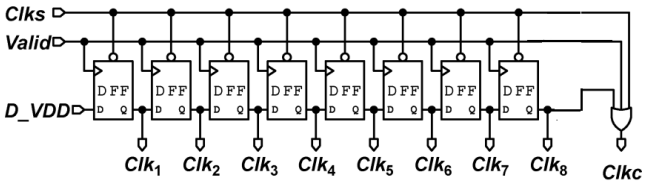
Schematic of bootstrap sampler



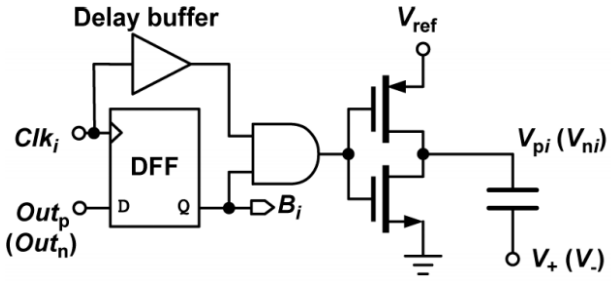
Schematic of comparator



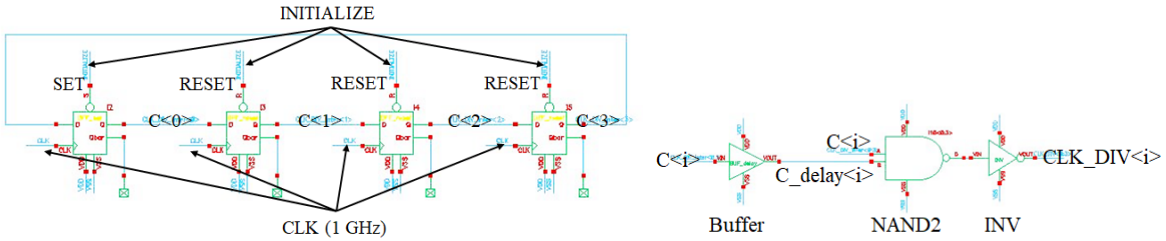
Schematic of SAR control logic



Schematic of DAC control logic



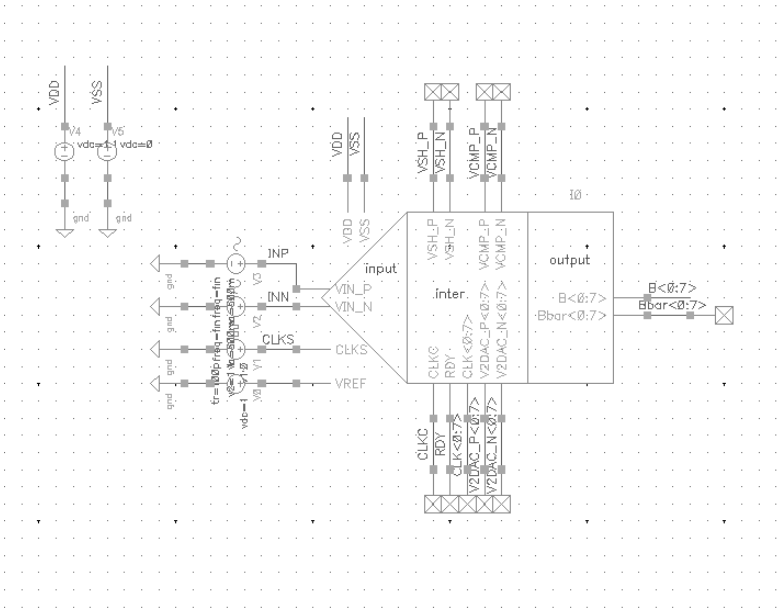
Schematic of Clock generation

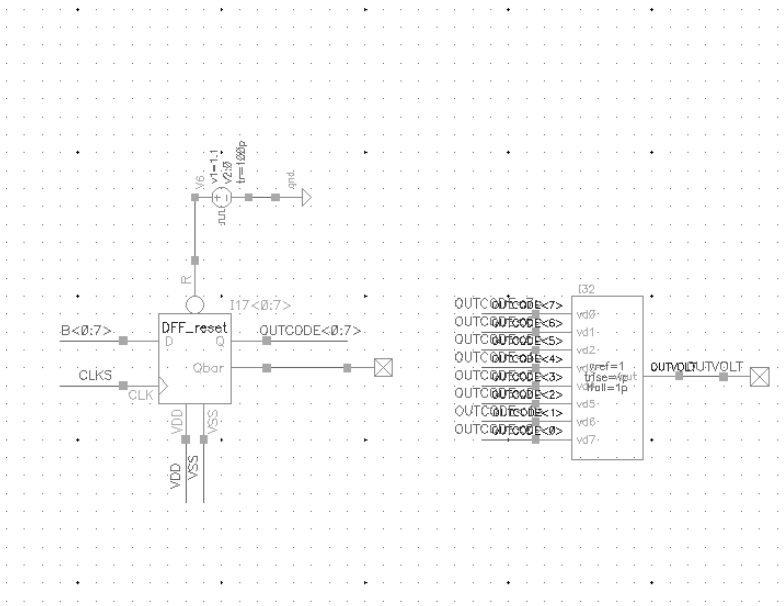


Test Bench:

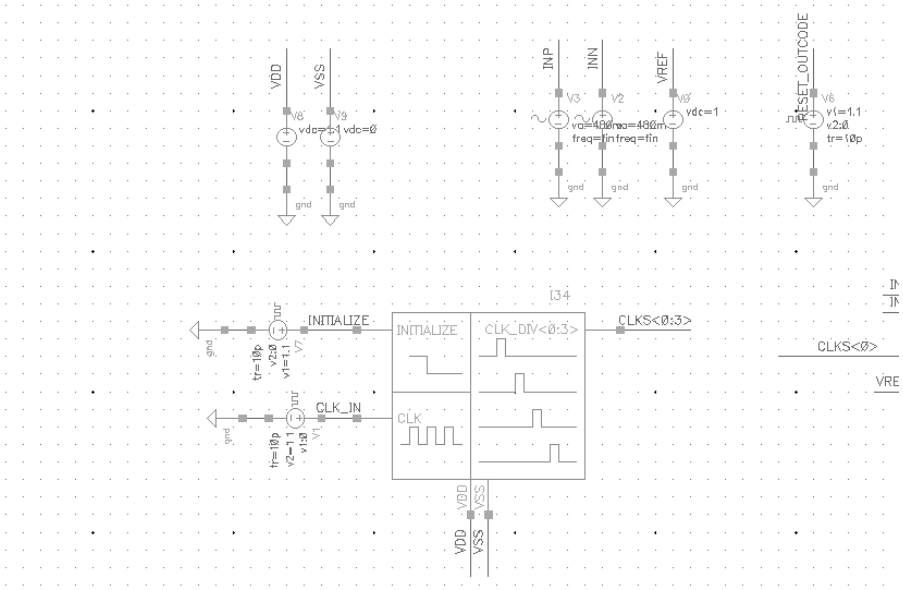
Locking time evaluation:

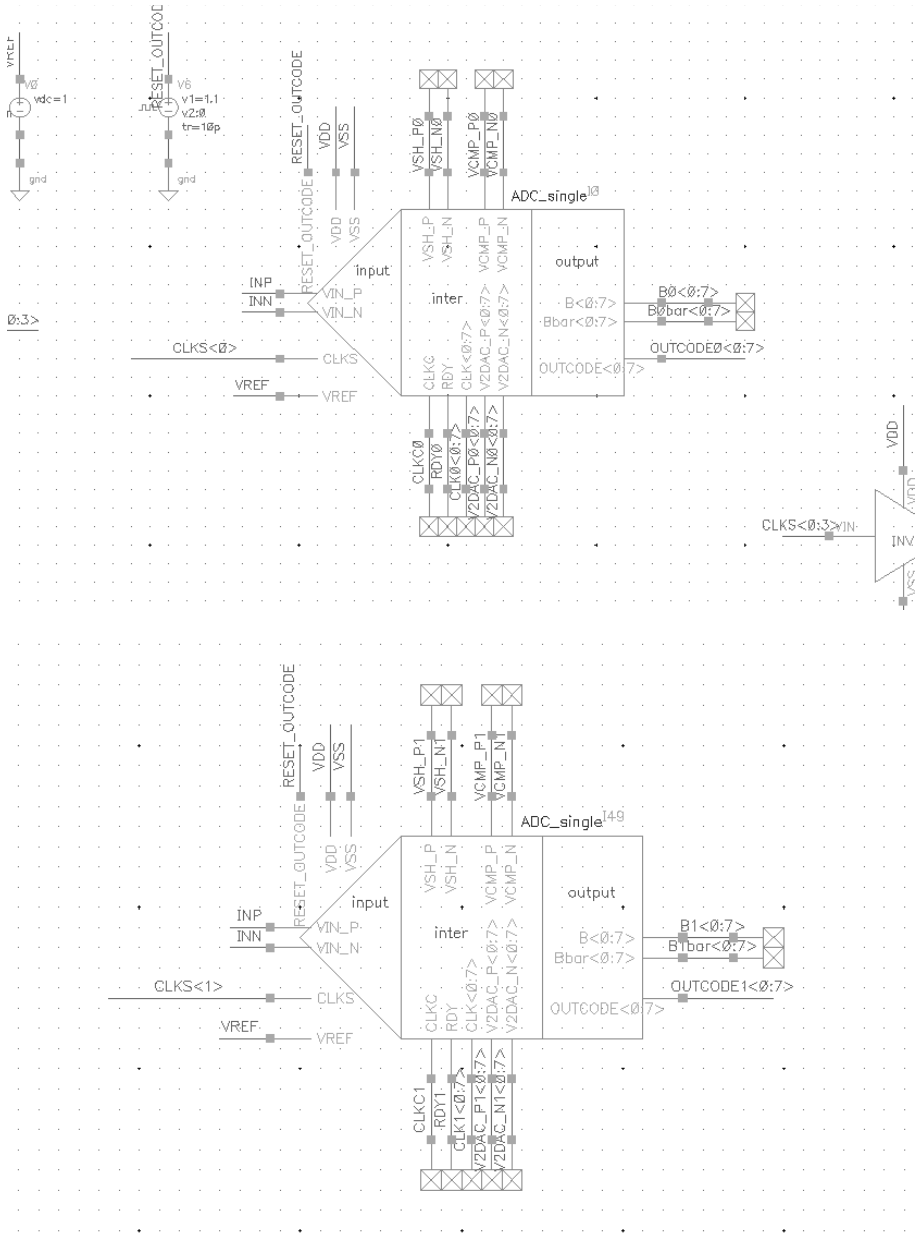
1. tb_chip_core: Testbench for single channel SAR ADC



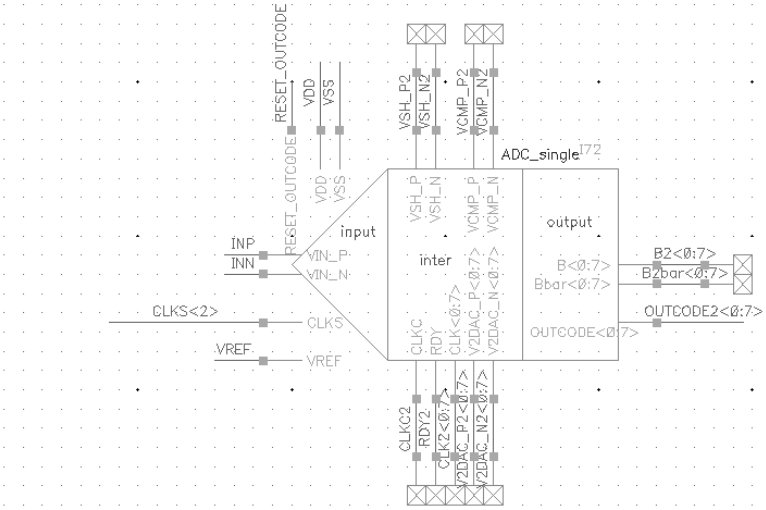


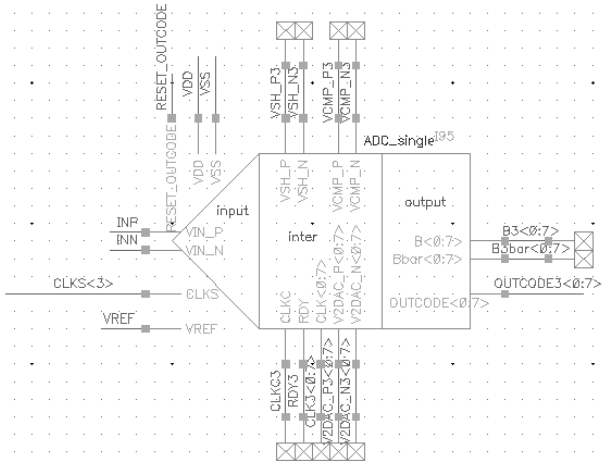
2. tb_chip_core_TI: Testbench for time-interleaved SAR ADC

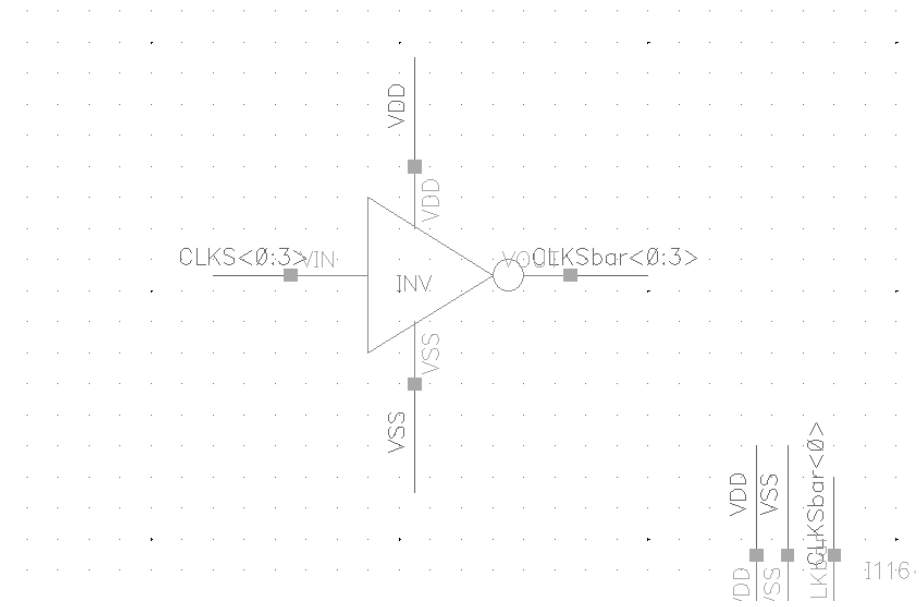


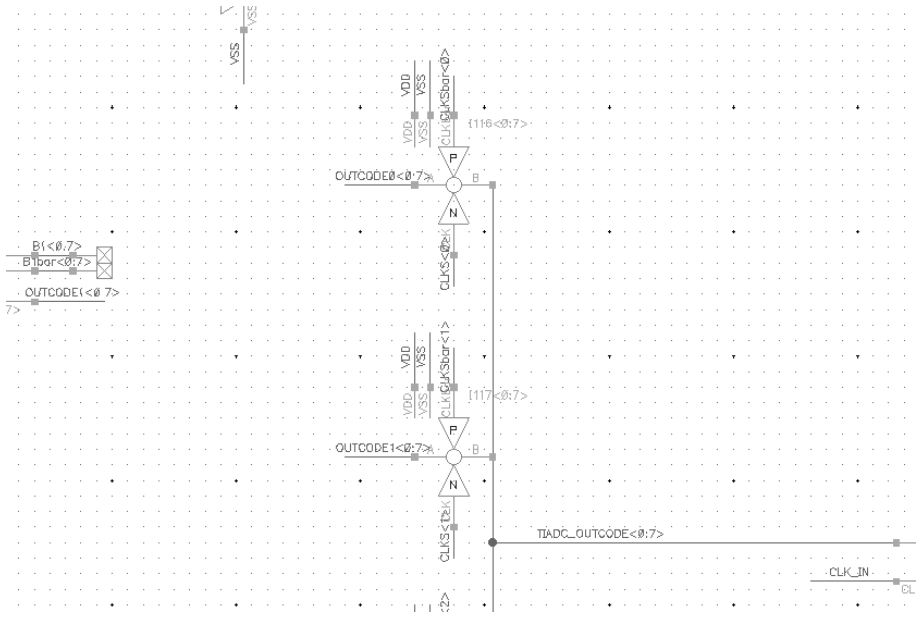

VREF
V0
vdc=1
gnd
RESET_OUTCODE
V6
v1=1.1
v2:0
tr=10p
gnd
RESET_OUTCODE
VDD
VSS
VSH_P0
VSH_N0
VCMP_P0
VCMP_N0
ADC_single I0
input
inter
output
INP
INN
VIN_P
VIN_N
CLKS<0>
CLKS
VREF
VREF
B0<0:7>
B0bar<0:7>
B<0:7>
Bbar<0:7>
OUTCODE0<0:7>
OUTCODE<0:7>
CLKC0
RDY0
CLK0<0:7>
V2DAC_P0<0:7>
V2DAC_N0<0:7>
VDD
CLKS<0:3>
VIN
INV
VSS
0:3>

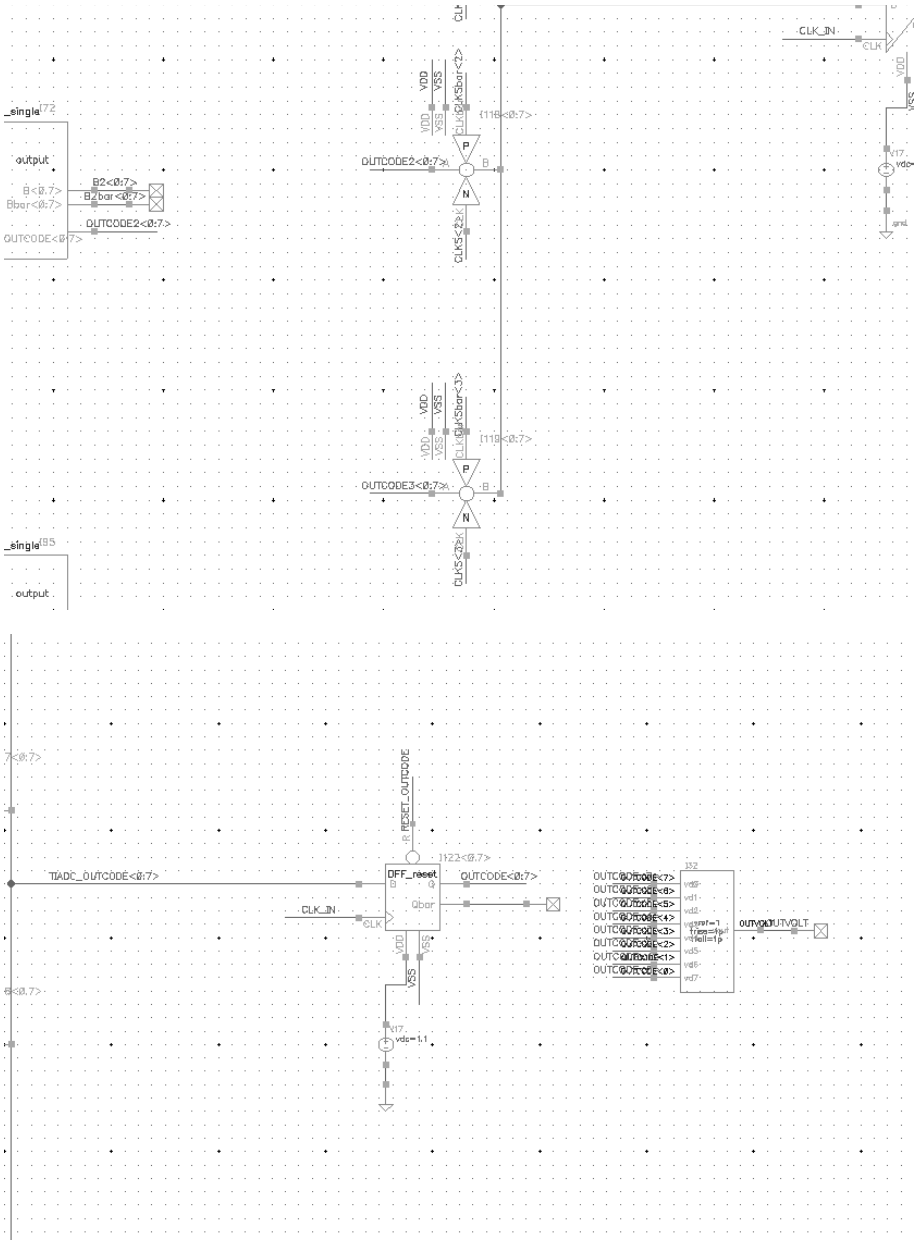
RESET_OUTCODE
VDD
VSS
VSH_P1
VSH_N1
VCMP_P1
VCMP_N1
ADC_single I4-9
input
inter
output
INP
INN
VIN_P
VIN_N
CLKS<1>
CLKS
VREF
VREF
B1<0:7>
B1bar<0:7>
B<0:7>
Bbar<0:7>
OUTCODE1<0:7>
OUTCODE<0:7>
CLKC1
RDY1
CLK1<0:7>
V2DAC_P1<0:7>
V2DAC_N1<0:7>


RESET_OUTCODE
VDD
VSS
VSH_P2
VSH_N2
VCMP_P2
VCMP_N2
ADC_single
I72
input
inter
output
INP
INN
VIN_P
VIN_N
CLKS<2>
CLKS
VREF
VREF
B2<0:7>
B2bar<0:7>
Bbar<0:7>
OUTCODE2<0:7>
CLKC2
RDY2
CLK2<0:7>
V2DAC_P2<0:7>
V2DAC_N2<0:7>
CLKC
RDY
CLK<0:7>
V2DAC_P<0:7>
V2DAC_N<0:7>
B<0:7>
OUTCODE<0:7>


RESET_OUTCODE
VDD
VSS
VSH_P3
VSH_N3
VCMP_P3
VCMP_N3
ADC_single
I95
input
inter
output
INP
INN
VIN_P
VIN_N
CLKS<3>
CLKS
VREF
VREF
B3<0:7>
B3bar<0:7>
Bbar<0:7>
OUTCODE3<0:7>
CLKC3
RDY3
CLK3<0:7>
V2DAC_P3<0:7>
V2DAC_N3<0:7>
CLKC
RDY
CLK<0:7>
V2DAC_P<0:7>
V2DAC_N<0:7>
B<0:7>
OUTCODE<0:7>


VDD
VDD
CLKS<Ø:3>
IN
INV
CLKSbar<Ø:3>
VSS
VSS
VDD
VSS
CLKSbar<Ø>
I116

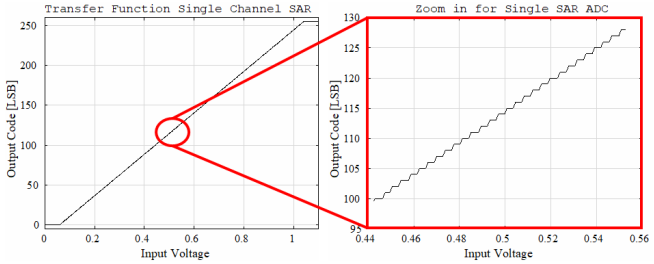

VSS
VDD
VSS
CLKSbar<Ø>
I116<Ø:7>
P
OUTCODE0<Ø:7>
B
N
CLKS<Ø>
B<Ø:7>
Bbar<Ø:7>
OUTCODE<Ø:7>
VDD
VSS
CLKSbar<1>
I117<Ø:7>
P
OUTCODE1<Ø:7>
B
N
TIADC_OUTCODE<Ø:7>
CLK_IN



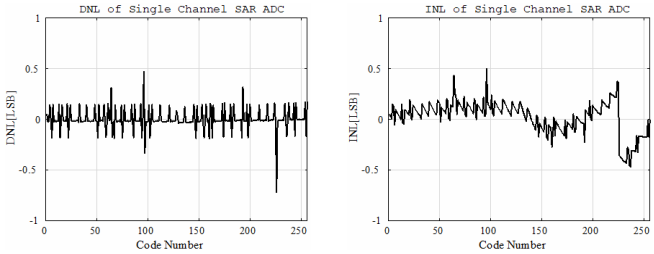
Simulation Results:

Single ADC

Single ADC Static Test:

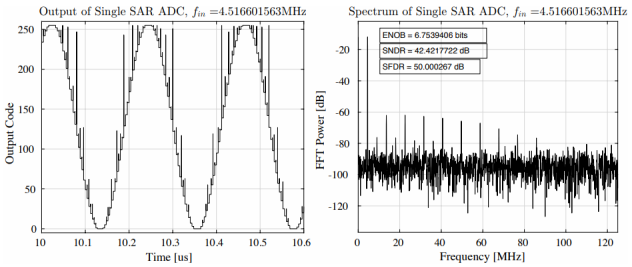


Ramp signal test

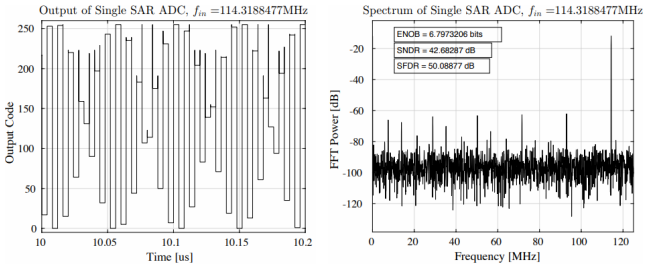


DNL INL

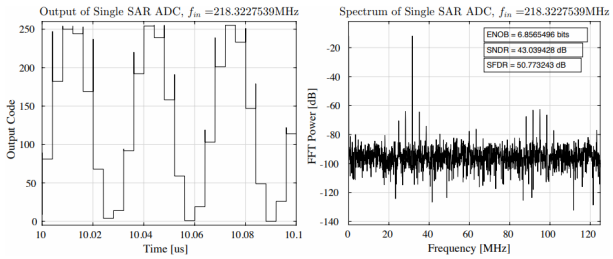
Single ADC Dynamic Tests:



Output Spectrum

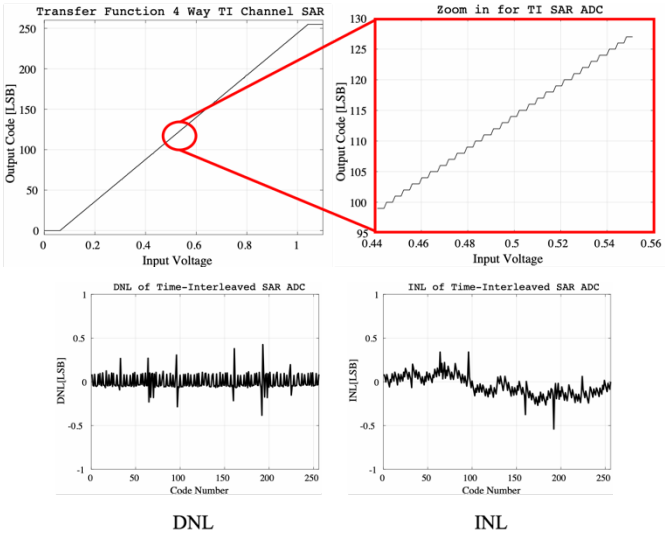


Output Spectrum



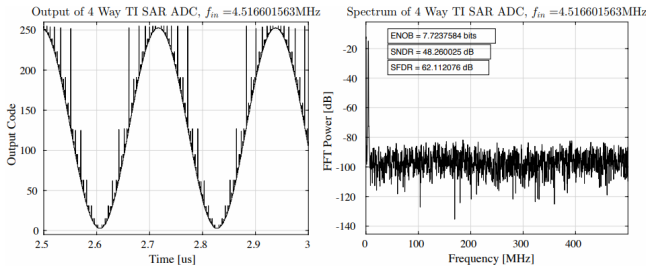
Output Spectrum

Time Interleaved ADC static test

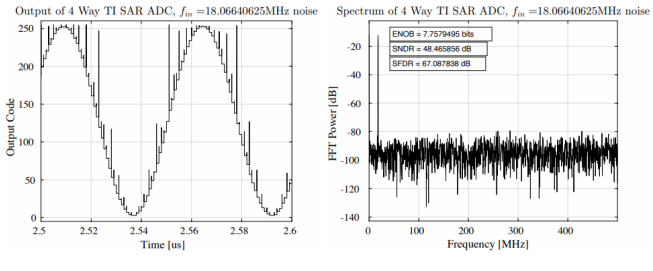


DNL INL

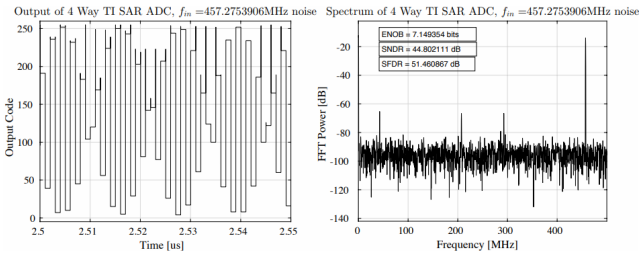
Time Interleaved ADC Dynamic Tests:



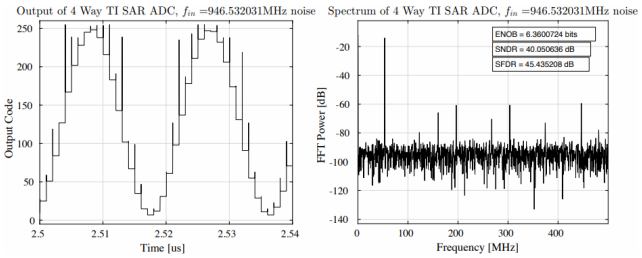
Output Spectrum



Output Spectrum



Output Spectrum



Output Spectrum

Performance summary

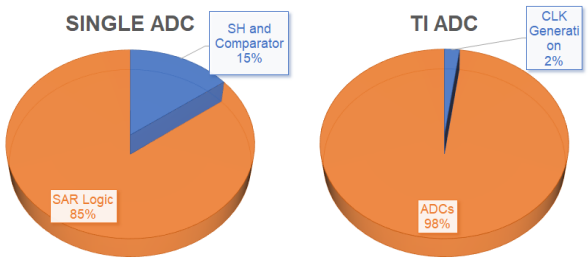
Single ADC

Specifications	f_{in} = 4.52 MHz	f_{in} = 114.32 MHz
Resolution [bit]	8	8
Sampling Rate [MS/s]	250	250
Input Swing [mV]	1000	1000
ENOB [bit]	6.75	6.80
SNDR [dB]	42.42	42.68
SFDR [dB]	50.00	50.09
Power [mW]	50.6	50.8
FoM [pJ/conv-step]	1.88	1.82

Time interleaved ADC

Specifications	f_{in} = 4.52 MHz	f_{in} = 18.07 MHz	f_{in} = 457.28 MHz
Resolution [bit]	8	8	8
Sampling Rate [GS/s]	1	1	1
Input Swing [mV]	1000	1000	1000
ENOB [bit]	7.72	7.75	7.15
SNDR [dB]	48.26	48.47	44.80
SFDR [dB]	62.11	67.09	51.46
Power [mW]	254.6	255.0	254.8
FoM [pJ/conv-step]	1.21	1.18	1.79

Power breakdown


SINGLE ADC
SH and Comparator 15%
SAR Logic 85%
TI ADC
CLK Generation 2%
ADCs 98%