KGD: Asynchronous SAR ADC in PTM

I. Introduction

In this design a 2-GS/s / 6-bit SAR ADC has been implemented. ADC is a commonly used design block for converting analog signal into digital domain. The block diagram representation of the design is as follows:

ADC Architecture:

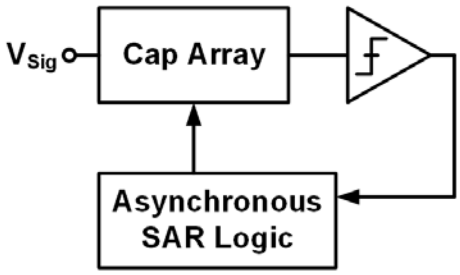


Figure 1: Architecture of Known Good Design (KGD) of SAR ADC

The major blocks in the design are:

- Track-and-hold network
- Comparator
- SAR logic / Clock generator

Description:

The Top-level cell: Asynch_SAR_ADC_6b2GSPS – A 2GHz / 6-bit SAR ADC.

Pin Configuration:

Pin Name	Specification
VDD	Power Supply, 0.8V
VSS	Ground
CLK	Sampling clock 2GHz
REFP/REFN	Reference voltage
IP/IN	Analog Input < 1GHz
DOUT<5:0>	6-bit Digital output

The input pins are: CLK (Sampling Clock), VDD (Power Supply), VSS (ground), REFP/REFN (Differential reference voltage), and IP/IN (Analog differential Input signal). The output pins are DOUT<5:0> binary digital output.

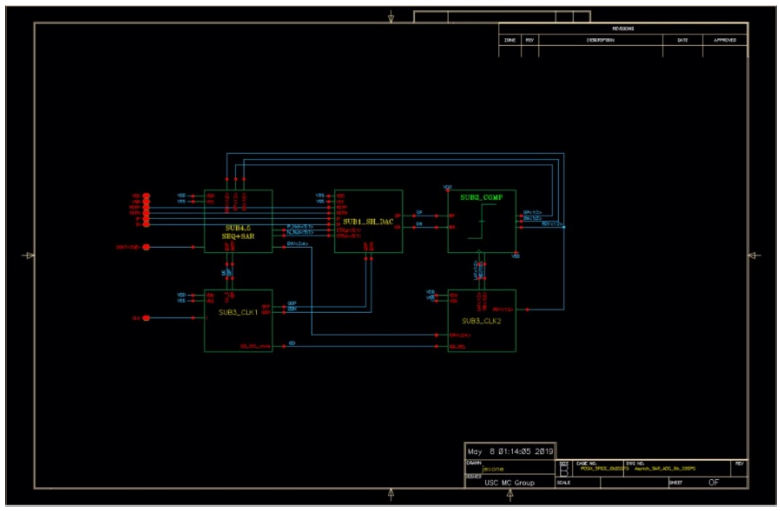
Description of the Cell Library:

The tabular description below corresponds to the structure of the design library as seen in Cadence.

#	Category	CellName	Description
1	TOP_CELL	Asynch_SAR_ADC_6b2GSPS	6-bit 2GS/s SAR ADC
		SUB1_CDAC_6b_diff	Track-and-Hold sampling network

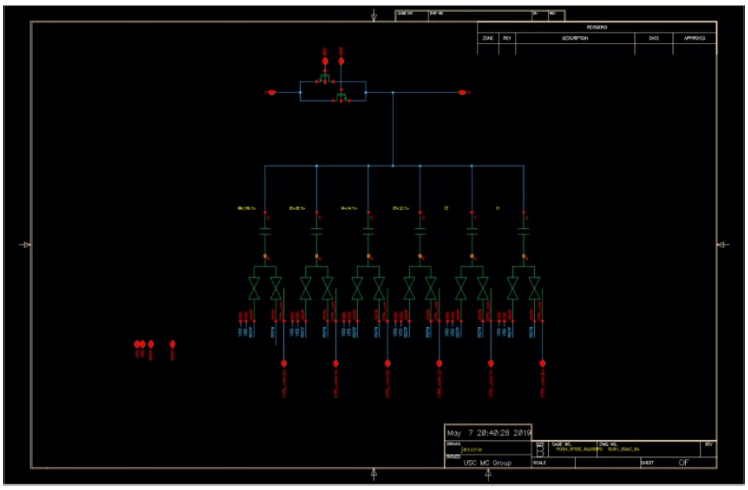
		SUB2_COMP_DUPLEX	Dual comparator pair
		SUB3_CLK1	Master clock generator (Sampling / conversion)
		SUB3_CLK2	Asynchronous clock generator
		SUB5_SEQ_TOP_6b_v2	Sequential State machine and Bit Cache
2	SUB1_SH_DAC	SUB1_CDAC_6b	Single-ended Top-plate sampling network 6b
		SUB1_CDAC_SW	Reference switch + Unit capacitor
3	SUB2_COMP	SUB2_COMP_DynamicAMP	1st Stage comparator (Gain stage)
		SUB2_COMP_DynamicLAT	2nd stage comparator (Latch)
		SUB2_RDYgen	Ready-signal generator
4	SUB3_CLK_GEN	SUB3_CLK1	Master clock generator (Sampling / conversion)
		SUB3_CLK2	Asynchronous clock generator
5	SUB4_SAR_LOGIC	SUB4_SAR_TOP	SAR logic top
		SUB4_SAR2_DFF	DFF for SAR Logic to drive ref. switch
		SUB4_SAR3	DFF for SAR Logic for the last digital output
6	SUB5_SEQ	SUB5_SEQ_6b	Sequencer for 6bit SAR

The complete schematic of the design is:

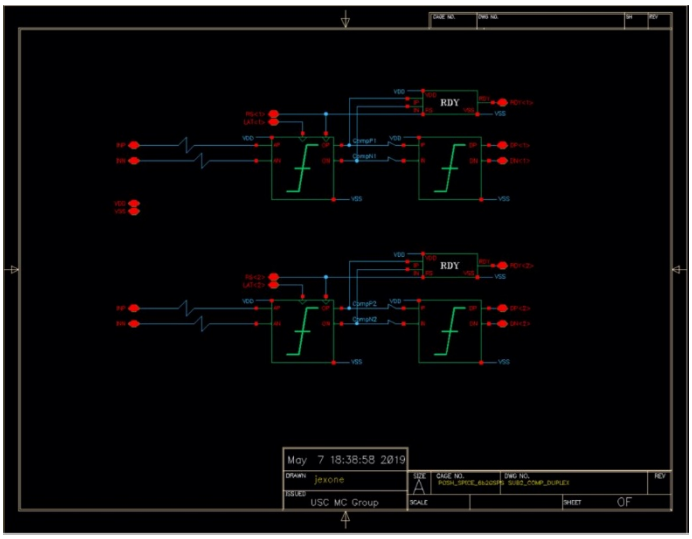


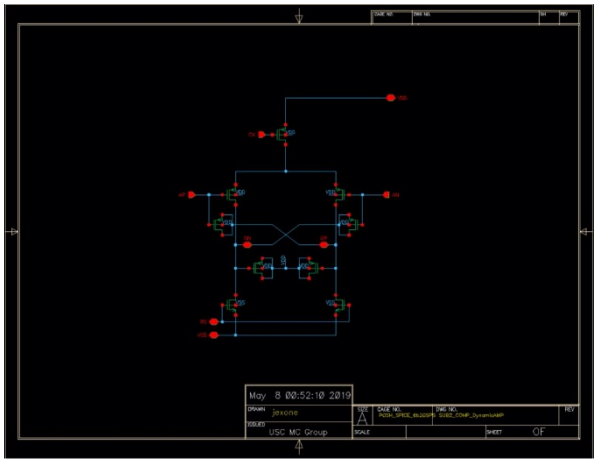
The schematic of the modules are as follows:

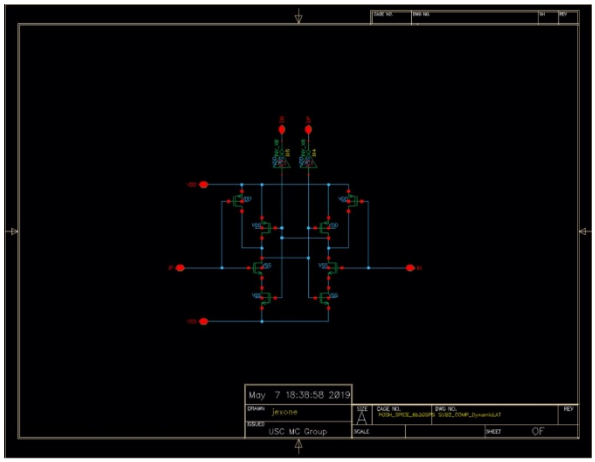
Track-and-hold network:



Dual comparator:

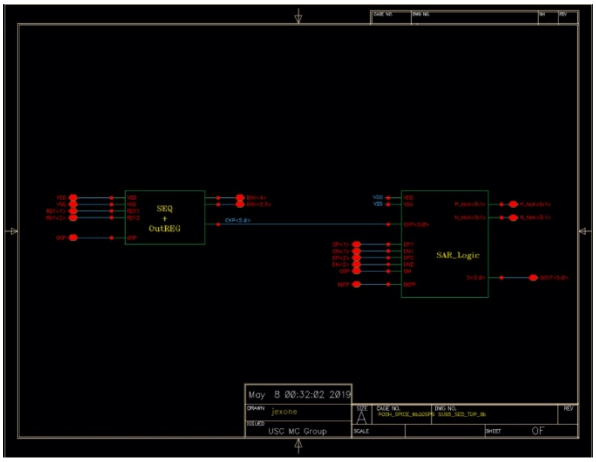


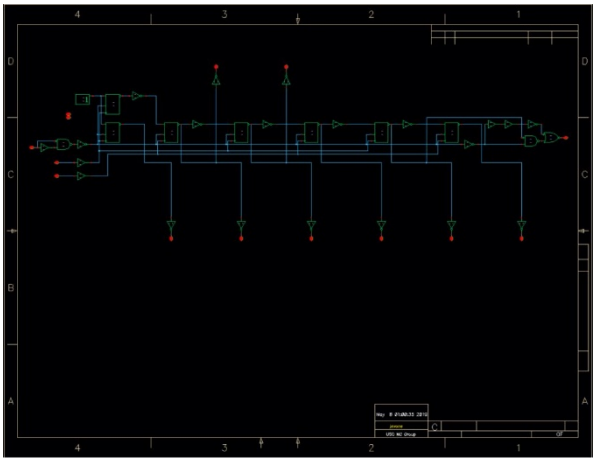




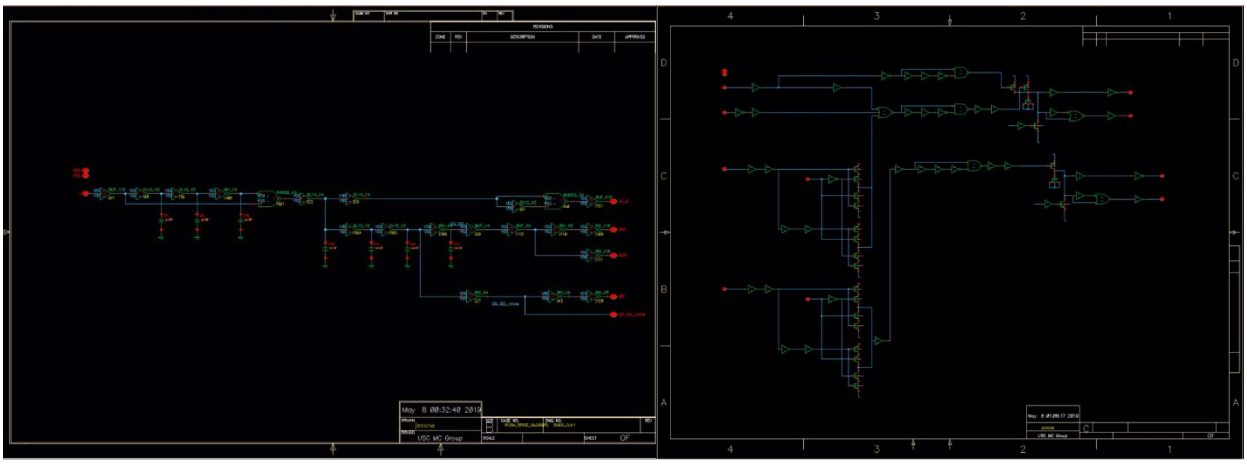
1st and 2nd stage comparator

Sequencer and SAR Logic:





Clock generator / Asynch. Clocking circuit:

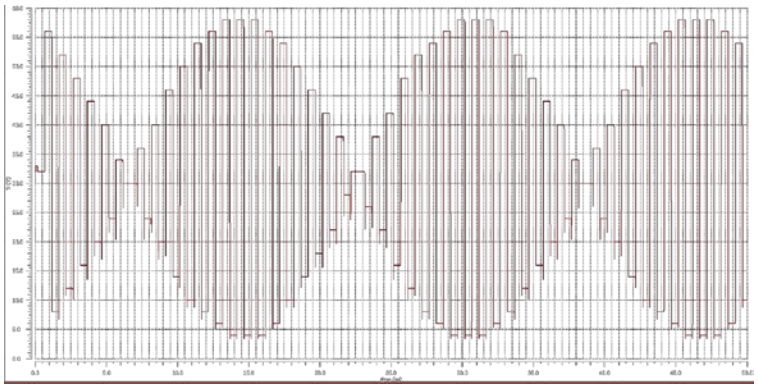


Test Bench:

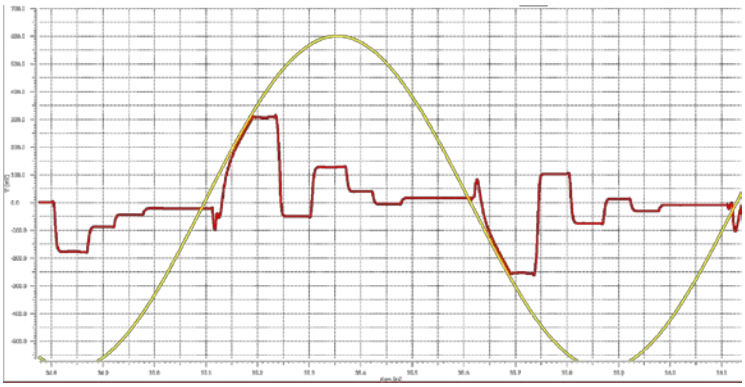
Dynamic performance evaluation with Sinusoidal input:

Testbench for ADC dynamic performance using transient analysis.

Simulation Results: Power dissipation: 560uW



Transient waveform with Nyquist input frequency



Transient waveform with Nyquist input frequency (Red: SAR Residue / Yellow: Input signal)