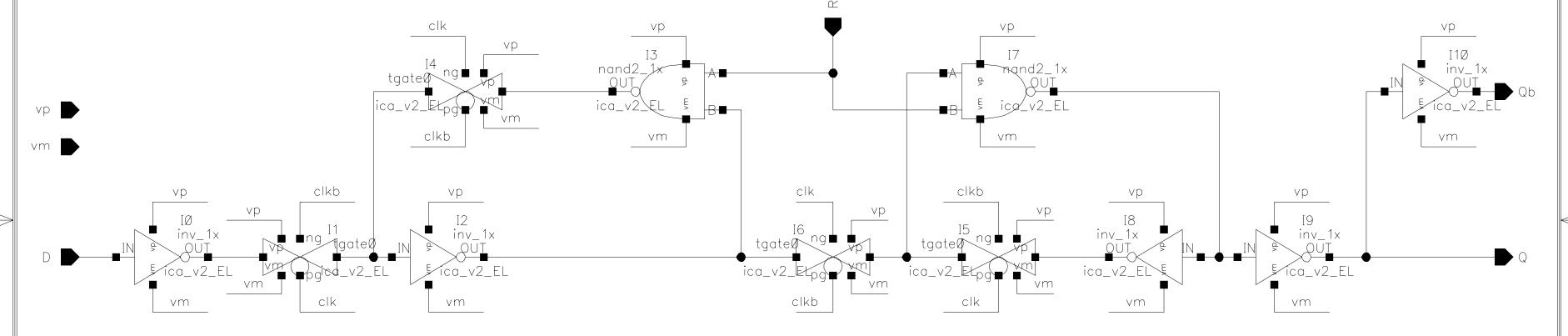
$\overline{}$												
REVISIONS												
ZONE	REV	DESCRIPTION			DATE	APPROVED						

Asynchronous RN sets Q=logic "Ø" NEED clock to be HIGH TO hold this value!!

flip I4 sideways to interchange "a" and "b" terminals



CK III II2 II2 inv_1x oUT clkb IN Sica_v2_EL vm vm

Interchange I5 and I6, then flip each sideways to interchange "a" and "b" inputs.

UPDATED					
Dec 17 Ø8:Ø2:32 2Ø18					
DRAWN		\bigcirc f f $_{\Gamma}$			
CHECKED					
CHECKED	SIZE CAGE NO.	DWG NO.			REV
ISSUED	SCALE		SHEET	OF	