12 bit SAR ADC Schematic Parallel outputs PO<11:0> ready of Output = (1-2*PO<11>)*(2~10*PO	ofter sync falling	approved edge Ø*PO<Ø>)
12bit SAR ADC Schematic Parallel outputs P0<11:0> ready or Output = (1-2*P0<11>)*(2~10*P0		
Parallel outputs PO<11:∅> ready a: Output = (1-2*PO<11>)*(2~1∅*PO	ıfter sync falling O<10>+ + 2~	edge Ø*P0<Ø>)
d d d d d d d d d d d d d d d d d d d	ıfter sync falling)<10>+ + 2~	edge Ø*P0<Ø>)
sericl output (ADCo) starts after He WS3 out first, LSB out last MS3 (ADCo<11> = 3 ngstive number - ADCo<11> = 2 ngstive number Output = (2*ADCo<11> -1)*{2^10}*2^10}*2^10**(1-ADCo<10>)*(1-ADCo<10>)1}* Page Page	I3 I4 inv_1x out Fica_v2_EL Fica_	dp
Dec 17 Ø7:54:1Ø 2Ø18 AU		
DRAWN CHECKED		
CHECKED SIZE CAGE NO. DWG NO.		REV
ISSUED	0	
SCALE	SHEET	<u>OF</u>