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**USC\_65nm\_Release\_Dec20\_2018**

1. User is required to have Cadence IC615 or later to read the schematics.
2. User needs the standard libraries that are distributed by Cadence to read the schematics (US\_8ths, basic, analogLib, functional, cdsDefTechLib)
3. User needs the 65nm technology libraries in order to be able to see the device symbols and properties. This requires an NDA between the user and Global Foundries, which is the responsibility of the user.
4. The 65nm library has technology properties for the selected metal stack option of **6\_00\_01\_00\_LB**, whose meaning is defined in the PDK to be obtained under NDA. The libraries and design are valid at PDK version V1.6.0 (Rev 11). The user is advised that selecting a different metal-stack option for tapeout will require the above variable to be changed. At the schematic level, this will affect the metal-oxide-metal capacitors used in the designs.
5. Simulation testbenches are provided for toplevel cells.
6. Simulation is using adexl and Spectre. Adexl views and Spectre states are provided.
7. Layout cells are not provided at this time.
8. The library has three top-level cells – ADC12b (twelve bit SAR ADC), aafilter\_vncap\_7MHz (differential input, differential output, six-pole anti-aliasing Butterworth filter) and opamp5 (general purpose differential input, differential output opamp). Layout cells will be provided to the user under NDA for these cells. A separate design schematic called aafilter\_vncap\_2p2MHz is provided to the interested reader to create a layout from the aafilter\_vncap\_7MHz layout as a learning exercise for the CAD flow (DRC, LVS and simulation after parasitic extraction).
9. Design Corners: Process Corners, -55C to 125C, Vdd nominal +/- 10%
   1. **Toplevel cell 1: ADC12b:**

12-bit, 20.4 MS/s SAR ADC with 285.714 MHz sampling clock (3.5ns period)

ADC has 12-bit parallel output as well as serial output.

**Typical Current consumption specifications from 1.2V supply at room temperature:**

Analog circuit current consumption: 484uA

Digital circuit current consumption: 93uA

Current consumption from 1.2V reference input: 386uA

Output I/O circuits for parallel outputs (10pF load on each output): 1.024mA

Total current consumption excluding I/O circuits: 963uA

**ADC Parallel output specification:**

Parallel outputs PO<11:0> ready after sync falling edge

Output = (1-2\*PO<11>)\*(2^10\*PO<10>+ ... + 2^0\*PO<0>)

**ADC Serial output specifications:**

serial output (ADCo) starts after signal “Ho” goes high.

MSB out first, LSB out last

MSB (ADCo<11>) = sign bit

- ADCo<11> = 1 positive number

- ADCo<11> = 0 negative number

Output = (2\*ADCo<11>-1)\*{2^10\*[ADCo<11>\*ADCo<10>+(1-ADCo<11>)\*(1-ADCo<10>)]+ …. + 2^0\*[ADCo<11>\*ADCo<0>+(1-ADCo<11>)\*(1-ADCo<0>)]}

**TestBenches:**

1. test\_ADC12b
2. test\_ADC12b\_sin: Testbench with 2 equal amplitude sine wave inputs at 2.551MHz and 3.827MHz.
3. Test\_comp2: Testbench for comparator resolution simulation using transient analysis
4. Test\_comp2\_ac: Testbench for comparator pre-amp gain and noise analyses
   1. **Toplevel cell 2: aafilter\_vncap\_7MHz**

Differential input, Differential output six-pole filter with nominal bandwidth of 7.143 MHz and min bandwidth > 4.6875 MHz across corners.

Fiilter is composed of three, cascaded two-pole biquad filter sections. Filter sections can be turned off by connecting the “on” input to ground instead of 1.2V.

**TestBenches:**

* + 1. test2\_aafilter\_vncap TestBench for aafilter\_vncap\_7MHz RminCmin and RmaxCmax corner testing
    2. test2\_power\_aafilter\_vncap TestBench for aafilter\_vncap\_7MHz
    3. test2\_aafilter\_mc Monte Carlo TestBench for aafilter\_vncap\_7MHz
    4. test2\_aafilter\_vncap TestBench for aafilter\_vncap\_7MHz
    5. test2\_aafilter\_vncap\_off TestBench for checking effect of offset in aafilter\_vncap\_7MHz
    6. opamp5 Schematic of opamp5 used in aafilter\_vncap\_7MHz
  1. **opamp5**

Differential input, differential output opamp with required GBW for biquad sections used in filter.

**TestBenches:**

1. test\_opamp5 TestBench for opamp5

The tabular description below corresponds to the structure of the design library as seen in Cadence. The “/” character indicates a subcategory under the category preceding the “/” character.

|  |  |  |  |
| --- | --- | --- | --- |
| **#** | Category | **CellName** | **Description** |
| 1 | ADC12b | ADC12b | 12-bit, 20.4MS/s SAR ADC |
|  |  | Shf\_line | Used by sarlogic2 cell in ADC12b |
|  |  | sarc | Used by sarlogic2 cell in ADC12b |
|  |  | comp2 | Comparator cell used in ADC12b |
|  |  | DAC\_array | DAC cell used in ADC12b |
|  | ADC12b/ADC\_TestBenches | test\_ADC12b | Testbench for ADC12b |
|  |  | test\_ADC12b\_sin | Testbench for ADC12b with 2.551 MHz sin wave input |
|  |  | test\_comp2 | Testbench for comparator used in ADC12b |
| 2 | Analog\_Biasing | Selfbias | Biascircuit used for biasing aafilter cell. |
| 3 | DAC\_Cells | DAC\_array | Segmented resistor-capacitor DAC used in ADC12b |
|  |  | R\_array2 | Resistive DAC segment |
|  |  | cap\_array5 | Capacitive array DAC segment |
|  |  | R\_cell3 | Basic unit cell of R\_array2 |
|  |  | cap\_cell | Basic unit cell of cap\_array5 |
|  |  | cap\_cell2 | Basic unit cell of cap\_array5 |
|  |  | cap\_cell\_dummy | Basic dummy cell of cap\_array5 |
|  |  | cap\_cell\_dummy2 | Basic dummy cell of cap\_array5 |
|  |  | cap\_cell\_tr | Basic unit cell of cap\_array5 |
| 4 | Digital Cells | dffr | DFF with reset |
|  |  | diffs | DFF with set |
|  |  | Inv\_1x | 1x strength inverter |
|  |  | Inv\_4x | 4x strength inverter |
|  |  | Inv\_8x | 8x strength inverter |
|  |  | Inv\_32x | 32x strength inverter |
|  |  | nor2\_1x | 1x strength nor2 gate |
|  |  | nor2\_4x | 4x strength nor2 gate |
|  |  | nor3\_1x | 1x strength nor3 gate |
|  |  | tgate0 | Transmission gate |
|  |  | tate1 | Transmission gate |
|  |  | tgate1R\_2p5u | Transmission gate |
|  |  | tgate1R\_p5u | Transmission gate |
|  |  | tgate2 | Transmission gate |
|  |  | tgateL | Transmission gate |
|  |  | tgateL1p5R | Transmission gate |
|  |  | tgateL1p25R | Transmission gate |
| 5 | Filter | aafilter\_vncap\_7MHz | Anti aliasing Butterworth filter with 7MHz nominal bandwidth, min BW across PVT > 4.6875 MHz and < 10.2 MHz across thirty-nine corners.This design has a measured bandwidth of 6.5 MHz and measured 01. dB compression point of 4.5 MHz. 1 dB compression point was not found in measurements. Filter matching across four filters on the same die was measured to be +/-  = +/- 0.0291 dB (+/- 0.67%)  in the frequency range 0.1 MHz to 7 MHz and  +/-  = +/- 0.0198 dB (+/- 0.46%).  Simulated linearity between –63dB and –72.35dB across thirty nine corners for failure rate target of 4 PPM. |
|  |  | bq1\_vncap\_7MHz | First biquad 2-pole filter section |
|  |  | bq2\_vncap\_7MHz | Second biquad 2-pole filter section |
|  |  | bq3\_vncap\_7MHz | Third biquad 2-pole filter section |
|  | Filters/Filter\_TestBenches | test2\_aafilter\_vncap | TestBench for aafilter\_vncap\_7MHz RminCmin and RmaxCmax corner testing |
|  |  | test2\_power\_aafilter\_vncap | TestBench for aafilter\_vncap\_7MHz |
|  |  | test2\_aafilter\_mc | Monte Carlo TestBench for aafilter\_vncap\_7MHz |
|  |  | test2\_aafilter\_vncap | TestBench for aafilter\_vncap\_7MHz |
|  |  | test2\_aafilter\_vncap\_off | TestBench for checking effect of offset in aafilter\_vncap\_7MHz |
| 6 | Opamps | opamp5 | Schematic of opamp5 used in aafilter\_vncap\_7MHz |
|  | Opamps/Opamp\_TestBench | test\_opamp5 | TestBench for opamp5 |