**KGD: DLL in GF 65nm**

1. **Introduction**

In this design a 2-GS/s / 8-phase DLL has been implemented. DLL is a commonly used design block for generating multi-phase clock signal for the system. The block diagram representation of the design is as follows:

**ADC Architecture:**

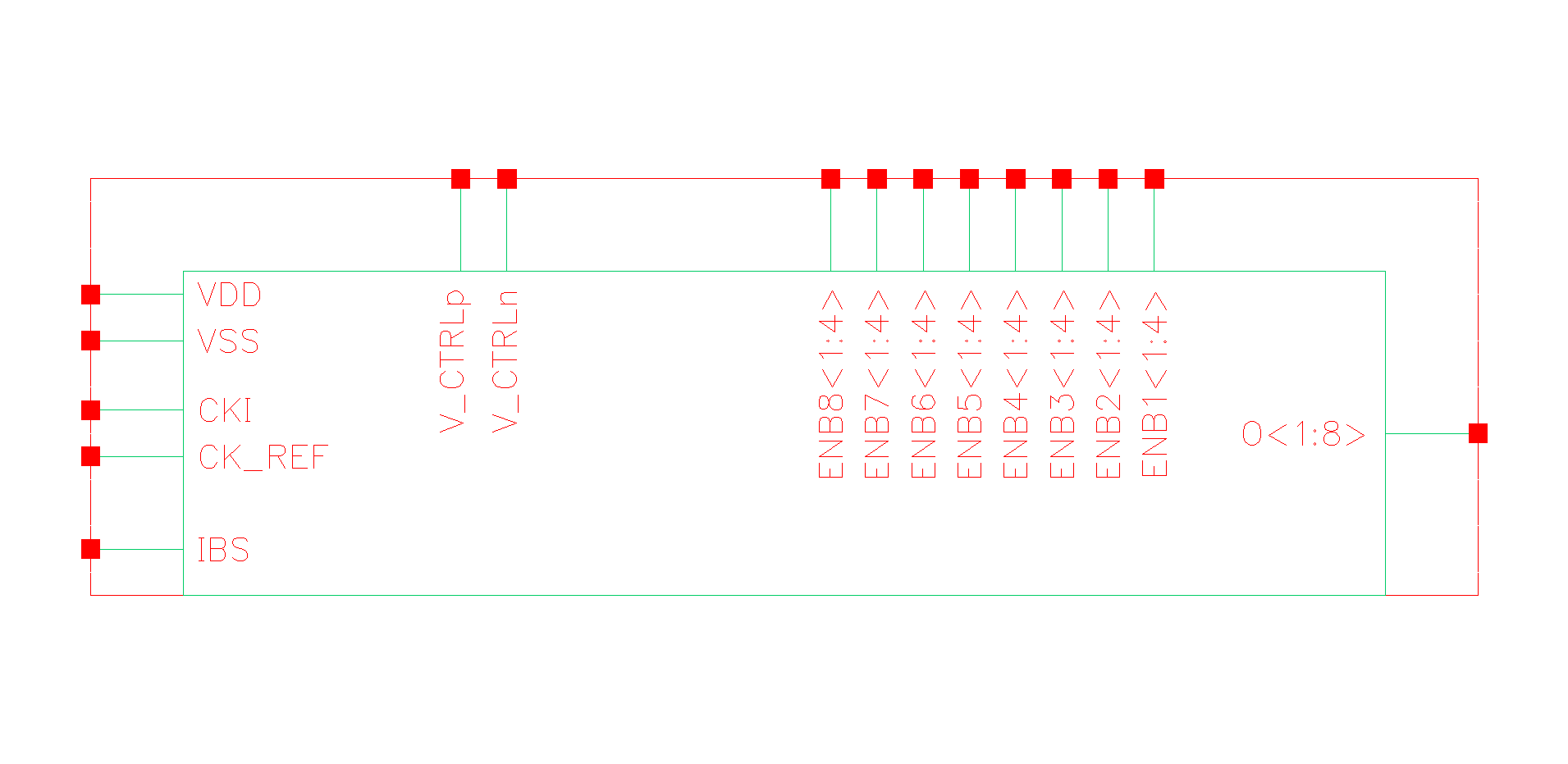


Figure 1: Architecture of Known Good Design (KGD) of DLL

The major blocks in the design are:

* Phase Detector
* Charge Pump
* Voltage Controlled Delay Line

**Description:**



**The Top-level cell:** DLL\_core – A 2GHz / 8-phase / 100fsec\_rms jitter DLL.

Pin Configuration:

|  |  |
| --- | --- |
| **Pin Name** | **Specification** |
| VDD | Power Supply, 0.9V – 1.1V |
| VSS | Ground |
| CKI | Input Clock ~2Ghz |
| IBS | Biasing current ~20uA |
| O<1:8> | 8 phase clock output |
| ENBX<1:4> | Delay fine tuning (0, VDD) |

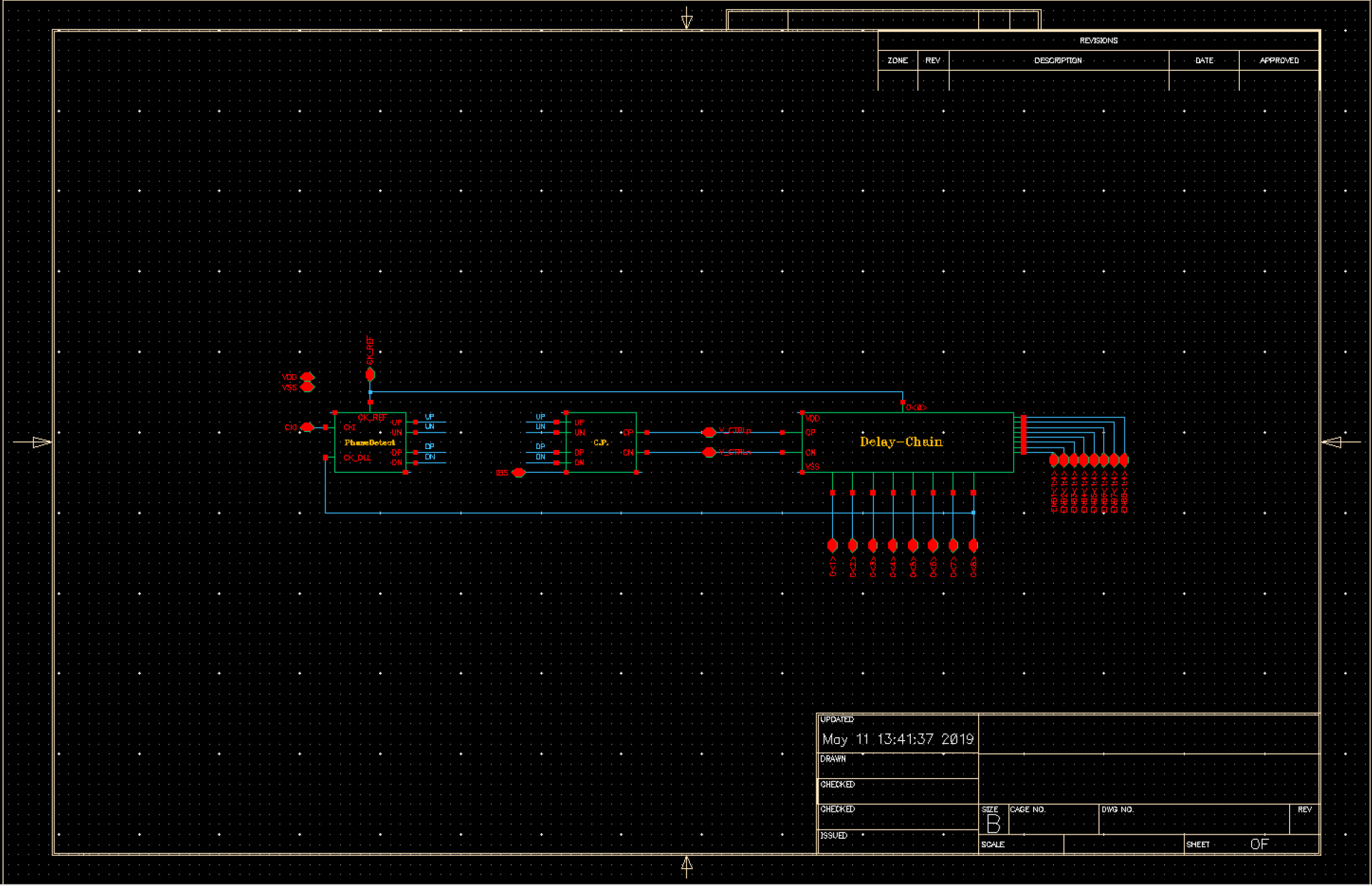
The input pins are: CKI (Input Clock), VDD (Power Supply), VSS (ground), IBS (Biasing of Charge Pump). The output pins are O<1:8> the 8 phase clock output. Pins ENBX<1:4> are for fine tune control of the delay of each delay cell unit.

**Description of the Cell Library:**

The tabular description below corresponds to the structure of the design library as seen in Cadence.

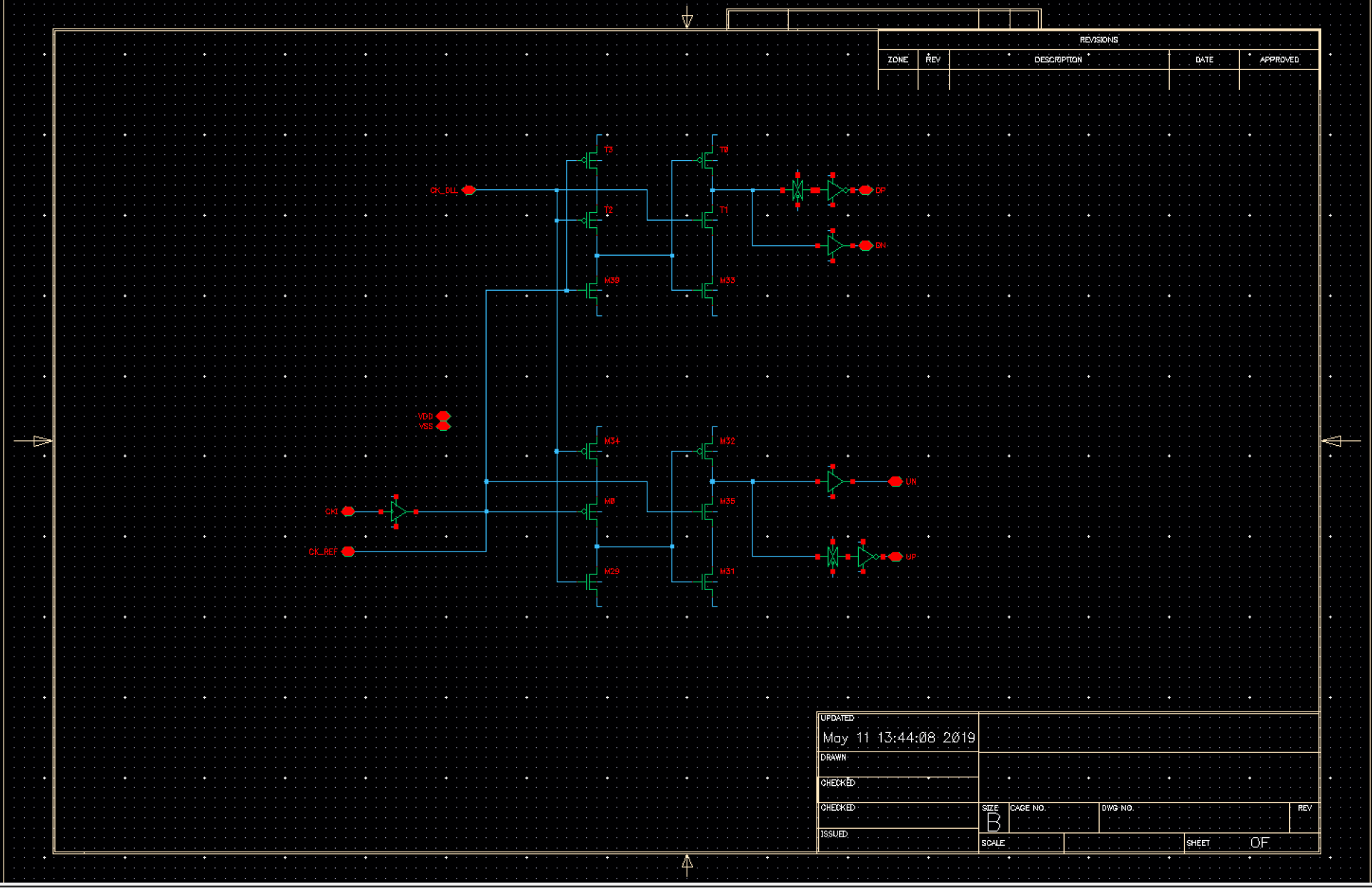
|  |  |  |  |
| --- | --- | --- | --- |
| **#** | Category | **CellName** | **Description** |
| 1 | GF65\_DLL | DLL\_core | 2GHz / 8-phase / 100fsec\_rms jitter DLL |
|  |  | SW\_std | Transmission gate switch |
|  |  | Lay\_CP | Charge Pump cell used in the DLL |
|  |  | Lay\_DLL\_PD\_top | Phase detector cell used in DLL |
|  |  | Lay\_DLL\_delay\_unit | Delay unit used in DLL |
| 2 | DLL Test Benches | test\_DLL | Testbench for DLL |

The complete schematic of the design is:



The schematic of the modules are as follows:

Phase detector:

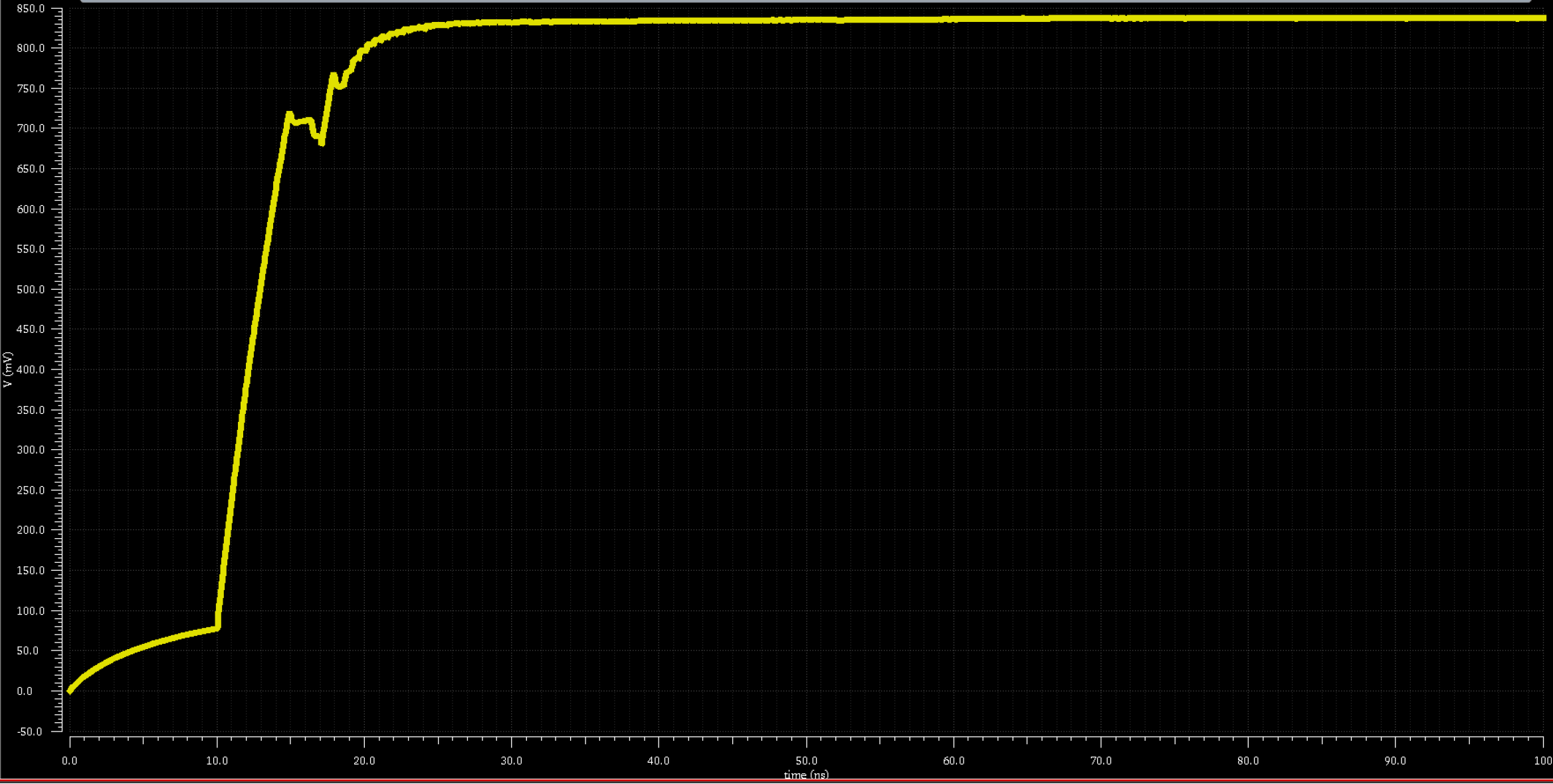


|  |  |
| --- | --- |
| Chare Pump and Loop-filter | Delay cells |
|  |  |

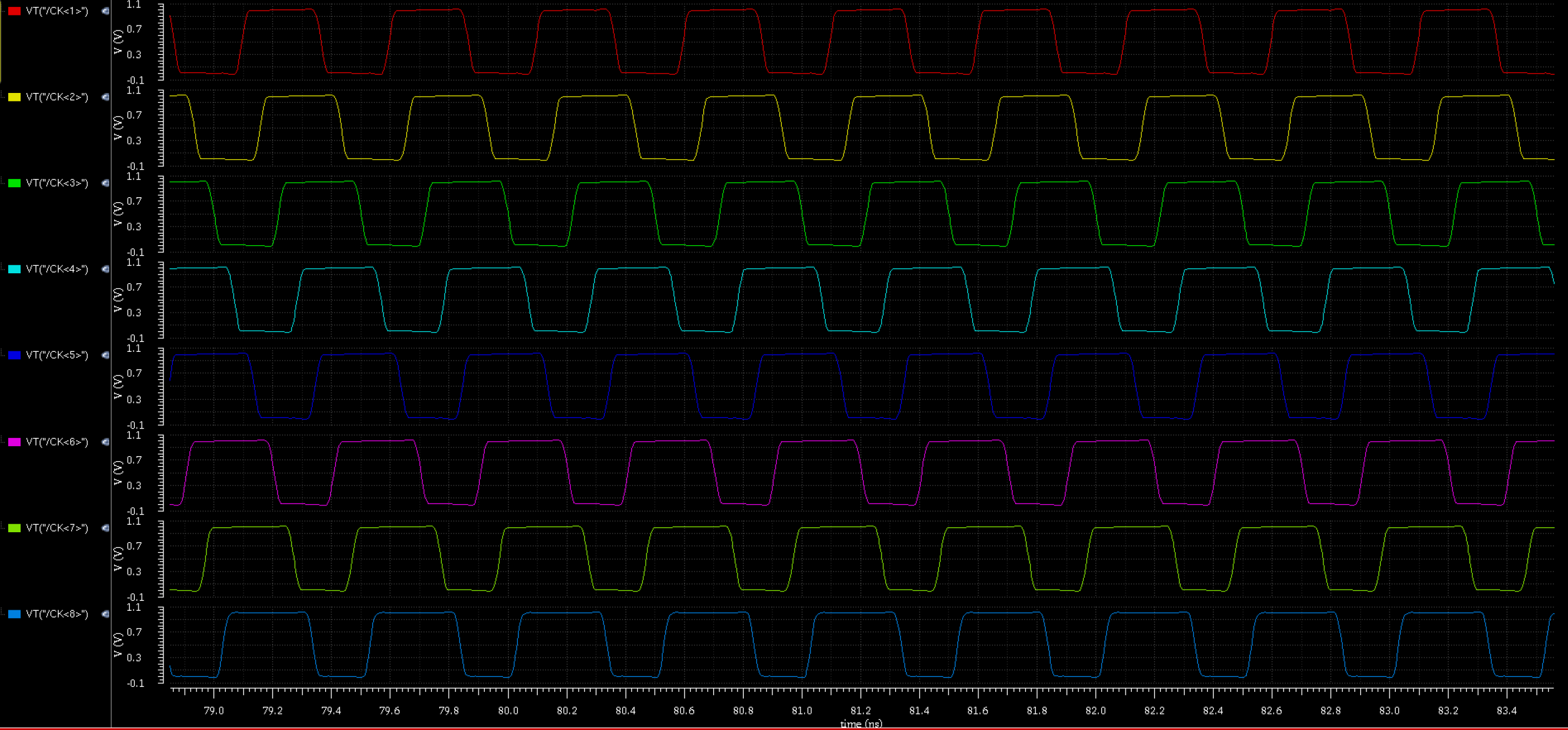
**Test Bench:**

Testbench for DLL transient analysis.

**Simulation Results: Power dissipation: 2.4mW**



Transient waveform of the phase locking



Transient waveform of 8 phase output clock signals