聯陽半導體
ITE Tech. Inc.

IT9130 (BX) Series

DVB-T Front-End Integrated Receiver

Preliminary Specification V0.0.2

ITE TECH. INC.

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Revision History

Section	Revision	Page No.
	• First release for IT9130 BX Series (IT9133FN/BX, IT9135FN/BX, IT9137FN/BX)	
	• Added Ordering Information of IT9133FN/BX and IT9137FN/BX	
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CONTENTS

FIGURES

TABLES

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1. Features

■ **Integrated RF Tuner for DVB-T**

- **Built-in RF tuner** to support DVB-T receptions at UHF band and VHF band
- **Zero-IF** direct conversion architecture to achieve low power consumption
- **Single-ended** RF input eliminates the requirement of Balun
- No external **SAW filter** is required
- **Integrated LNA** with low noise figure to meet MBRAI 2.0 requirement and achieve superior sensitivity performance without the need of external LNA
- Integrated Received Signal Strength Indicator (**RSSI**) for precise AGC adjustment in the environments with Adjacent Channel Interferences (ACI)
- Automatic RF/BB AGC **gain distribution** to properly compromise the performance between noise and linearity
- Built-in **RF loop-through** with adjustable gain

■ **Superior DVB-T COFDM Reception**

- Complete OFDM demodulation compliant to DVB-T specification ETSI 300 744, including Annexes F and G
- Performance compliant to NorDig Unified v2.1, D-Book, E-Book, Taiwan BSMI, and MBRAI2.0
- Robust immunity to Doppler Effect in **mobile**/ **portable** reception
- Superior dynamic **echo** performance which meets NorDig, D-Book, and MBRAI echo inside and outside guard interval tests
- Diversity-enabled **dual channel receiving** capability enabling high mobility DVB-T reception, picture-in-picture (PIP), and record while watching (PVR) applications
- Automatic 2K/4K/8K mode and guard interval detection
- Digital carrier frequency offset correction up to ±500KHz
- Digital crystal frequency jitter compensation up to ±100ppm
- All-digital time and frequency synchronization tracking loop
- All-digital **adjacent channel interference** (ACI) rejection filtering for supporting 5/6/7/8MHz bandwidth
- Adaptive **co-channel interference** (CCI) filtering for interferences including PAL/ SECAM/NICAM
- Effective **impulse noise** rejection
- **Fast channel scan** and **switch** time

■ **Versatile Interfaces**

- Embedded **USB 1.1** and **2.0** compatible interface support with suspend mode
- Serial and parallel **MPEG2-TS output** interface with simple two-wire control bus
- **MPEG2-TS input** interface to support dual-channel reception or TS relay
- Infrared (**IR**) interface provided for remote control
- Multiple sets of **PWM** and **GPIO** for external control purpose

■ **Compact for Application Designs**

- **Single crystal** (12MHz or 20.48 MHz) is only required to provide all internal clocks
- **On-chip LDO** provides the flexibility of system-wise power design
- **Single power supply** (3.3V) is only required, with the option of using external 1.2V
- Superior all-CMOS SoC technology enables **ultra-low power** consumption (minimum **200mW** core power consumption operating at 8MHz, 8K mode, 64QAM, and code rate 7/8 with Transport Stream output)
- **Single-ended** RF input eliminates the requirement of Balun
- High sensitivity and ACI immunity are achieved **without external LNA**
- **Reference clock output** to enable signal crystal design with other chips

■ **Simple Application Programming Interface with Complete SW Package**

- Complete **API** for fast and easy integration with **application processors**, **multimedia processors**, or CPU-based platforms
- Integrated transport stream de-multiplexer (**PID filtering**) with bypass mode
- Comprehensive **performance** and **signal condition** monitoring parameters available through register access
- **Auto signal re-acquisition** without external programming
- Windows **Mobile/CE** drivers support
- USB **BDA driver** support for **Windows 7**/XP/Vista
- **Linux driver** support

2. General Description

IT9130 is a series of highly integrated DVB-T single-chip receiver consisting of high quality RF tuner front-end and COFDM demodulator to aim for superior performance, ultra-low power consumption, and simple system design of various DVB-T applications. IT9130 offers very low total Bill Of Material solutions. It does not require external SAW filter, LNA, or Balun. IT9130 requires only one power regulator and one crystal to further simplify the system design and reduce the system cost. The ultra-low power consumption feature of the IT9130 makes it the perfect choice for all kinds of DVB-T applications. IT9130 series also supports lots of output interfaces, including embedded USB 2.0 interface, and serial/parallel MPEG2-TS interface input/output with built-in de-multiplexer.

IT9130 series is compliant with ETSI EN 300 744 V1.5.1 (including Annexes F and G), NorDig Unified Requirement 2.1, MBRAI2.0, DTG D-Book, IEC62216-1 E-Book, BSMI Taiwan and it can operate at 2K, 4K, or 8K mode with 5, 6, 7, or 8MHz bandwidth. All modulations (QPSK, 16QAM, 64QAM), code rates (1/2, 2/3, 3/4, 5/6, 7/8), and guard intervals (1/4, 1/8, 1/16, 1/32) are supported and automatically detected from the TPS parameters.

Depending on the reception status, IT9130 continuously adjusts the states of its internal modules to avoid unnecessary power consumption and hence it can achieve the maximal power saving.

The integrated RF tuner of IT9130 provides frond-end frequency down-conversion for applications over UHF band and VHF band. The integrated LNA with low noise figure meets MBRAI 2.0 requirement and achieve superior sensitivity performance without the need of external LNA

The Zero-IF direct conversion architecture of IT9130 achieves low power consumption and the integrated dual analog-to-digital converters (ADC) are capable of delivering the performance required for all modulations and code rates of DVB-T.

The single-ended RF input architecture of IT9130 eliminates the requirement of balun components.

IT9130 AGC control loop bandwidth is designed to track a wide dynamic range of the received signal levels for slow or fast channel variations. The automatic RF/BB AGC gain distribution properly compromises the performance between noise and linearity.

In IT9130, an active impulse noise rejection algorithm removes the detrimental effects of the impulse noise and significantly improves the robustness of TV reception against interference from vehicles and electrical appliances.

IT9130 uses the most advanced digital signal processing techniques to combat various impairments encountered in fixed, portable, and mobile channels. Co-channel interference is actively searched and rejected by sophisticated digital signal processing in IT9130. Adjacent Channel Interference (ACI) is rejected by precisely controlled digital filters for 5, 6, 7, and 8MHz bandwidth. The Integrated Received Signal Strength Indicator (RSSI) further yields precise AGC adjustment in the environments with ACI.

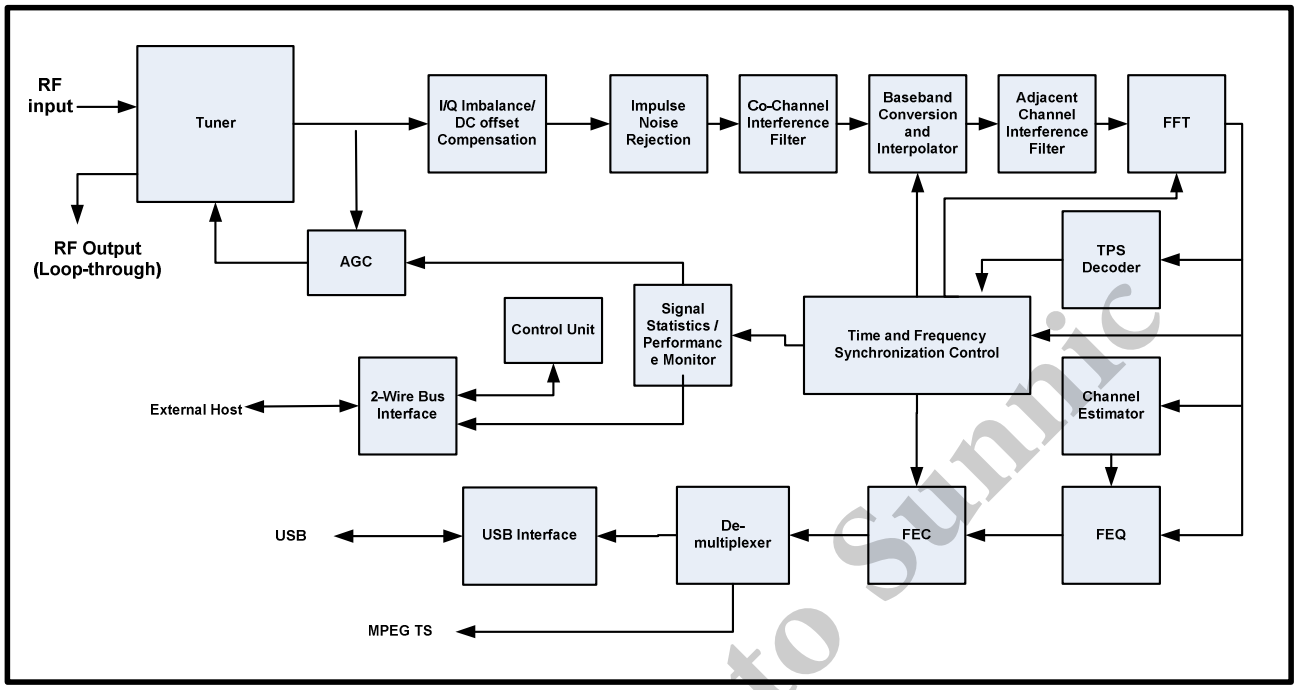
The all-digital synchronization tracking loops of IT9130 are capable of recovering carrier frequency offsets as large as ±500 kHz and tolerating crystal jitters as large as ±100ppm. The adaptive FFT window position tracking loop in IT9130 accurately identifies pre-echo or post-echo multi-path channels even in highly mobile environments. Therefore, inter-symbol interference (ISI) and inter-carrier interference (ICI) is greatly reduced.

In IT9130, the common phase error caused by tuner phase noise is corrected by a joint channel estimation and phase noise tracking algorithm to improve the robustness to RF imperfections. Besides, the multi-dimensional channel estimation and tracking scheme in IT9130 adaptively adjusts its internal parameters to reflect the different requirements in fixed, portable, or mobile channels and hence, optimal performance can be achieved for all DVB-T applications.

IT9130 provides a comprehensive set of performance monitoring parameters accessible. These parameters include signal strength and signal quality indicators, post-Viterbi bit error rate, Reed-Solomon packet error rate, TPS lock, and MPEG Sync lock indicators, carrier and crystal offsets, and many more.

A complete set of application programming interface (API) is available, facilitating fast and easy integration into products on Windows Mobile, Windows CE, Windows 7, Windows XP, Vista, Linux, and many other operating systems. Furthermore, a complete set of USB drivers on Windows 7/XP/Vista with Microsoft BDA (Broadcast Driver Architecture) compliant and on Windows Mobile/CE are provided for IT9130.

3. Block Diagram



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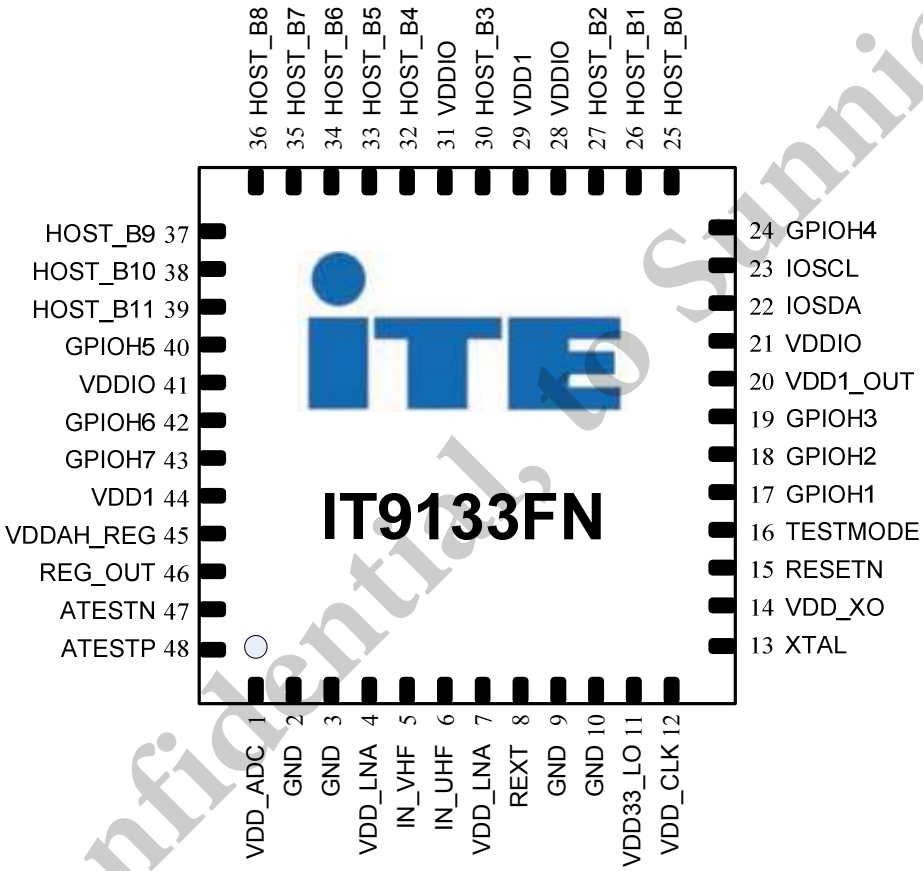
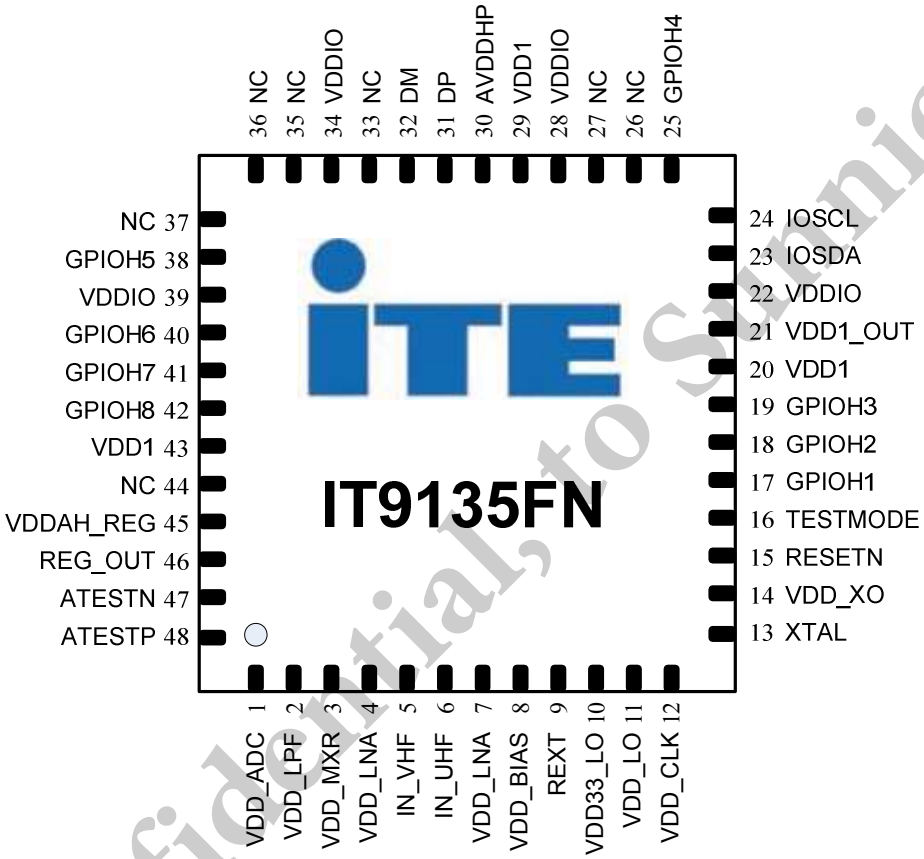
4. Pin Configuration





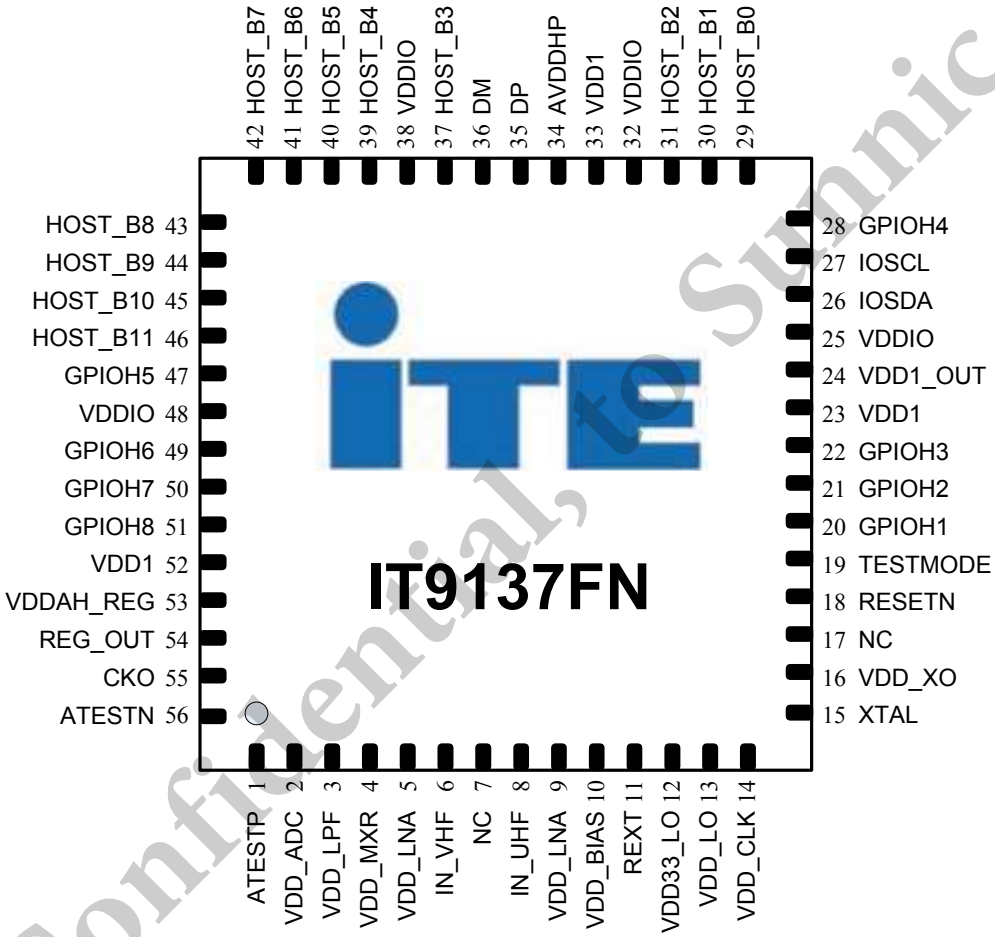


Table 4-1. IT9133 pin listed in numeric order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VDD_ADC	13	XTAL	25	HOST_B0	37	HOST_B9
2	GND	14	VDD_XO	26	HOST_B1	38	HOST_B10
3	GND	15	RESETN	27	HOST_B2	39	HOST_B11
4	VDD_LNA	16	TESTMODE	28	VDDIO	40	GPIOH5
5	IN_VHF	17	GPIOH1	29	VDD1	41	VDDIO
6	IN_UHF	18	GPIOH2	30	HOST_B3	42	GPIOH6
7	VDD_LNA	19	GPIOH3	31	VDDIO	43	GPIOH7
8	REXT	20	VDD1_OUT	32	HOST_B4	44	VDD1
9	GND	21	VDDIO	33	HOST_B5	45	VDDAH_REG
10	GND	22	IOSDA	34	HOST_B6	46	REG_OUT
11	VDD33_LO	23	IOSCL	35	HOST_B7	47	ATESTN
12	VDD_CLK	24	GPIOH4	36	HOST_B8	48	ATESTP

Table 4-2. IT9135 pin listed in numeric order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VDD_ADC	13	XTAL	25	GPIOH4	37	NC
2	VDD_LPF	14	VDD_XO	26	NC	38	GPIOH5
3	VDD_MXR	15	RESETN	27	NC	39	VDDIO
4	VDD_LNA	16	TESTMODE	28	VDDIO	40	GPIOH6
5	IN_VHF	17	GPIOH1	29	VDD1	41	GPIOH7
6	IN_UHF	18	GPIOH2	30	AVDDHP	42	GPIOH8
7	VDD_LNA	19	GPIOH3	31	DP	43	VDD1
8	VDD_BIAS	20	VDD1	32	DM	44	NC
9	REXT	21	VDD1_OUT	33	NC	45	VDDAH_REG
10	VDD33_LO	22	VDDIO	34	VDDIO	46	REG_OUT
11	VDD_LO	23	IOSDA	35	NC	47	ATESTN
12	VDD_CLK	24	IOSCL	36	NC	48	ATESTP

Table 4-3. IT9137 pin listed in numeric order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	ATESTP	15	XTAL	29	HOST_B0	43	HOST_B8
2	VDD _ ADC	16	VDD_XO	30	HOST_B1	44	HOST_B9
3	VDD_LPF	17	NC	31	HOST_B2	45	HOST_B10
4	VDD_MRX	18	RESETN	32	VDDIO	46	HOST_B11
5	VDD_ LNA	19	TESTMODE	33	VDD1	47	GPIOH5
6	IN_VHF	20	GPIOH1	34	AVDDHP	48	VDDIO
7	NC	21	GPIOH2	35	DP	49	GPIOH6
8	IN_UHF	22	GPIOH3	36	DM	50	GPIOH7
9	VDD_ LNA	23	VDD1	37	HOST_B3	51	GPIOH8
10	VDD_BIAS	24	VDD1_OUT	38	VDDIO	52	VDD1
11	REXT	25	VDDIO	39	HOST_B4	53	VDDAH_REG
12	VDD33_LO	26	IOSDA	40	HOST_B5	54	REG_OUT
13	VDD_ LO	27	IOSCL	41	HOST_B6	55	CKO
14	VDD_CLK	28	GPIOH4	42	HOST_B7	56	ATESTN

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5. Pin Description

Table 5-1. IT9133 Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
1	VDD_ADC	PWR	-	***+1.4V Analog Power Supply***
4,7	VDD_LNA	PWR	-	***+1.4V Analog Power Supply***
11	VDD33_LO	PWR	-	***+3.3V Analog Power Supply***
12	VDD_CLK	PWR	-	***+1.4V Analog Power Supply***
14	VDD_XO	PWR	-	***+1.4V Analog Power Supply***
45	VDDAH_REG	PWR	-	***+3.3V Analog Power Supply***
21,28,31,41	VDDIO	PWR	-	***+3.3V Power Supply***
29,44	VDD1	PWR	-	***+1.2V Power Supply***
2,3,9,10	GND	GND	-	***Ground***

Table 5-2. IT9133 Pin Description of Analog I/O Signals

Pin(s) No.	Symbol	Attribute	Power	Description
5	IN_VHF	AI	-	***RF signal input (VHF)***
6	IN_UHF	AI	-	***RF signal input (UHF)***
8	REXT	AIO	-	***External bias resistor***
13	XTAL	AI	-	***Crystal Oscillator input***
20	VDD1_OUT	AO	VDD1	***Internal LDO output (+1.2V)***
46	REG_OUT	AO	VDDAH_REG	***Internal LDO output (+1.4V)***
47	ATESTN	AO	-	***Reserved***
48	ATESTP	AO	-	***Reserved***

Table 5-3. IT9133 Pin Description of Digital I/O Signals

Pin(s) No.	Symbol	Attribute	Power	Description
15	RESETN	DI	VDDIO	***Power-on Reset (Low Active)***
16	TESTMODE	DI	VDDIO	***Test mode selection; tied to ground for normal operation.***
17	GPIOH1	DIO	VDDIO	***General purpose I/O***
18	GPIOH2	DIO	VDDIO	***General purpose I/O***
19	GPIOH3	DIO	VDDIO	***General purpose I/O***
22	IOSDA	DIO	VDDIO	***Two-wire bus serial data line***
23	IOSCL	DI	VDDIO	***Two-wire bus serial clock line***
24	GPIOH4	DIO	VDDIO	***General purpose I/O***
25	HOST_B0	DO	VDDIO	***Host interface***
26	HOST_B1	DO	VDDIO	***Host interface***
27	HOST_B2	DO	VDDIO	***Host interface***
30	HOST_B3	DO	VDDIO	***Host interface***
32	HOST_B4	DO	VDDIO	***Host interface***
33	HOST_B5	DO	VDDIO	***Host interface***
34	HOST_B6	DO	VDDIO	***Host interface***
35	HOST_B7	DO	VDDIO	***Host interface***
36	HOST_B8	DO	VDDIO	***Host interface***
37	HOST_B9	DO	VDDIO	***Host interface***
38	HOST_B10	DO	VDDIO	***Host interface***
39	HOST_B11	DO	VDDIO	***Host interface***
40	GPIOH5	DIO	VDDIO	***General purpose I/O***
42	GPIOH6	DIO	VDDIO	***General purpose I/O***
43	GPIOH7	DIO	VDDIO	***General purpose I/O***

Table 5-4. IT9135 Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
1	VDD_ADC	PWR	-	***+1.4V Analog Power Supply***
2	VDD_LPF	PWR	-	***+1.4V Analog Power Supply***
3	VDD_MXR	PWR	-	***+1.4V Analog Power Supply***
4,7	VDD_LNA	PWR	-	***+1.4V Analog Power Supply***
8	VDD_BIAS	PWR	-	***+1.4V Analog Power Supply***
10	VDD33_LO	PWR	-	***+3.3V Analog Power Supply***
11	VDD_LO	PWR	-	***+1.4V Analog Power Supply***
12	VDD_CLK	PWR	-	***+1.4V Analog Power Supply***
14	VDD_XO	PWR	-	***+1.4V Analog Power Supply***
20,29,43	VDD1	PWR	-	***+1.2V Power Supply***
22,28,34,39	VDDIO	PWR	-	***+3.3V Power Supply***
30	AVDDHP	PWR	-	***+3.3V Power Supply for USB***
45	VDDAH_REG	PWR	-	***+3.3V Analog Power Supply***

Table 5-5. IT9135 Pin Description of Analog I/O Signals

Pin(s) No.	Symbol	Attribute	Power	Description
5	IN_VHF	AI	-	***RF signal input (VHF)***
6	IN_UHF	AI	-	***RF signal input (UHF)***
9	REXT	AIO	-	***External bias resistor***
13	XTAL	AI	-	***Crystal Oscillator input***
21	VDD1_OUT	AO	VDD1	***Internal LDO output (+1.2V)***
46	REG_OUT	AO	VDDAH _REG	***Internal LDO output (+1.4V)***
31	DP	AIO	-	***Differential Positive signal for USB***
32	DM	AIO	-	***Differential Negative signal for USB***
47	ATESTN	AO	-	***Reserved***
48	ATESTP	AO	-	***Reserved***

Table 5-6. IT9135 Pin Description of Digital I/O Signals

Pin(s) No.	Symbol	Attribute	Power	Description
15	RESETN	DI	VDDIO	***Power-on Reset (Low Active)***
16	TESTMODE	DI	VDDIO	***Test mode selection; tied to ground for normal operation.***
17	GPIOH1	DIO	VDDIO	***General purpose I/O***
18	GPIOH2	DIO	VDDIO	***General purpose I/O***
19	GPIOH3	DIO	VDDIO	***General purpose I/O***
23	IOSDA	DIO	VDDIO	***Two-wire bus serial data line***
24	IOSCL	DO	VDDIO	***Two-wire bus serial clock line***
25	GPIOH4	DIO	VDDIO	***General purpose I/O***
38	GPIOH5	DO	VDDIO	***General purpose I/O***
40	GPIOH6	DIO	VDDIO	***General purpose I/O***
41	GPIOH7	DIO	VDDIO	***General purpose I/O***
42	GPIOH8	DIO	VDDIO	***General purpose I/O***

Table 5-7. IT9137 Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
2	VDD_ADC	PWR	-	***+1.4V Analog Power Supply***
3	VDD_LPF	PWR	-	***+1.4V Analog Power Supply***
4	VDD_MXR	PWR	-	***+1.4V Analog Power Supply***
9	VDD_LNA	PWR	-	***+1.4V Analog Power Supply***
10	VDD_BIAS	PWR	-	***+1.4V Analog Power Supply***
12	VDD33_LO	PWR	-	***+3.3V Analog Power Supply***
13	VDD_LO	PWR	-	***+1.4V Analog Power Supply***
14	VDD_CLK	PWR	-	***+1.4V Analog Power Supply***
16	VDD_XO	PWR	-	***+1.4V Analog Power Supply***
23,33,52	VDD1	PWR	-	***+1.2V Power Supply***
25,32,38,48	VDDIO	PWR	-	***+3.3V Power Supply***
34	AVDDHP	PWR	-	***+3.3V Power Supply for USB***
53	VDDAH_REG	PWR	-	***+3.3V Analog Power Supply***

Table 5-8. IT9137 Pin Description of Analog I/O Signals

Pin(s) No.	Symbol	Attribute	Power	Description
1	ATESTP	AIO	-	***Reserved***
6	IN_VHF	AI	-	***RF signal input (VHF)***
8	IN_UHF	AI	-	***RF signal input (UHF)***
11	REXT	AIO	-	***External bias resistor***
15	XTAL	AIO	-	***Crystal Oscillator input***
24	VDD1_OUT	AO	VDD1	***Internal LDO output (+1.2V)***
35	DP	AIO	-	***Differential Positive signal for USB***
36	DM	AIO	-	***Differential Negative signal for USB***
54	REG_OUT	AO	VDDAH_REG	***Internal LDO output (+1.4V)***
55	CKO	AO	-	***Clock output for another device***
56	ATESTN	AO	-	***Reserved***

Table 5-9. IT9137 Pin Description of Digital I/O Signals

Pin(s) No.	Symbol	Attribute	Power	Description
18	RESETN	DI	VDDIO	***Power-on Reset (Low Active)***
19	TESTMODE	DI	VDDIO	***Test mode selection; tied to ground for normal operation.***
20	GPIOH1	DIO	VDDIO	***General purpose I/O***
21	GPIOH2	DIO	VDDIO	***General purpose I/O***
22	GPIOH3	DIO	VDDIO	***General purpose I/O***
26	IOSDA	DIO	VDDIO	***Two-wire bus serial data line***
27	IOSCL	DO	VDDIO	***Two-wire bus serial clock line***
28	GPIOH4	DIO	VDDIO	***General purpose I/O***
29	HOST_B0	DO	VDDIO	***Host interface***
30	HOST_B1	DO	VDDIO	***Host interface***
31	HOST_B2	DO	VDDIO	***Host interface***
37	HOST_B3	DO	VDDIO	***Host interface***
39	HOST_B4	DO	VDDIO	***Host interface***
40	HOST_B5	DO	VDDIO	***Host interface***
41	HOST_B6	DO	VDDIO	***Host interface***
42	HOST_B7	DO	VDDIO	***Host interface***
43	HOST_B8	DO	VDDIO	***Host interface***
44	HOST_B9	DO	VDDIO	***Host interface***

Pin(s) No.	Symbol	Attribute	Power	Description
45	HOST_B10	DO	VDDIO	***Host interface***
46	HOST_B11	DO	VDDIO	***Host interface***
47	GPIOH5	DO	VDDIO	***General purpose I/O***
49	GPIOH6	DIO	VDDIO	***General purpose I/O***
50	GPIOH7	DIO	VDDIO	***General purpose I/O***
51	GPIOH8	DIO	VDDIO	***General purpose I/O***

Table 5-10. Pin description of GPIO and strapping

Name	Strapping	IO Functions	State after RESET
GPIOH1	Clock Select Bit 0	GPIO/ PWM/ Lock Indicator 1	High-Z
GPIOH2	Clock Select Bit 1	GPIO/ PWM/ Lock Indicator 2	High-Z
GPIOH3	Clock Select Bit 2	GPIO/ PWM/ Lock Indicator 3	High-Z
GPIOH4	Clock Select Bit 3	GPIO/ PWM/ Lock Indicator 4	High-Z
GPIOH5	Mode Select Bit 0/ Two-wire bus address bit 0	GPIO/ Suspend Resume	High-Z
GPIOH6	Mode Select Bit 1/ Two-wire bus address bit 1	GPIO	High-Z
GPIOH7	Mode Select Bit 2	GPIO; IR receiving	High-Z
GPIOH8	Mode Select Bit 3	GPIO	High-Z

Table 5-11. Strapping sampled at the rising edge of the RESET signal

Pin Name	Selection
{GPIOH4,GPIOH3,GPIOH2,GPIOH1}	Crystal frequency: 0000 crystal = 12 MHz 0001 crystal = 20.48MHz
{GPIOH8,GPIOH7,GPIOH6,GPIOH5}	Mode strapping and 2-wire bus address selection: 00xx TS mode, {GPIOH6, GPIOH5} = 2-wire address[1:0] 0001 Salve device of DCA mode 0101 USB mode

Table 5-12. Pin list of Host Interface

Pin \ Mode	TS Output Mode	TS Input Mode	Diversity Master Mode	Diversity Slave Mode
HOST_B0	MPEG Fail	MPEG Data[7]	Output Data[3]	Output Clock
HOST_B1	MPEG Sync	MPEG Data[6]	Output Data[2]	Output Valid
HOST_B2	MPEG Valid	MPEG Data[5]	Output Data[1]	Output Data[0]
HOST_B3	MPEG Clock	MPEG Data[4]	Output Data[0]	Output Data[1]
HOST_B4	MPEG Data[0]	MPEG Data[3]	Output Valid	Output Data[2]
HOST_ B5	MPEG Data[1]	MPEG Data[2]	Output Clock	Output Data[3]
HOST_B6	MPEG Data[2]	MPEG Data[1]	Input Data[3]	Input Clock
HOST_B7	MPEG Data[3]	MPEG Data[0]	Input Data[2]	Input Valid
HOST_B8	MPEG Data[4]	MPEG Clock	Input Data[1]	Input Data[0]
HOST_B9	MPEG Data[5]	MPEG Valid	Input Data[0]	Input Data[1]
HOST_B10	MPEG Data[6]	MPEG Sync	Input Valid	Input Data[2]
HOST_B11	MPEG Data[7]	MPEG Fail	Input Clock	Input Data[3]

Notes: 1) These pins have no integrated pull up/down.
2) The state of these pins immediately after reset is high-Z.
3) The pads of these pins are of the CMOS type.
4) These pins are on I/O power domain

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6. Powering

IT9130 has four power domains, RF, Core, IO, and USB respectively.

The RF Domain is supplied by 3.3V±10% to provide power for RF tuner functions. The external 3.3V should be connected to pin VDDAH_REG. The other RF analog power supply pins (1.4V) shall be connected to the pin REG_OUT to be powered by the built-in voltage regulator.

The Core Domain is supplied by 1.2V±10% to provide power for the core circuits of IT9130. It can be provided by external 1.2V or using the internal voltage regulator from the pin VDD1_OUT.

The IO Domain provides power for the host interface, including the MPEG TS interface, diversity interface, 2-wire bus, and GPIOH1~GPIOH8. The supply voltage for IO Domain is 3.3V±10%.

The USB Power Domain is supplied by 3.3v±10% to power the USB interface under USB mode (IT9135/IT9137 only). Otherwise, the pin AVDDHP should be connected to ground.

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7. Functional Descprition

7.1 Output Modes

IT9130 supports different output modes according to the selected output interfaces, including USB2.0 mode, and MPEG TS mode. The output mode is chosen by appropriately setting the strapping pins as specified in Table 5-11 and register programming after strapping.

The USB2.0 mode is further divided into stand-alone, diversity, and dual-channel modes. To support diversity and dual-channel modes for DVB-T applications, one IT9137 is required as the master device of diversity mode and a second IT9133 or IT9137 is required as the slave device.

The supported operation modes of IT9130 are summarized in Table 7-1 and the control and data paths in each operation mode are summarized in Table 7-2.

Table 7-1. Operation modes of IT9130

Mode / Part #	MPEG TS	USB2.0	USB2.0 Diversity/ Dual-channel
IT9133	Yes	No	Slave
IT9135	No	Yes	No
IT9137	Yes	Yes	Master/Slave

Table 7-2. Data path and contol paths at each output mode

Path / Mode	Data Path	Control Path
USB 2.0	USB	USB
MPEG TS	MPEG TS	2-wire bus

7.1.1 MPEG TS Mode

In the MPEG TS mode, IT9130 outputs MPEG2 transport streams to the host through either the parallel or serial MPEG2 TS output interface. A backend MPEG2 decoder is needed to interface with IT9130 using the 2-wire bus and the MPEG2 TS interface signals. More details of the MPEG TS interface are given in Section 7.9.1.

7.1.2 Standard USB2.0 Mode

In the standard USB 2.0 mode, IT9130 communicates with the host through the embedded USB 2.0 interface. The data streams decoded by IT9130 and control/status signals are all encapsulated in the USB frames. The standard USB2.0 mode also supports diversity receiving and dual-channel receiving for picture-in-picture (PIP) applications in DVB-T. More details of the USB interface are given in Section 7.10

7.1.2.1 Dual-Channel Reception

When operating in the USB mode, dual-channel receiving is supported. The dual-channel receiving function enables two IC's of the IT9130 series to be independently tuned into different RF channels. The contents of the RF channels are simultaneously delivered to the host for picture-in-picture (PIP) and similar applications. For

dual-channel receiving, one IT9137 is connected to the host through the USB interface, and configured as the master device that controls a slave device. The slave device can be an IT9133 or IT9137.

7.1.3 Diversity Reception

When operating in the USB modes, diversity receiving is also supported. The diversity receiving function enables two IC's of the IT9130 series, connected through the diversity interface, to communicate and exchange data in order to significantly enhance receiver sensitivity and mobile performance. For diversity receiving, one IT9137 is connected to the host through the USB interface, and configured as the master device that controls an IT9133 or IT9137 slave device. More details of the diversity interface are given in Section 7.9.2.

7.2 Analog Interface

7.2.1 Clocking

IT9130 has on-chip crystal amplifiers for clock generation. Only single 12MHz crystal is required to generate all internal clocks.

IT9137 also provides a buffered clock output (CKO) which, for example, can be used to drive a second IT9130 series IC in diversity receiving or dual-channel applications.

The IT9130 clocking circuit requires a stable reference clock. It can be provided by either of the following two methods:

1. Connect a crystal across the oscillator pin XTAL and ground, or
2. Connect an external clock source to the pin XTAL.

With programmable PLL, the supported reference clock frequencies can be selected as 12MHz or 20.48MHz. This clock source can come from the crystal, other external clock source, or the buffered clock output (CKO) of another IT9130 series IC (in diversity receiving or dual-channel applications).

7.2.2 Clock Table

The programmable PLL default clock ratio is decided by pin strapping which is described in Table 5-11. After the initial operation, it can also be re-programmed through register access. More details on programming the PLL ratio for different clock frequency selection can be found in IT9130 Programming Guide.

7.3 Initialization

Several important system parameters need to be programmed correctly in order to insure proper operations of IT9130. These include, among other things, the carrier frequency of the RF signal, ADC sampling frequency, and the channel bandwidth, which can be 5, 6, 7, or 8 MHz. More details on initializing IT9130 can be found in IT9130 Programming Guide.

7.4 UHF/VHF RF Tuner

IT9130 with RF tuner integrated to support DVB-T applications over UHF band (470 MHz ~ 862 MHz) and VHF band III (170 MHz ~ 240MHz). The Integrated LNA with low noise figure achieves superior sensitivity performance without the need of external LNA. The single-ended RF input architecture also eliminates the requirement of Balun. The automatic RF/BB AGC gain distribution can properly compromise the performance between noise and linearity.

7.5 DVB-T COFDM Digital Signal Processing

7.5.1 Time-Domain Signal Processing

Before the received signals are converted to the frequency domain via Fast Fourier Transform (FFT), several sophisticated digital signal processing algorithms are implemented to handle different impairments encountered in the transmission environment.

An automatic gain control (AGC) mechanism measures the received signal strength to determine the correct tuner gain-control signal values. The DC offset and IQ amplitude and phase imbalance are dynamically tracked and compensated.

Co-channel interference (CCI) due to PAL, NICAM, or any other source is adaptively detected and notched out if necessary. No prior knowledge of the CCI location is needed, and the activation of the CCI cancellation filter is automatic.

The sampling frequency offset introduced by the front-end tuner is compensated digitally to generate a complex signal centered at DC at the elementary period, which is 7/64us for 8MHz channels, 1/8us for 7MHz channels, and 7/48us for 6MHz channels, and 7/40us for 5MHz channels.

Adjacent channel interference (ACI) is removed by a very sharp digital filter whose bandwidth is independent of the DVB-T channel bandwidth.

7.5.2 Frequecy-Domain Signal Processing

In the frequency domain, a Transmission Parameter Signaling (TPS) decoder is implemented to extract system parameters, including the constellation, hierarchy information, code rate, FFT mode, and guard interval.

The channel estimator estimates and the amplitude and phase distortion caused by the transmission channel and radio frequency (RF) front-end. The common phase error introduced by the RF front-end is also estimated. These distortions are then compensated by the frequency domain equalizer (FEQ). The equalized output of FEQ is then used to generate the input to forward-error-correction (FEC) for further processing.

7.5.3 Synchronization Loop

An all-digital synchronization loop is implemented in IT9130 to determine and track the correct FFT window position, track and compensate for the carrier frequency offset caused by the front-end tuner, and track and compensate for the clock jitter introduced by the local crystal. Since the synchronization loop is entirely digital, no analog VCXO is necessary. The IT9130 synchronization loop is capable of correcting carrier frequency offsets of up to ±500 kHz and clock offsets of up to ±100ppm

7.6 Forward Error Correction

7.6.1 FEC for DVB-T

Inner symbol and bit de-interleavers and outer de-interleavers compliant with ETSI EN 300 744 are implemented in the IT9130 forward error correction (FEC). Optional in-depth de-interleavers are also available for 2K and 4K modes. A Viterbi decoder with de-puncturing is used to decode the punctured convolutional code. A shortened (204, 188) Read-Solomon decoder that corrects up to eight byte-errors in a 204 byte frame follows the Viterbi decoder to extract the transport stream packets. A fail signal is alerted when the number of error bytes exceeds eight, and the same input is bypassed to the output in this case. Finally, de-scrambler reverses the scrambling process, and the 0x47 or 0xB8 sync byte insertion is removed after the de-scrambler. The output of the descrambler is then sent to the output interface.

7.7 Performance Monitor

IT9130 provides a complete set of registers for monitoring the performance and status of the demodulator. The parameters that can be monitored and derived include, among other things, the sampling clock and carrier frequency offsets, TPS and MPEG-2 lock signals, TPS parameters, bit error rates and packet error rates, signal quality, and signal strength. Details on performance monitoring for different broadcasting standards can be found in IT9130 Programming Guide.

7.8 2-Wire Interfaces

IT9130 provides a 2-wire interface for communicating with the host. It is also used to communicate with the second IT9130 series IC for diversity receiving or dual-channel receptions. The IT9130 2-wire Interface uses, respectively, pins IOSDA for the serial data and IOSCL for the serial clock. The bus address of the IT9130 2-wire Interface is determined by the strapping pins GPIOH6 and GPIOH5. When IT9130 is first powered on, the RESETN pin should be held low. Given the IT9130 is desired for MPEG TS mode or the slave device under USB diversity/dual-channel mode, as the RESETN pin transitions from low to high, the logic level of the strapping pins GPIOH6 and GPIOH5 are latched to determine the 2-wire bus address, as shown in Table 7-3. Note that the logic level of the strapping pins, GPIOH6 and GPIOH5, also determines its operation mode, as described in Table 5-11.

Table 7-3. IT9130 2-wire bus address mapping table

{GPIOH6,GPIOH5} at strapping	2-Wire Bus Address
00	0x38
01*	0x3A
10	0x3C
11	0x3E

Note: {GPIOH6, GPIOH5} = {0, 1} is only used as the salve device for DCA/dual-channel applications

The IT9130 2-wire Interface supports both read and write operations. The circuit works as a slave transmitter in the read operation mode and slave receiver in the write operation mode to communicate with the Host. To communicate with the second IT9130 series IC, the circuit works as a master transmitter in the write operation mode and master receiver in the read operation mode.

Details on using the 2-wire Interface can be found in IT9130 Programming Guide.

7.9 Host Interfaces

IT9133 and IT9137 provides flexible interface, the so-called Host Interface, for connecting to the host in stand-alone applications, and for connecting to the master device, slave device, or the host in diversity receiving and dual-channel receiving modes. Depending on the application, these Host Interface can be configured into input interfaces or output interfaces. Host Interface comprises pins HOST_B0~HOST_B11.

IT9137 Host Interface (HOST_B0~HOST_B11) is used for connecting to the host in stand-alone modes, or for connecting to the master/slave device or the host in diversity receiving and dual-receiving modes. When connecting to the host, Host Interface (HOST_B0~HOST_B11) is configured into the MPEG TS mode with appropriate address selection by appropriate setting the strapping pins listed in Table 5-11. When connecting to the salve device, Host Interface should be configured as the master diversity interface for diversity receiving or configured as the MPEG TS input interface for dual-channel receiving. When connecting to the master device, Host Interface (HOST_B0~HOST_B11) should be configured into slave diversity interface for diversity receiving or MPEG TS output interface for dual-channel receiving, where the I2C address should be selected as 0x3A.

IT9133 Host Interface (HOST_B0~HOST_B11) is used to communicate with the host for MPEG-TS mode, and for communicating with the master device for diversity receiving and dual-channel receiving modes. When connecting to host, Host Interface (HOST_B0~HOST_B11) is configured as the MPEG TS mode with

appropriate address selection, which is selected by setting the strapping pins listed in Table 5-11. When connecting to the master device, Host Interface (HOST_B0~HOST_B11) should be configured into slave diversity interface for diversity receiving or MPEG TS output interface for dual-channel receiving, where the I2C address of IT9133 should be selected as 0x3A by the strapping pins listed in Table 5-11.

Details on how to configure the IT9130 host interfaces can be found in IT9130 Programming Guide.

7.9.1 MPEG2 Transport Stream Interface

The pin descriptions of Host Interface of IT9130 under MPEG TS mode are listed in Table 7-4.

Table 7-4. IT9130 MPEG-2 TS interface pins

Pin Name	MPEG TS Output Interface (IT9133/IT9137)		MPEG TS Input Interface (IT9137)	
	Function	Description	Function	Description
HOST_B0	MPEG Fail	MPEG uncorrectable packet indicator	MPEG Data[7]	# MPEG transport stream data. # 8-bit in the parallel mode and 1-bit in the serial mode. # Data[0] or Data[7] can be the data pin in the serial mode
HOST_B1	MPEG Sync	MPEG packet sync	MPEG Data[6]	
HOST_B2	MPEG Valid	MPEG data valid	MPEG Data[5]	
HOST_B3	MPEG Clock	MPEG clock	MPEG Data[4]	
HOST_B4	MPEG Data[0]	# MPEG transport stream data. # 8-bit in the parallel mode and 1-bit in the serial mode. # Data[0] or Data[7] can be the data pin in the serial mode	MPEG Data[3]	
HOST_B5	MPEG Data[1]		MPEG Data[2]	
HOST_B6	MPEG Data[2]		MPEG Data[1]	
HOST_B7	MPEG Data[3]		MPEG Data[0]	
HOST_B8	MPEG Data[4]		MPEG Clock	MPEG clock
HOST_B9	MPEG Data[5]		MPEG Valid	MPEG data valid
HOST_B10	MPEG Data[6]		MPEG Sync	MPEG packet sync pulse
HOST_B11	MPEG Data[7]		MPEG Fail	MPEG uncorrectable packet indicator

The MPEG TS interface of IT9130 offers both parallel/serial input and output. For IT9130 (IT9133/IT9137) operating in the MPEG-TS mode to communicate with the Host, the MPEG TS interface can operate in the parallel output mode, serial output mode, or be disabled. A timing diagram of the parallel output mode is shown in the example of Figure 7-1. For the serial output mode, the MPEG TS data can be configured to be output on Data[7] or Data[0]. On the other hand, for an IT9130 (IT9137) operating in the standard USB2.0 mode, the MPEG-2 transport stream interface is an input interface that accepts MPEG-2 transport streams in both serial and parallel fashion. A table of IT9130 MPEG-2 TS interface modes is given in Table 7-5.

The IT9130 MPEG-2 transport stream interface is fully configurable. The list of configurable parameters is shown in Table 7-6. Details on configuring the IT9130 MPEG-2 TS interface are available in IT9130 Programming Guide.

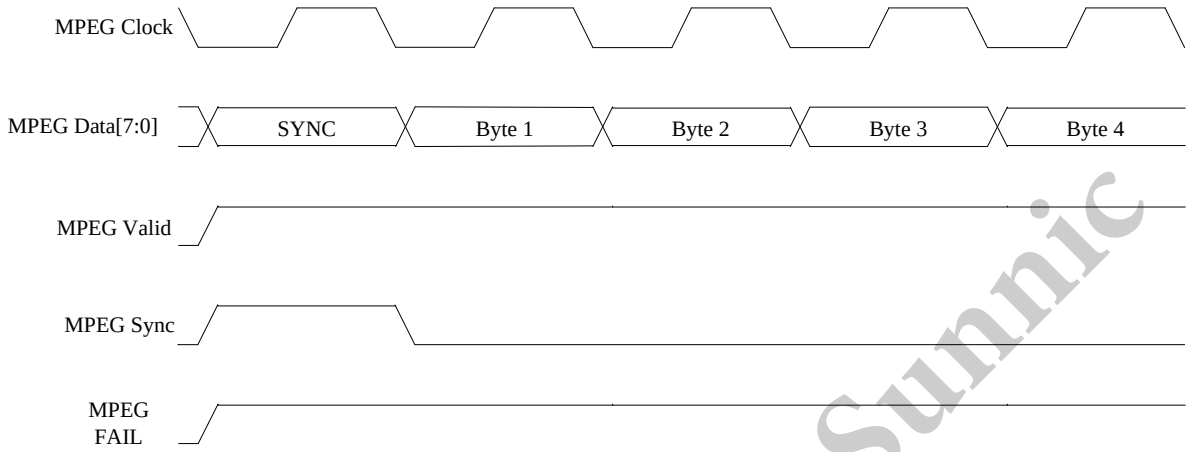


Figure 7-1. An example of MPEG2 parallel linterface timing diagram

Table 7-5. The IT9130 MPEG-2 TS interface mode selection

Part Number	Operation Mode	MPEG-2 TS interface operation modes
IT9133/IT9137	MPEG-2 TS mode	Serial Output. Data is on Data[7] or Data[0].
		Parallel Output
		Disabled
IT9137	Standard USB2.0 mode	Serial Input. Data is on Data[7] or Data[0].
		Parallel Input

Table 7-6. Configurable parameters of the IT9130 MPEG-2 TS interface

Parameter	Selections
Output Mode	Parallel Output Serial Output
Output data pin of serial mode.	Data[7] or Data[0]

Bit-Order	For Parallel Mode: Data[7] can be MSB or LSB For Serial Mode: Can be MSB first or LSB first.
Style of the MPEG-2 sync byte	MPEG-2 style or DVB-T style.
Signal polarity	Clock, Sync, Valid, and Fail can be independently configured to be active high or low.
The style of MPEG Valid	Continuous or gapped.
The gap between consecutive 188-byte payloads in units of byte times.	0 ~ 255
MPEG Sync assertion for the serial output mode, select whether MPEG Sync is asserted only for the first bit or for all bits of the first byte.	Asserted for all bits of the first byte or for the first bit only.
MPEG Clock frequency	Configurable
MPEG Sync pin for the serial input mode	Can be used or wired to ground.

7.9.1.1 Parallel Output Interface

When the MPEG-2 TS interface is programmed to be the parallel output mode, each byte of the payload of the MPEG-2 transport stream will be output to Data[7]~Data[0] in parallel. MPEG Valid is asserted when a payload byte is being output on Data[7]~Data[0]. MPEG Sync is asserted at the first payload byte of each transport stream packet. MPEG Fail is asserted throughout the entire duration of any erroneous transport stream packet. Note that there can be gaps between bytes in MPEG Valid. Example timing diagrams with continuous and gapped MPEG Valid are shown in Figure 7-2 and Figure 7-3 respectively.

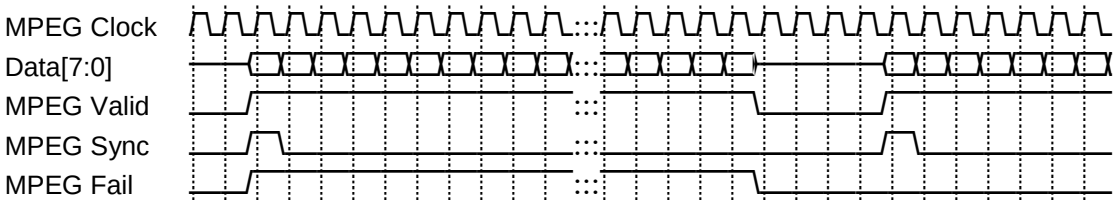


Figure 7-2. Timing diagram with continuous MPEG valid in parallel mode

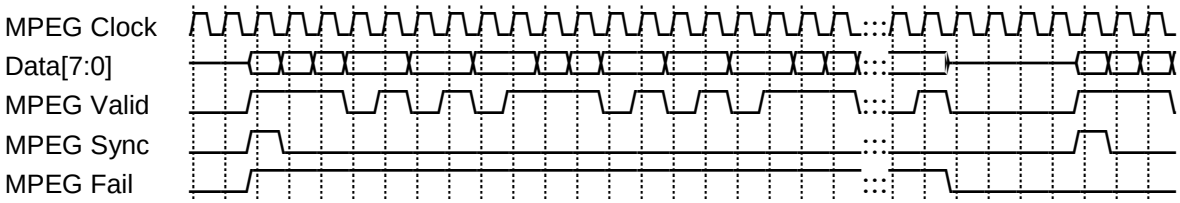


Figure 7-3. Timing diagram with gapped MPEG valid in parallel mode

7.9.1.2 Serial Output Interface

In IT9130, the MPEG TS interface can operate in the serial output mode. In the serial output mode, the payloads of MPEG-2 transport stream will be serially output on MPEG Data[7] or MPEG Data[0]. In this mode, MPEG Valid can be asserted at the first bit or entire 8 bits of the payload of the transport stream. Furthermore, there can be gaps in MPEG Valid, but there can be no gaps within the 8 bits of a byte. Example timing diagrams of MPEG Valid without and with gaps are shown in Figure 7-4 and Figure 7-5, respectively. Finally, same as in the parallel mode, for any error packet, MPEG Fail is asserted throughout the entire duration of any erroneous transport stream packet.

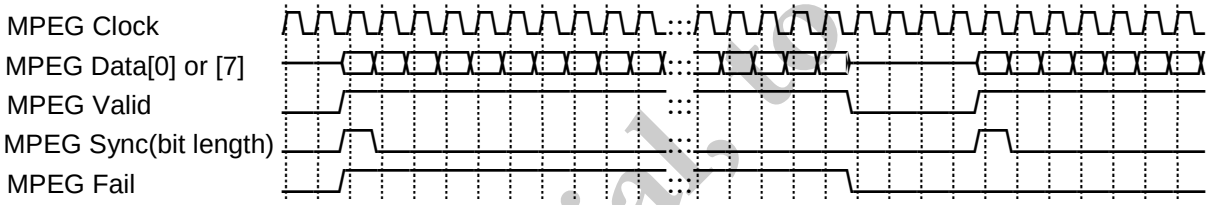


Figure 7-4. Timing diagram of continuous MPEG valid signal in serial mode

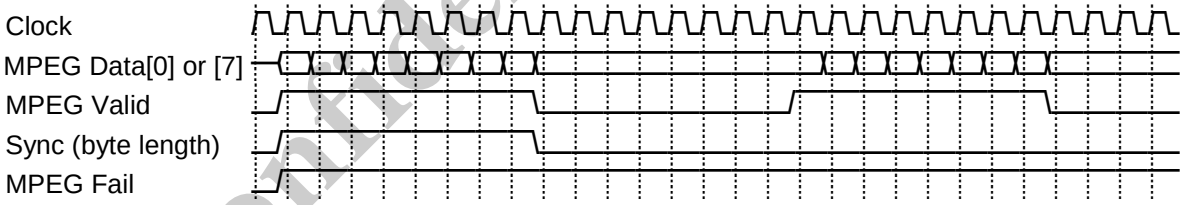
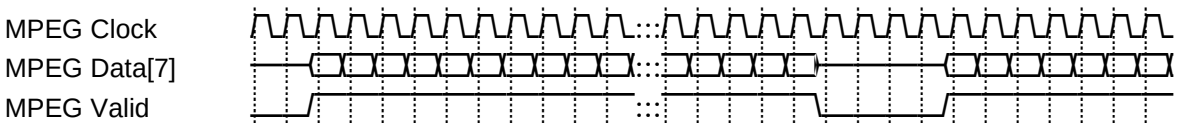


Figure 7-5. Timing diagram of gapped MPEG valid signal in serial mode

7.9.1.3 Serial and Parallel Input Interface

The MPEG TS interface of IT9130 can become an input interface for accepting a secondary MPEG2 TS stream and forwarding to the host. Both parallel and serial data are supported for receiving the secondary MPEG2 TS stream. An example timing diagram for the IT9130 MPEG2 TS serial input interface is shown in Figure 7-6.



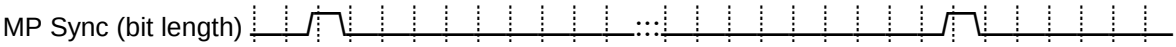


Figure 7-6. Timing diagram of the IT9130 MPEG TS serial input interface

MPEG Sync of IT9130 can be wired to the ground if MPEG Sync is not available from the MPEG TS stream provider.

7.9.2 Diversity Interface

The diversity interface of IT9130 aligns and combines 2 demodulated streams. As shown in Figure 7-7, signals are combined and transferred from one IC to another using two-way transmission between adjacent demodulators. Alignment of the two streams is performed before combining, and the corresponding maximum delay tolerance is shown in Table 7-7.

In a diversity-receiving system, one IT9137 acts as the master device and another IT9133 or IT9137 acts as the slave device. The master device takes the combined demodulated stream from the slave through the Host Interface bus and transfers to FEC. The error-corrected MPEG2 data packets are sent out through the standard USB2.0 interface. The slave device combines its own data stream with the stream received from the master device through the Host Interface. The combined stream is output to the master device through the Host Interface. The pin descriptions of the diversity interface are listed in Table 7-8 and Table 7-9 for the master and slave devices, respectively.

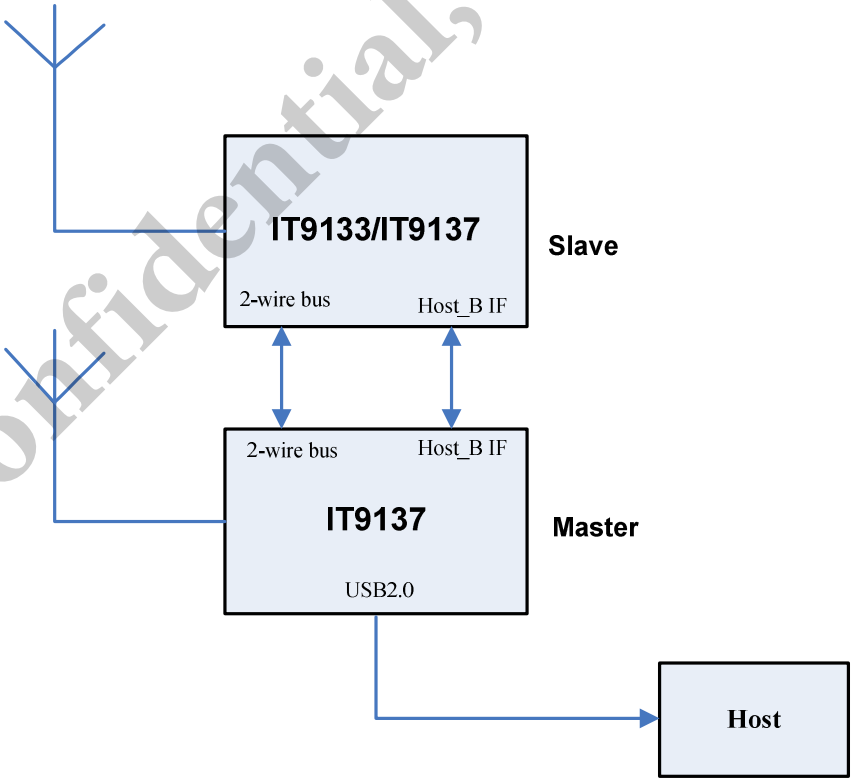


Figure 7-7. Diversity reception

Table 7-7. Maximum delay tolerance between the two streams of the diversity interface

	BW	5MHz	6MHz	7MHz	8MHz
Maximum Delay Tolerance (μs)	2K mode	358.4	298.66	256	224
	4K mode	716.8	597.33	512	448
	8K mode	716.8	597.33	512	448

Table 7-8. Diversity interface pin descriptions for the master device

Pin Name	Diversity Interface Function (Master Device)
HOST_B0	Output Data[3]
HOST_B1	Output Data[2]
HOST_B2	Output Data[1]
HOST_B3	Output Data[0]
HOST_B4	Output Valid
HOST_B5	Output Clock
HOST_B6	Input Data[3]
HOST_B7	Input Data[2]
HOST_B8	Input Data[1]
HOST_B9	Input Data[0]
HOST_B10	Input Valid
HOST_B11	Input Clock

Table 7-9. Diversity interface pin descriptions for the slave device

Pin Name	Diversity Interface Function (Slave Device)
HOST_B0	Output Clock
HOST_B1	Output Valid
HOST_B2	Output Data[0]
HOST_B3	Output Data[1]
HOST_B4	Output Data[2]
HOST_B5	Output Data[3]
HOST_B6	Input Clock
HOST_B7	Input Valid
HOST_B8	Input Data[0]

HOST_B9	Input Data[1]
HOST_B10	Input Data[2]
HOST_B11	Input Data[3]

7.10 USB Interface

IT9130 supports USB 2.0 standard with many configurable parameters in the Endpoint 0 descriptors.

7.10.1 USB Descriptors

Most strings and parameters in the descriptors are configurable in the external EEPROM, including:
Device descriptors: vender ID, product ID, device release number, manufacturer string index, product string index, serial number string index, configuration characteristics (self-powered, remote wake-up, …etc.), max power consumption, and interrupt endpoint (Endpoint 3) polling interval; and

Strings: the string description of the manufacturer and the product and the serial number. These strings are defined in USB 2.0 standard.

Please refer IT9130 Programming Guide for details on the external EEPROM.

7.10.2 USB Control Protocol

7.10.2.1 Default Endpoint (Endpoint 0)

Endpoint 0 is the same as defined in USB 2.0 standard.

7.10.2.2 Control Message

Proprietary control messages are sent through a request-and-reply model. Any request packet corresponds to a reply packet, unless the communication is malfunctioning. A sequence number field is employed in each control packet to resolve the late reply and duplicate request/reply problems.

The available control messages include those for getting the current configuration, downloading the firmware, computing firmware checksum, booting IT9130, copying the firmware to a slave device, reading and writing the IT9130 memory, as well as 2-wire bus control messages, software reset control messages, and Control Unit command control messages

7.10.2.3 Data Message

Data messages convey the MPEG2 transport streams received by IT9130.

7.11 IR Interface

IT9130 supports IR protocols such as NEC, RC5, and RC6. The IR function can be enabled or disabled and the IR protocol can be selected by appropriately setting the corresponding fields in the external EEPROM. For IT9130 operating in the standard USB 2.0 mode, it considered as a USB composite device with HID when the IR function is enabled. Otherwise it is a USB single device. More details on EEPROM settings are available in IT9130 Programming Guide. The IT9130 IR decoder decodes raw signals received from the IR photo-receiver. Then the demodulated signals are converted to HID (Human Interface Devices) format according to a translation table that is downloaded from the driver via the memory write protocol (See 7.10.2 for more details on USB control protocols). At last the USB host receives IR messages via USB Endpoint 3.

More details of the IT9130 IR interface are available in IT9130 Programming Guide.

7.11.1 The Function Keys and Alternative Keys

The function key (FN) is used to create alternative key sequences for a remote control. When FN of a remote control is pressed, an alternative key sequence is initiated, and any keys pressed are considered “alternative” if they are pressed within a predefined expiration time after the previous key press. This design enables a remote control with fewer keys (buttons) to almost double its “effective” number of keys. IT9130 will not send any key when only the function key is pressed

Alternative keys are supported in IT9130 as mentioned in IT9130 Programming Guide.

7.11.2 The External EEPROM

An external EEPROM can be used for storing USB related information and possibly other hardware related information in systems using IT9130. The content and format of the external EEPROM is given in detail in IT9130 Programming Guide.

7.11.3 Boot Scheme

Detailed boot scheme of IT9130 is described in IT9130 Programming Guide.

7.12 GPIO Interface

Please refer to IT9130 GPIO User Manual for application detail.

8. Power Mode

8.1 Power Mode

IT9130 supports the following power modes, as shown in Table 8-1:

1. Suspend – all functions are turned off except for one internal slow clock and the suspend control block. It could be initiated by USB suspend operation or by applying a high voltage on the GPIOH5 pin with appropriate parameters setting.

2. RX – all the functions are ON.

Table 8-1. Power mode table

States	Slow clock	IT9130	Host interface
Suspend	ON	OFF (Only USB PHY and control block active)	OFF
RX	ON	ON	ON

The transition time between each power state is listed in Table 8-2.

Table 8-2. IT9130 power state transition time

To / From	Suspend mode	RX mode
Suspend mode	N/A	2msec
RX mode	50 μ sec	N/A

8.2 Current Consumption

For the current consumption detail, please refer to IT9130 Power Consumption Report.

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9. Register Descriptions

Two central processors are embedded in IT9130 responsible for the register access, respectively named as Processor_LINK and Processor_OFDM. For the detail, please see IT9130 Programming Guide. Table 9-1and Table 9-2 list the register descriptions. Registers with attribute RW or RWS are read-write registers. Registers with attribute R or RS are read-only registers.

Table 9-1. List of Processor_OFDM registers

Address	Register Name	Bits	Attrib	Register Description	Default
0xF006	*reg_p_pwm_rf_if_from_hw*	0	RW	0: PWM source from micro-controller 1: PWM source from hardware	1'h1
0xF05E	*reg_p_pwm_cycle_unit[3:0]*	3:0	RW	Period of PWM = Crystal frequency / (256 x (p_pwm_cycle_unit+1))	4'h1
0xF05F	*reg_p_pwm_en*	0	RW	0: PDM generates control signal to RF/IF AGC 1: PWM generates control signal to RF/IF AGC	1'h0
0xF900	*reg_tpsd_txmod[1:0]*	1:0	R	DVB-T transmission mode (TPS bits S38, S39)	2'h0
0xF901	*reg_tpsd_gi[1:0]*	1:0	R	DVB-T guard interval (TPS bits S36, S37)	2'h0
0xF902	*reg_tpsd_hier[2:0]*	2:0	R	DVB-T hierarchy information (TPS bits S27,S28,S29)	3'h0
0xF903	*reg_tpsd_const[1:0]*	1:0	R	DVB-T constellation (TPS bits S25, S26)	2'h0
0xF904	*reg_bw[1:0]*	1:0	RW	DVB-T channel bandwidth. 00: 6MHz 01: 7MHz 10: 8MHz 11:5MHz	2'h0
0xF905	*reg_dec_pri*	0	RW	High/Low priority stream select. 0: LP 1: HP	1'h0
0xF906	*reg_tpsd_hpcr[2:0]*	2:0	R	Code Rate for HP Stream (TPS bits S30,S31,S32)	3'h0
0xF907	*reg_tpsd_lpcr[2:0]*	2:0	R	Code Rate for LP Stream (TPS bits S33,S34,S35)	3'h0
0xF908	*reg_tpsd_indep*	0	R	In-depth interleaving information (TPS bit S27)	1'h0
0xF1A3	*reg_bfs_fcw[7:0]*	7:0	RW	Carrier frequency control word	8'h0
0xF1A4	*reg_bfs_fcw[15:8]*	7:0	RW		8'h0
0xF1A5	*reg_bfs_fcw[22:16]*	6:0	RW		7'h0
0xF1B3	*fcw_q[7:0]*	7:0	RS	Carrier frequency offset	8'h0
0xF1B4	*fcw_q[15:8]*	7:0	RS		8'h0
0xF1B5	*fcw_q[22:16]*	6:0	RS		7'h0
0xF980	*psb_overflow*	0	RWS	Packet smooth buffer overflow indicator	1'h0
0xF981	*no_modify_tei_bit*	0	RW	0: Enable modification of TEI in TS output 1: Disable modification of TEI in TS output	1'h0
0xF982	*keep_sf_sync_byte*	0	RW	Style of MPEG-2 sync byte 0: MPEG-2 style. The inverted sync byte (0xB8) in DVB-T shall be inverted again so that the output sync byte is always 0x47 as required by MPEG-2. 1: DVB-T style. In this case the FEC module transfers the decoded data to the MPEG-2 TS interface without modification. The sync byte of every eighth super-frame is inverted (0xB8) according to the DVB-T specifications.	1'h0
0xF984	*mpeg_ser_do7*	0	RW	MPEG-2 interface data output at serial mode 0: Output to DATA0 1: Output to DATA1	1'h0
0xF985	*mpeg_ser_mode*	0	RW	MPEG-2 output is serial	1'h0
0xF986	*mpeg_par_mode*	0	RW	MPEG-2 output is parallel	1'h0
0xF987	*psb_empty*	0	RS	Packet smoothing buffer empty indicator	1'h0

0xF988	*ts_not_188*	0	RS	TS error signal	1'h0
0xF989	*mssync_len*	0	RW	For the MPEG serial output mode, select whether MPSTR is asserted only for the first bit or for all bits of the first byte. 0: Asserted for all bits of the first byte 1: Asserted for the first bit only	1'h0
0xF98A	*msdo_msb*	0	RW	For the serial output mode, select the endianness of the serial data output. 0: LSB first 1: MSB first For the parallel output mode, select the bit ordering of the parallel output 0: MPDATA7 is the MSB of TS data 1: MPDATA0 is the MSB of TS data	1'h1
0xF98B	*mpeg_clk_gated*	0	RW	The style of MPCLK 0: Free running. MPCLK is always present 1: Gated. There is no MPCLK when no valid data is available.	1'h0
0xF98C	*mpeg_err_pol*	0	RW	The polarity of MPFAIL 0: Active high (set to 1 to indicate error) 1: Active low	1'h0
0xF98D	*mpeg_sync_pol*	0	RW	The polarity of MPSTR 0: Active high (set to 1 to indicate frame sync) 1: Active low	1'h0
0xF98E	*mpeg_vld_pol*	0	RW	The polarity of MPFRM 0: Active high (set to 1 to indicate valid data) 1: Active low	1'h0
0xF98F	*mpeg_clk_pol*	0	RW	The polarity of MPCLK. 0: Data changes after the rising edge of MPCLK 1: Data changes after the falling edge of MPCLK	1'h0
0xF990	*reg_mpeg_full_speed*	0	RW	Full speed in mpeg interface	1'h0
0xF991	*pid_complement*	0	RW	PID table complement; 0: Pid out if table hit 1: Pid out if table not hit.	1'h0
0xF992	*pid_rst*	0	RWS	Reset PID table	1'h0
0xF993	*pid_en*	0	RW	PID_en	1'h0
0xF994	*pid_index_en*	0	RW	Enable current PID index	1'h1
0xF995	*pid_index[4:0]*	4:0	RWS	PID index	5'h0
0xF996	*pid_dat_l[7:0]*	7:0	RW	PID data register (bit 7-0)	8'h0
0xF997	*pid_dat_h[4:0]*	4:0	RW	PID data register (bit 12-8)	5'h0
0xF999	*sync_byte_locked*	0	RS	Indicate sync_byte_locked	1'h0
0xF99A	*ignore_sync_byte*	0	RW	Don't check sync byte x47	1'h1
0xF99C	*reg_mpeg_vld_tgl*	0	RW	The style of MPFRM 0: MPFRM will be sent out continuously. 1: Allow gaps in between bytes in MPFRM.	1'h0
0xF99D	*reg_mp2_sw_rst*	0	RW	MPEG software reset	1'h1
0xF99E	*psb_en*	0	RW	Packet smooth buffer enable	1'h1
0xF9A1	*lost_pkt_cnt_l[7:0]*	7:0	RS	Number of lost packet (low byte)	8'h0
0xF9A2	*lost_pkt_cnt_h[7:0]*	7:0	RS	Number of lost packet (high byte)	8'h0
0xF9A9	*reg_tpsd_bw_mp2if[1:0]*	1:0	RW	Target DVB-T channel bandwidth for MPCLK frequency control	2'h0
0xF9AA	*reg_tpsd_gi_mp2if[1:0]*	1:0	RW	Target guard interval for MPCLK frequency control	2'h0
0xF9AB	*reg_tpsd_cr_mp2if[2:0]*	2:0	RW	Target code rate for MPCLK frequency control	3'h0
0xF9AC	*reg_tpsd_cons_mp2if[1:0]*	1:0	RW	Target constellation for MPCLK frequency control	2'h0

0xF9AD	*reg_fw_table_en*	0	RW	MPCLK frequency control: 0: The frequency of MPCLK depends on the actual bandwidth and TPS parameters of the current DVB-T channel. 1: The frequency of MPCLK depends on the target values in the registers reg_tpsd_bw_mp2if, reg_tpsd_gi_mp2if, reg_tpsd_cr_mp2if, and reg_tpsd_cons_mp2if.	1'h0
0xF9B0	*reg_packet_gap[7:0]*	7:0	RW	The gap between consecutive 188-byte payloads in units of byte times. Takes values of 0 to 255. Applies to the parallel output mode and serial output mode.	8'h10
0xF9B2	*reg_ts_dat_inv*	0	RW	Serial TS input data polarity inversion. 0: Serial TS input data is not inverted. 1: Serial TS input data is inverted.	1h'0
0xF9B3	*reg_ts_lsb_1st*	0	RW	Endianness of the serial TS input 0: MSB first 1: LSB first	1h'0
0xF9B4	*reg_ts_capt_bg_sel*	0	RW	For serial TS input: 0: MPEG sync is ignored (can be wired to ground). 1: MPEG sync is used.	1'h1
0xF9B7	*reg_ts_sync_inv*	0	RW	Serial TS input sync inversion. 0: MPEG-2 sync is not inverted 1: MPEG-2 sync is inverted.	1'h0
0xF9B8	*reg_ts_vld_inv*	0	RW	Serial TS input valid inversion. 0: MPEG-2 valid is not inverted. 1: MPEG-2 valid is inverted	1'h0
9xF9CC	*reg_tsip_en*	0	RW	0: Disable parallel TS input 1: Enable parallel TS input	1'h0
0xF9CD	*reg_tsis_en*	0	RW	0: Disable serial TS input 1: Enable serial TS input	1'h0
0xF9D9	*reg_clk_sel[1:0]*	1:0	RS	Read back values related to the MPEG output clock rate: 0: clk_phy/8 1: clk_phy/4 2: clk_phy/2 3: clk_phy	2'h0
0xF9DA	*reg_tog_sel[1:0]*	1:0	RS	Read back values related to the MPEG output clock rate: 0: 5/8 1: 6/8 2: 7/8 3: 8/8	2'h0
0xF9E0	*reg_check_tpsd_hier*	0	RW	Enable reg_tpsd_hier for determining output speed 0: Don't care reg_tpsd_hier; 1: Depend on reg_tpsd_hier	1'h0

Table 9-2. List of Processor_LINK registers

Address	Register Name	Bits	Attrib	Register Description	Default
0xD800	*pwron_clk_strap[3:0]*	3:0	RS	Clock strapping information: 0000: Crystal frequency= 12MHz, 0001: Crystal frequency = 20.48MHz,	4'h0
0xD801	*pwron_mode_strap[3:0]*	3:0	RS	Peripheral mode strap info: 00xx: TS mode, I2C_address[1:0], 0001: Salve device of DCA mode 0101: USB mode Others: Reserved	4'h0
0xD806	*reg_ofsm_suspend*	0	RWS	Write 1 to enter suspend mode.	1'h0
0xD808	*wake_int*	0	RWS	External wake up interrupt status	1'h0
0xD809	*reg_top_pwrdw_hwen*	0	RW	Enable hardware suspend function without interrupting MCU 0: Disable 1: Enable	1'h0
0xD80A	*reg_top_pwrdw_inv*	0	RW	Hardware suspend polarity (via GPIOH5)	1'h0
0xD80C	*wake_int_en*	0	RW	Enable external wake up interrupt	1'h0
0xD80D	*pwrdw_int*	0	RWS	Hardware suspend interrupt status	1'h0
0xD81A	*reg_top_clkoen*	0	RW	Enable CLKO output	1'h1
0xD830	*reg_top_padmiscdr2*	0	RW	Bit 0 of output driving control	1'h0
0xD831	*reg_top_padmiscdr4*	0	RW	Bit 1 of output driving control	1'h1
0xD832	*reg_top_padmiscdr8*	0	RW	Bit 2 of output driving control	1'h0
0xD833	*reg_top_padmiscdrsr*	0	RW	MPEG output slew rate control: 0: Default 1: Slew rate boosts	1'h0
0xD8AE	*reg_top_gpioh1_i*	0	RS	GPIOh1 input	1'h0
0xD8AF	*reg_top_gpioh1_o*	0	RW	GPIOh1 output	1'h0
0xD8B0	*reg_top_gpioh1_en*	0	RW	GPIOh1 output enable 1: Output mode 0: Input mode	1'h0
0xD8B1	*reg_top_gpioh1_on*	0	RW	GPIOh1 enable	1'h0
0xD8B2	*reg_top_gpioh3_i*	0	RS	GPIOh3 input	1'h0
0xD8B3	*reg_top_gpioh3_o*	0	RW	GPIOh3 output	1'h0
0xD8B4	*reg_top_gpioh3_en*	0	RW	GPIOh3 output enable 1: Output mode 0: Input mode	1'h0
0xD8B5	*reg_top_gpioh3_on*	0	RW	GPIOh2 enable	1'h0
0xD8B6	*reg_top_gpioh2_i*	0	RS	GPIOh2 input	1'h0
0xD8B7	*reg_top_gpioh2_o*	0	RW	GPIOh2 output	1'h0
0xD8B8	*reg_top_gpioh2_en*	0	RW	GPIOh2 output enable 1: Output mode 0: Input mode	1'h0
0xD8B9	*reg_top_gpioh2_on*	0	RW	GPIOh2 enable	1'h0
0xD8BA	*reg_top_gpioh5_i*	0	RS	GPIOh5 input	1'h0
0xD8BB	*reg_top_gpioh5_o*	0	RW	GPIOh5 output	1'h0
0xD8BC	*reg_top_gpioh5_en*	0	RW	GPIOh5 output enable 1: Output mode 0: Input mode	1'h0
0xD8BD	*reg_top_gpioh5_on*	0	RW	GPIOh5 enable	1'h0

0xD8BE	*reg_top_gpioh4_i*	0	RS	GPIOh4 input	1'h0
0xD8BF	*reg_top_gpioh4_o*	0	RW	GPIOh4 output	1'h0
0xD8C0	*reg_top_gpioh4_en*	0	RW	GPIOh4 output enable 1: Output mode 0: Input mode	1'h0
0xD8C1	*reg_top_gpioh4_on*	0	RW	GPIOh4 enable	1'h0
0xD8C2	*reg_top_gpioh7_i*	0	RS	GPIOh7 input	1'h0
0xD8C3	*reg_top_gpioh7_o*	0	RW	GPIOh7 output	1'h0
0xD8C4	*reg_top_gpioh7_en*	0	RW	GPIOh7 output enable 1: Output mode 0: Input mode	1'h0
0xD8C5	*reg_top_gpioh7_on*	0	RW	GPIOh7 enable	1'h0
0xD8C6	*reg_top_gpioh6_i*	0	RS	GPIOh6 input	1'h0
0xD8C7	*reg_top_gpioh6_o*	0	RW	GPIOh6 output	1'h0
0xD8C8	*reg_top_gpioh6_en*	0	RW	GPIOh6 output enable 1: Output mode 0: Input mode	1'h0
0xD8C9	*reg_top_gpioh6_on*	0	RW	GPIOh6 enable	1'h0
0xD8CE	*reg_top_gpioh8_i*	0	RS	GPIOh6 input	1'h0
0xD8CF	*reg_top_gpioh8_o*	0	RW	GPIOh6 output	1'h0
0xD8D0	*reg_top_gpioh8_en*	0	RW	GPIOh8 output enable 1: Output mode 0: Input mode	1'h0
0xD8D1	*reg_top_gpioh8_on*	0	RW	GPIOh8 enable	1'h0
0xD8EE	*reg_top_lock2_out*	0	RW	GPIOH2 is used as lock indicator	1'h0
0xD8EF	*reg_top_lock2_tpsd*	0	RW	GPIOH2 lock indication 1: TPS lock 0: MPEG lock	1'h0
0xD8F3	*reg_top_lock1_out*	0	RW	GPIOH1 is used as lock indicator	1'h0
0xD8F4	*reg_top_lock1_tpsd*	0	RW	GPIOH1 lock indication 1: TPS lock 0: MPEG lock	1'h0
0xD8F8	*reg_top_lock4_out*	0	RW	GPIOH4 is used as lock indicator	1'h0
0xD8F9	*reg_top_lock4_tpsd*	0	RW	GPIOH4 lock indication 1: TPS lock 0: MPEG lock	1'h0
0xD8FD	*reg_top_lock3_out*	0	RW	GPIOH3 is used as lock indicator	1'h0
0xD8FE	*reg_top_lock3_tpsd*	0	RW	GPIOH3 lock indication 1: TPS lock 0: MPEG lock	1'h0
0xD902	*reg_top_pwm0_en*	0	RW	PWM0 enable	1'h0
0xD903	*reg_top_pwm1_en*	0	RW	PWM1 enable	1'h0
0xD904	*reg_top_pwm2_en*	0	RW	PWM2 enable	1'h0
0xD905	*reg_top_pwm3_en*	0	RW	PWM3 enable	1'h0
0xD907	*reg_top_pwm0_pos[2:0]*	2:0	RW	PWM positions	3'h0
0xD908	*reg_top_pwm0_width[1:0]*	1:0	RW	PWM pulse width	2'h0
0xD909	*reg_top_pwm0_duration[7:0]*	7:0	RW	PWM duration (0 to 255 maps to 0% to 99.6%)	8'h0
0xD90B	*reg_top_pwm1_pos[2:0]*	2:0	RW	PWM positions	3'h0
0xD90C	*reg_top_pwm1_width[1:0]*	1:0	RW	PWM pulse width	2'h0
0xD90D	*reg_top_pwm1_duration[7:0]*	7:0	RW	PWM duration (0 to 255 maps to 0% to 99.6%)	8'h0

0xD90F	*reg_top_pwm2_pos[2:0]*	2:0	RW	PWM positions	3'h0
0xD910	*reg_top_pwm2_width[1:0]*	1:0	RW	PWM pulse width	2'h0
0xD911	*reg_top_pwm2_duration[7:0]*	7:0	RW	PWM duration (0 to 255 maps to 0% to 99.6%)	8'h0
0xD913	*reg_top_pwm3_pos[2:0]*	2:0	RW	PWM positions	3'h0
0xD914	*reg_top_pwm3_width[1:0]*	1:0	RW	PWM pulse width	2'h0
0xD915	*reg_top_pwm3_duration[7:0]*	7:0	RW	PWM duration (0 to 255 maps to 0% to 99.6%)	8'h0
0xD91B	*reg_top_hostb_mpeg_par_mode*	0	RW	Host B TS mode register, 1: mpeg parallel mode	1'h0
0xD91C	*reg_top_hostb_mpeg_ser_mode*	0	RW	Host B TS mode register, 1: mpeg serial mode	1'h0
0xD91D	*reg_top_hostb_mpeg_ser_do7*	0	RW	0: Host_B mpeg serial mode data out by pin data0 1: Host_B mpeg serial mode data out by pin data7	1'h0
0xD91E	*reg_top_hostb_dca_upper*	0	RW	Host B TS mode register, 1: connect to DCA upper chip	1'h0
0xD91F	*reg_top_hostb_dca_lower*	0	RW	Host B TS mode register, 1: connect to DCA lower chip	1'h0
0xD920	*reg_top_host_reverse*	0	RW	Reverse all Host_B pins in order	1'h0
0xF103	*reg_one_cycle_counter_tuner[7:0]*	7:0	RWS	2-Wire interface speed control in units of 400 ns Period of SCL = (reg_one_cycle_counter_tuner * 400) ns	8'h10

10. DC Characteristics

10.1 Absolute Maximum Ratings*

Table 10-1. IT9130 absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Core Power Voltage	VDD1	-0.3	1.32	V
I/O Power Voltage	VDDIO	-0.3	3.6	V
USB Power Supply	AVDDHP	-0.3	3.6	V
Internal Regulator Power Voltage	VDDAH_REG VDDIO	-0.3	3.6	V
Voltage on input pins	VI	-0.3	VDDIO+0.3	V
Voltage on output pins	VO	-0.3	VDDIO+0.3	V
Storage Temperature	Tstg	-40	150	ºC
Junction Temperature	Tj		125	ºC

QFN48 Junction-Ambient Thermal Resistance (2-layer PCB)	Air Flow	0	1	2	3	m/s
	Rth(j-a)	68.9	55.1	49.7	47	ºC/W
QFN48 Junction-Ambient Thermal Resistance (4-layer PCB)	Air Flow	0	1	2	3	m/s
	Rth(j-a)	26.2	23	21.7	21.1	ºC/W
QFN56 Junction-Ambient Thermal Resistance (2-layer PCB)	Air Flow	0	1	2	3	m/s
	Rth(j-a)	63.1	50.5	45.5	43	ºC/W
QFN56 Junction-Ambient Thermal Resistance (4-layer PCB)	Air Flow	0	1	2	3	m/s
	Rth(j-a)	24.4	21.4	20.2	19.7	ºC/W

***Comments**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

10.2 Operating Conditions

Table 10-2. IT9130 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
VHF band III frequency range	IN_VHF	170		240	MHz
UHF band frequency range	IN_UHF	470		862	MHz
Core Power	VDD1	1.08	1.2	1.3	V
I/O Power Voltage	VDDIO	2.97	3.3	3.6	V
Power for USB	AVDDHP	2.97	3.3	3.6	V

Internal Regulator Power Supply	VDDAH_REG VDDIO	3.0	3.3	3.6	V
Ambient Operating Temperature (Commercial)	Ta	0		70	ºC

10.3 DC Electrical Characteristics

Table 10-3. IT9130 DC electrical characteristics

Note: RF_VDD=3.3V, VDD1=1.2V, VDDIO=3.3V, AVDDHP=3.3V, and Ta=25 ºC unless otherwise specified.

Parameter	Symbol	Test Condition	Min.	Typ	Max.	Unit
High Level Input Voltage for 3.3v IO	VIH		2.0			V
Low Level Input Voltage for 3.3v IO	VIL				0.8	V
Input Capacitance	Cin			3		pF
Power Consumption (Operating, with internal voltage regulator)	P_{op}*	USB mode			547	mW
		MPEG-TS mode			508	mW
Power Consumption (Suspend, with internal voltage regulator)	P_{sus}	Suspend (USB)			2.2	mW
		Suspend (by GPIOH5)			0.5	
High Level Output Voltage for 3.3v IO	VOH		3.0			V
Low Level Output Voltage for 3.3v IO	VOL				0.4	V
High/Low Level Output Current	IOH/IOL	Digital Output Pins	0		4	mA
High/Low Level Output Current	IOH/IOL	5V tolerant Open-Drain	0		2	mA

Note: *Test signal: 8MHz BW, 8K mode, 64QAM, Code Rate 7/8, GI 1/32 for DVB-T.

11. AC Characteristics

11.1 MPEG-2 TS Output

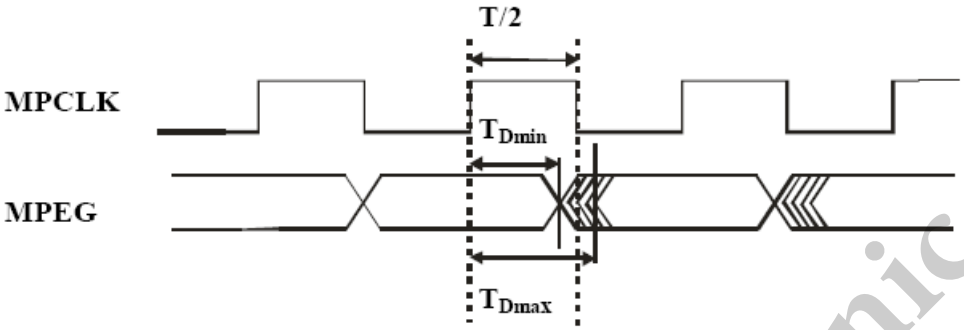


Figure 11-1. IT9130 MPEG-2 TS output timing diagram

Table 11-1. IT9130 MPEG-2 TS output timing

Parameter	Description	Min.	Max.	Unit
T/2	a half MPCLK clock cycle			ns
T_{Dmin}	Minimum valid delay	3	NA	ns
T_{Dmax}	Maximum valid delay	NA	6.5	ns

11.2 MPEG-2 TS Input

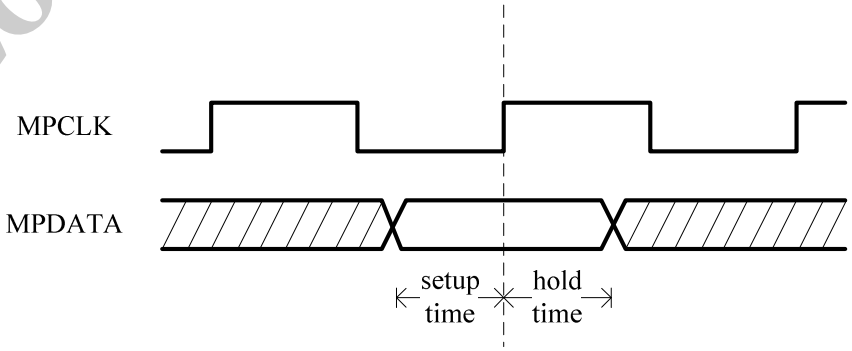


Figure 11-2. IT9130 MPEG-2 TS input timing diagram

Table 11-2. IT9130 MPEG-2 TS input timing

Parameter	Requirement	Unit
Input Set-up Time	8.29	ns
Input Hold Time	0	ns

11.3 2-Wire Bus Output Timing

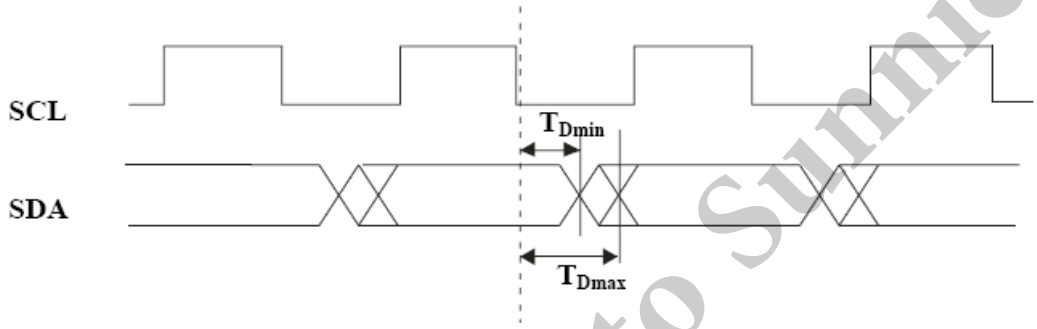


Figure 11-3. IT9130 2-wire bus output timing diagram.

Table 11-3. IT9130 2-wire bus output timing.

Parameter	Description	Min.	Max.	Unit
T_{Dmin}	Minimum valid delay of 2-wire bus output	T/2 + 2	NA	ns
T_{Dmax}	Maximum valid delay of 2-wire bus output	NA	T/2+6	ns

11.4 2-Wire Bus Input Timing

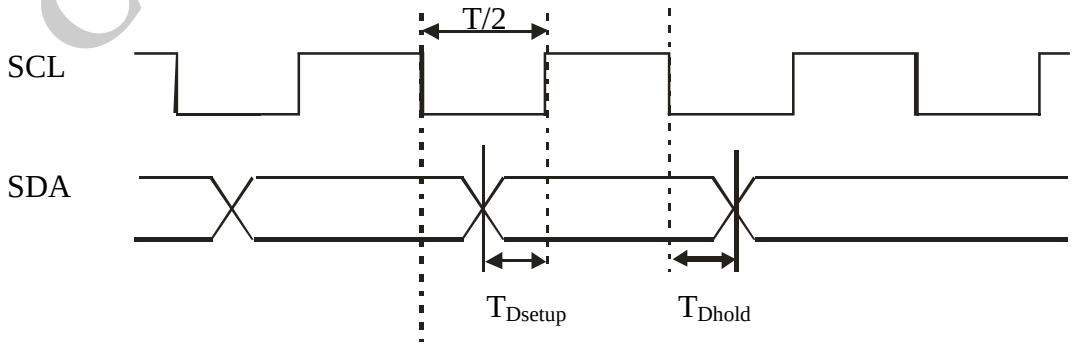


Figure 11-4. IT9130 2-wire bus input timing diagram.

Table 11-4. IT9130 2-wire bus input timing.

Parameter	Description	Min.	Max.	Unit
T_{Dsetup}	2-wire bus input setup time	2	T/2 -2	ns
T_{Dhold}	2-wire bus input hold time	2	T/2 -2	ns

11.5 Diversity Interface Input Timing

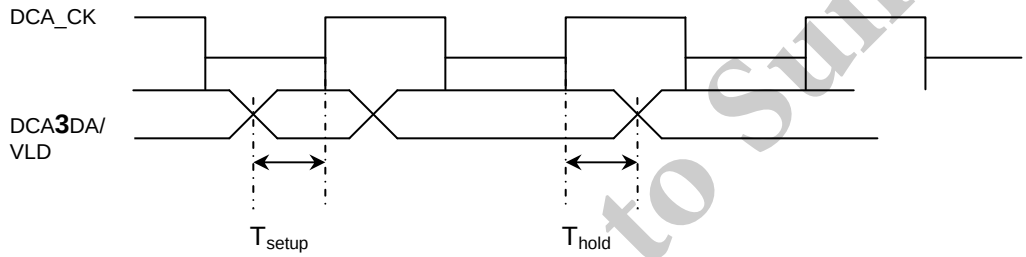


Figure 11-5. IT9130 diversity input timing diagram

Table 11-5. IT9130 diversity input timing (default setting)

Parameter	Description	Requirement	Unit
T_{setup}	Setup Time	0.7	ns
T_{hold}	Hold Time	2.6	ns

11.6 Diversity Interface Output Timing

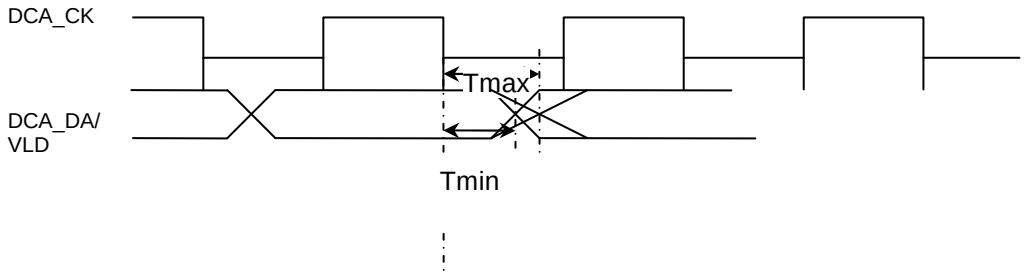


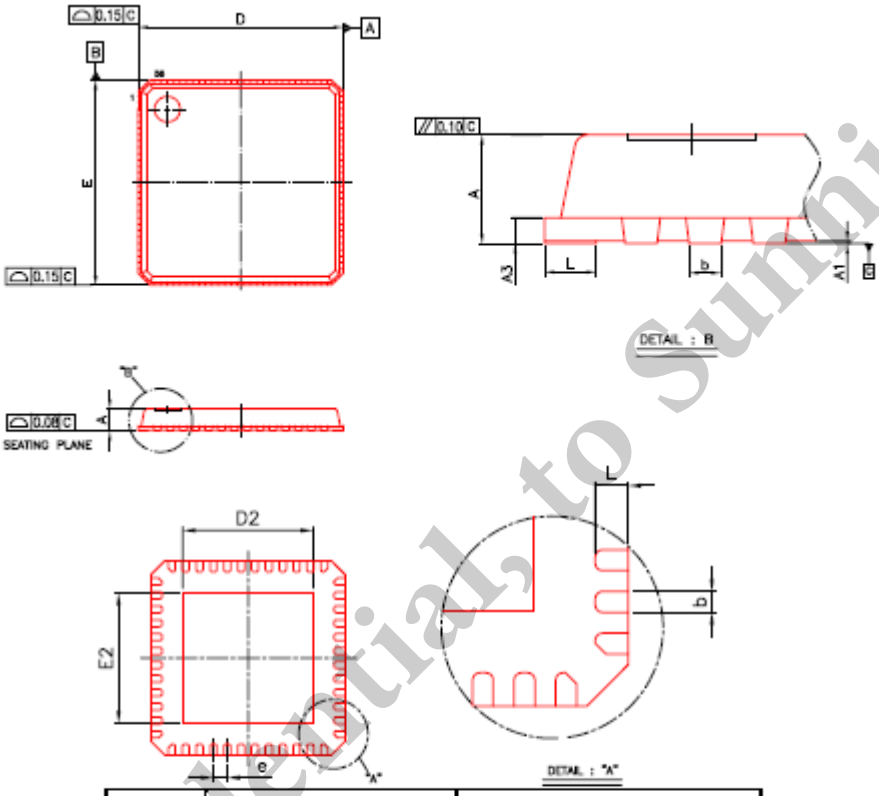
Figure 11-6. IT9130 diversity output timing diagram

Table 11-6. IT9130 diversity output timing

Parameter	Description	Min.	Max.	Unit
T_{min}	Minimum data/valid delay	2.28	NA	ns
T_{max}	Maximum data/valid delay	NA	8.69	ns

12. Package Information

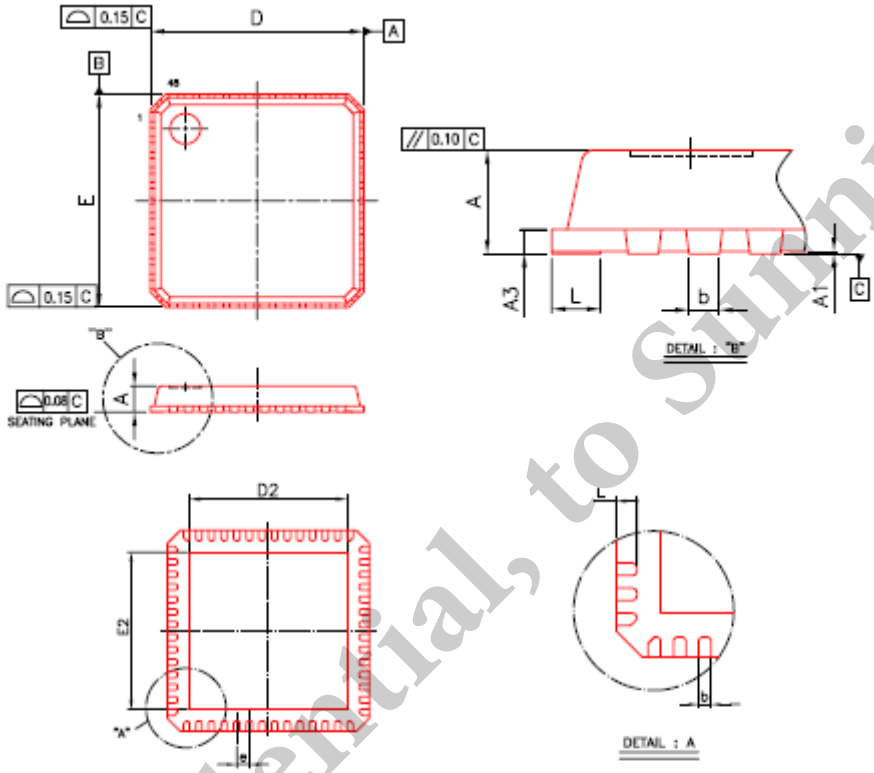
IT9133FN/ IT9135FN – QFN48



Symbol	Dimensions in inches			Dimensions in mm		
A	0.031	0.033	0.035	0.80	0.85	0.90
A1	0.000	0.001	0.002	0.00	0.02	0.05
A3	0.008 REF			0.20 REF		
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.272	0.276	0.280	6.90	7.00	7.10
D2	0.193	0.207	0.221	4.90	5.25	5.61
E	0.272	0.276	0.280	6.90	7.00	7.10
E2	0.193	0.207	0.221	4.90	5.25	5.61
e	0.020 BSC			0.50 BSC		
L	0.012	0.016	0.020	0.30	0.40	0.50

Notes:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT : JEDEC MO-220.

IT9137FN – QFN56



Symbol	Dimensions in inches			Dimensions in mm		
A	0.031	0.033	0.035	0.80	0.85	0.90
A1	0.000	0.001	0.002	0.00	0.02	0.05
A3	0.008 REF			0.20 REF		
b	0.007	0.0010	0.012	0.18	0.25	0.30
D	0.311	0.315	0.319	7.90	8.00	8.10
D2	0.165	---	0.244	4.20	---	6.20
E	0.311	0.315	0.319	7.90	8.00	8.10
E2	0.165	---	0.244	4.20	---	6.20
e	0.020 BSC			0.50 BSC		
L	0.012	0.016	0.020	0.30	0.40	0.50

Notes:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT : JEDEC MO-220.

13. Ordering Information

Part Number	Description	Package	Body Size
IT9133FN/BX	DVB-T front-end receiver with MPEG2 TS interface for UHF/VHF DVB-T receptions.	QFN 48	7mm × 7mm
IT9135FN/BX	DVB-T front-end receiver with USB2.0 interface for UHF/VHF DVB-T receptions.	QFN 48	7mm × 7mm
IT9137FN/BX	DVB-T front-end receiver with USB2.0, MPEG2 TS interface for UHF/VHF DVB-T receptions, dual-channel receptions supported.	QFN 56	8mm × 8mm

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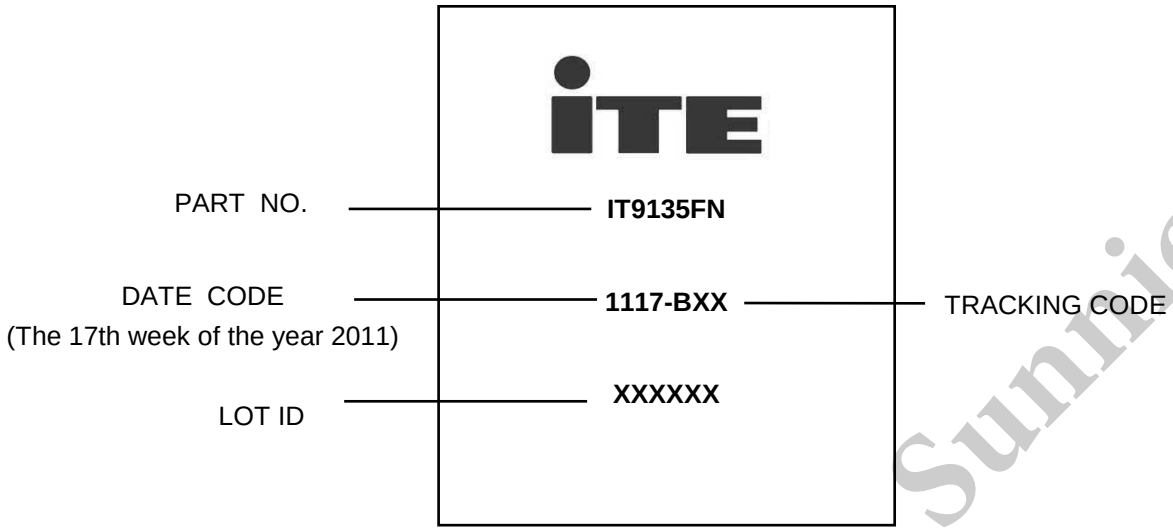
14. Top Marking Information



ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2005)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc..

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.

(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.

(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.

(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.

(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).

(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.

(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.

(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.

(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.

(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.

(c) Buyer will not return any goods without first obtaining a customer return order number.

(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.

(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.

(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.