IW Input Bits / Control Output Bits

	27	26	25	24	23	22	21	20	RFW	EXTop1	EXTop0	ALUSrcB	ALUOp2	ALUOp1	ALUOp0
add(r)	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0
add(i)	0	0	1	0	1	0	0	0	1	0	0	1	0	0	0
mov(r)	0	0	0	1	1	0	1	0	1	0	0	0	0	1	1
mov(i)	0	0	1	1	1	0	1	0	1	0	0	1	0	1	1
sub(r)	0	0	0	0	0	1	0	0	1	0	0	0	0	0	1
sub(i)	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1
rsb(r)	0	0	0	0	0	1	1	0	1	0	0	0	1	0	0
rsb(i)	0	0	1	0	0	1	1	0	1	0	0	1	1	0	0
and(r)	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1
and(i)	0	0	1	0	0	0	0	0	1	0	0	1	1	0	1
cmp(r)	0	0	0	1	0	1	0	1	0	0	0	0	0	0	1
cmp(i)	0	0	1	1	0	1	0	1	0	0	0	1	0	0	1
mvn(i)	0	0	1	1	1	1	1	0	1	0	0	1	1	1	0
lsl(r)	0	0	0	1	1	0	1	0	1	1	1	0	0	1	1
lsl(i)	0	0	0	1	1	0	1	0	1	1	1	1	0	1	1
lsr(r)	0	0	0	1	1	0	1	0	1	1	1	0	0	1	1
lsr(i)	0	0	0	1	1	0	1	0	1	1	1	1	0	1	1
asr(r)	0	0	0	1	1	0	1	0	1	1	1	0	0	1	1
asr(i)	0	0	0	1	1	0	1	0	1	1	1	1	0	1	1
ldr(r)	0	1	1	1	1	0	0	1	1	0	0	0	0	0	0
ldr(i)(down)	0	1	0	1	0	0	0	1	1	0	1	1	0	0	1
ldr(i)(up)	0	1	0	1	1	0	0	1	1	0	1	1	0	0	0
str(r)	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
str(i)(down)	0	1	0	1	0	0	0	0	0	0	1	1	0	0	1
str(i)(up)	0	1	0	1	1	0	0	0	0	0	1	1	0	0	0
mul	0	0	0	0	0	0	X	X	1	0	0	0	0	1	0
b	1	0	1	0	X	X	X	X	0	1	0	1	0	0	0
bl	1	0	1	1	X	X	X	X	1	1	0	1	0	0	0
bx	0x12FFF1								0	0	0	0	0	0	0

	PCSel1	PCSel0	RR0Sel1	RR0Sel0	RR1Sel0	RR2Sel0	WRSel1	WRSel0	WDSel	MR	MW	CPSRW	SHen	Decode Rom		
add(r)	0	0	0	0	0	0	0	0	0	0	0	0	0	10000000000000000000	00001000	20
add(i)	0	0	0	0	0	0	0	0	0	0	0	0	0	10010000000000000000	00101000	20
mov(r)	0	0	0	0	0	1	0	0	0	0	0	0	1	10000110000010000001	00011010	
mov(i)	0	0	0	0	0	0	0	0	0	0	0	0	0	10010110000000000000	00111010	
sub(r)	0	0	0	0	0	0	0	0	0	0	0	0	0	10000010000000000000	00000100	
sub(i)	0	0	0	0	0	0	0	0	0	0	0	0	0	10010010000000000000	00100100	
rsb(r)	0	0	0	0	0	0	0	0	0	0	0	0	0	10001000000000000000	00000110	
rsb(i)	0	0	0	0	0	0	0	0	0	0	0	0	0	10011000000000000000	00100110	
and(r)	0	0	0	0	0	0	0	0	0	0	0	0	0	10001010000000000000	00000000	
and(i)	0	0	0	0	0	0	0	0	0	0	0	0	0	10011010000000000000	00100000	
cmp(r)	0	0	0	0	0	0	0	0	0	0	0	1	0	00000010000000000010	00010101	
cmp(i)	0	0	0	0	0	0	0	0	0	0	0	1	0	00010010000000000010	00110101	
mvn(i)	0	0	0	0	0	0	0	0	0	0	0	0	0	10011100000000000000	00111110	
lsl(r)	0	0	1	1	0	0	0	0	0	0	0	0	1	11100110011000000001	00011010	
lsl(i)	0	0	1	1	0	0	0	0	0	0	0	0	1	11110110011000000001	00011010	
lsr(r)	0	0	1	1	0	0	0	0	0	0	0	0	1	11100110011000000001	00011010	
lsr(i)	0	0	1	1	0	0	0	0	0	0	0	0	1	11110110011000000001	00011010	
asr(r)	0	0	1	1	0	0	0	0	0	0	0	0	1	11100110011000000001	00011010	
asr(i)	0	0	1	1	0	0	0	0	0	0	0	0	1	11110110011000000001	00011010	
ldr(r)	0	0	0	0	0	1	0	0	0	1	0	0	1	10000000000010001001	01111001	
ldr(i)(down)	0	0	0	0	0	0	0	0	0	1	0	0	0	10110010000000001000	01010001	
ldr(i)(up)	0	0	0	0	0	0	0	0	0	1	0	0	0	10110000000000001000	01011001	
str(r)	0	0	0	0	0	1	0	0	0	0	1	0	1	00000000000010000101	01111000	
str(i)(down)	0	0	0	0	1	0	0	0	0	0	1	0	0	00110010000100000100	01010000	
str(i)(up)	0	0	0	0	1	0	0	0	0	0	1	0	0	00110000000100000100	01011000	
mul	0	0	1	0	0	0	1	0	0	0	0	0	0	10000100010001000000		
b	0	1	0	1	0	0	0	0	0	0	0	0	0	01010000101000000000		
bl	0	1	0	1	0	0	0	1	1	0	0	0	0	11010000101000110000		
bx	1	0	0	0	0	0	0	0	0	0	0	0	0	00000001000000000000