

Spreadsheet tips

SDT (ldr / str)

Shifting (lsl, lsr)

Conditional Execution

Data Path
Control Unit

add(r)

ldr(r)

add(i)

ldr(i)(dn)

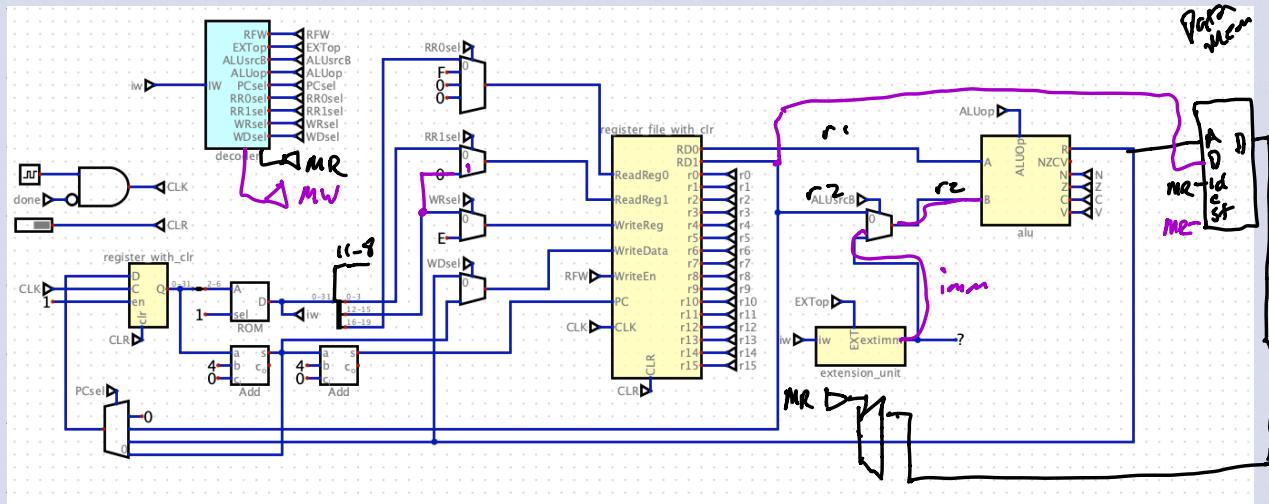
mov(r)

ldr(i)(up)

mov(i)

ldr r0, [r1, #4]
ldr r0, [r1, #-8]

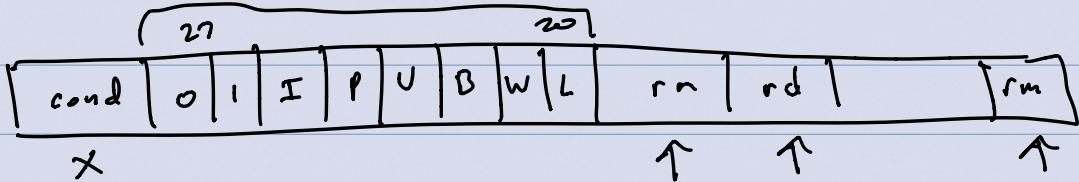
SDT (ldr / str)



ldr(r)

ldr r0, [r1, r2] *

8 bits



0b 01111001

ldr c:(<dn>)

ldr r0,[r1,#-4]

r1

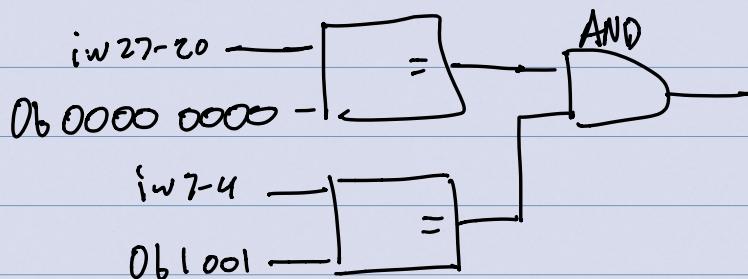
$ALU_{src} = 1$
 $ALU_{op} = sub\ 010$
 $ExtOp = 01$

R R R
str r0,[r1,r2] X

str r0,[r1] \Rightarrow str r0,[r1];#0]
str(r1) (up)

str r0,[r1,#4]
str r0,[r1,#-4] str(c:(<dn>))

Multiply

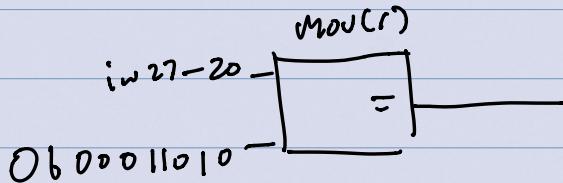


Shifting with LSL/LSR

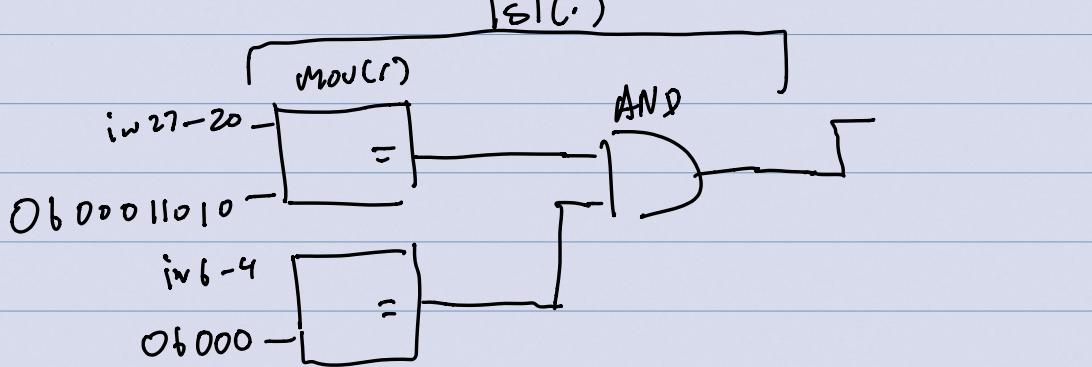
Decoder

$\text{mov}(r) + \text{shift bits}$

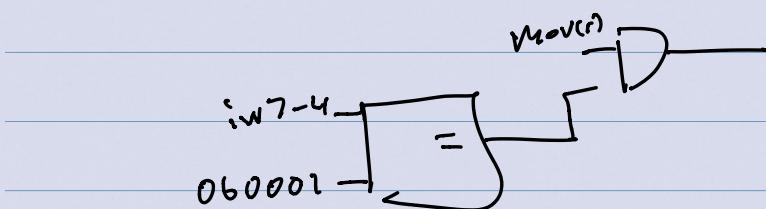
$ls1(r)$
 $\rightarrow ls1(i)$
 $ls1(r)$
 $ls1(i)$



$ls1(i)$

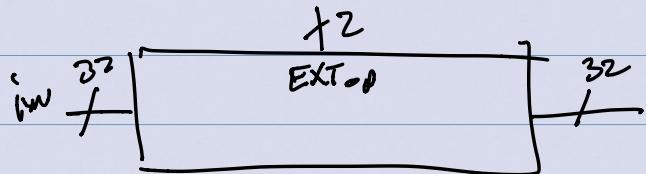


$ls1(r)$ $ls1(r_0, r_1, r_2)$ $r_0 = r_1 \ll r_2$

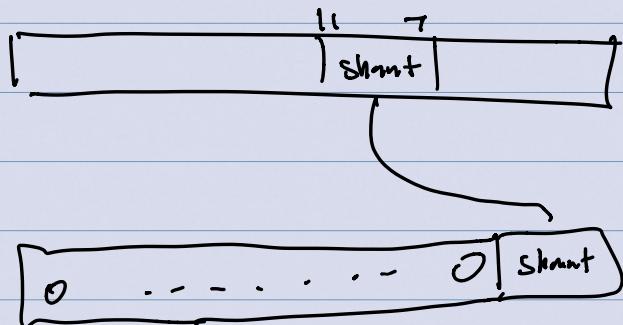


LS1/LSR Datapath

We need bits 11-7 to go to the Extender



- | | |
|----|--------------------------------|
| 00 | 8 bit zero extend |
| 01 | 12 bit zero extend |
| 10 | 24 bit sign extend \times^4 |
| 11 | 5 bit shift amount zero extend |

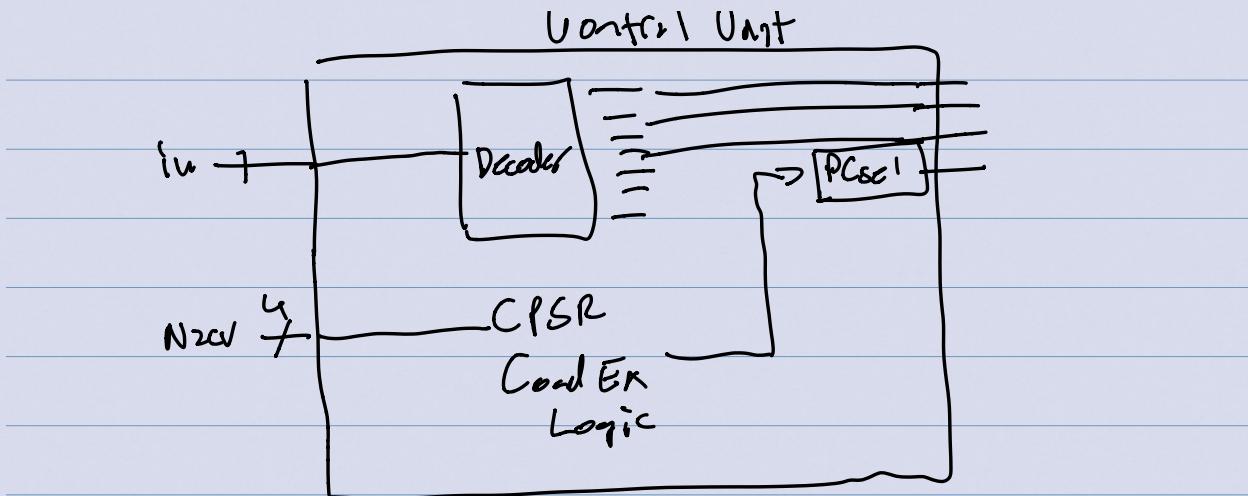


Control Unit

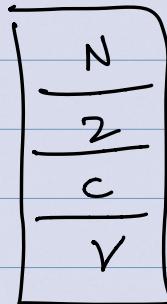
Conditional Execution

breq, bnc, blt, bge

Cmp r^o, #0 → NZCV → CPSR
breq foo ← Cond + CPSR $\stackrel{\text{reg}}{=}$ NZCV



$CPSR \rightarrow \text{Registers}$



Conditional Execution

1) On cmp store NZCV into CPSR reg
in Control Unit

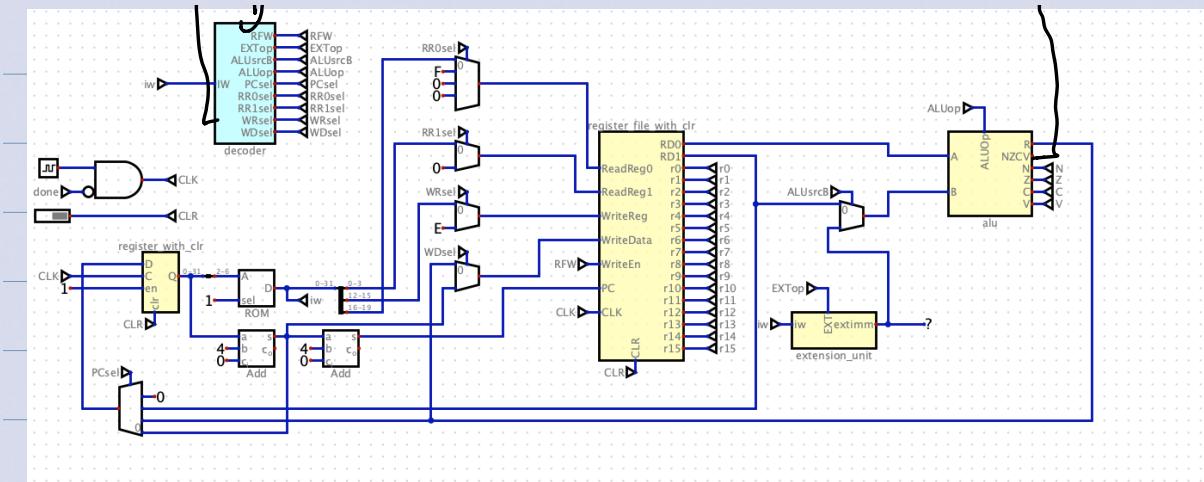
2) On execution of conditional branch

check cond code and cond conditions

if true \rightarrow take branch

if false \rightarrow go to PC + 4





CPSPW CPSR Write

true if decoded a (mpc:) (mpcr)

cond

