

## Project 05

### Review

wires, gates (and, or, not)

inputs and outputs

combinational logic

sum-of-products

sequential logic

clock, circuits that can hold values

SR Latch  $\rightarrow$  D Latch  $\rightarrow$  D flipflop (1 bit reg)

D Latch w/ CLR      D flipflop w/ CLR

n-bit Register

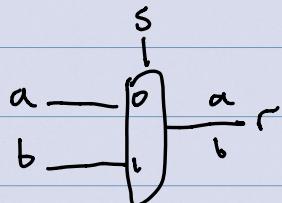
n-bit Counter (adder + register)

Digital ROM components

c-analyze (Project 05 implemented in C)

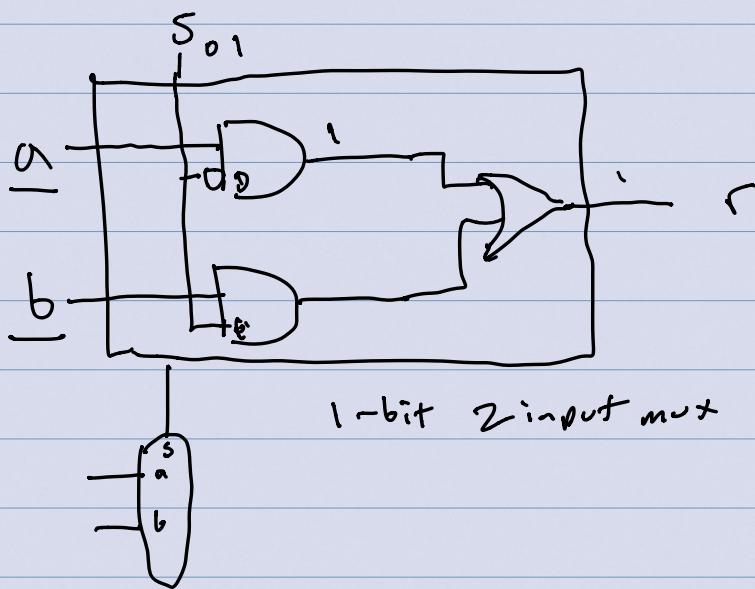
### Multiplexor

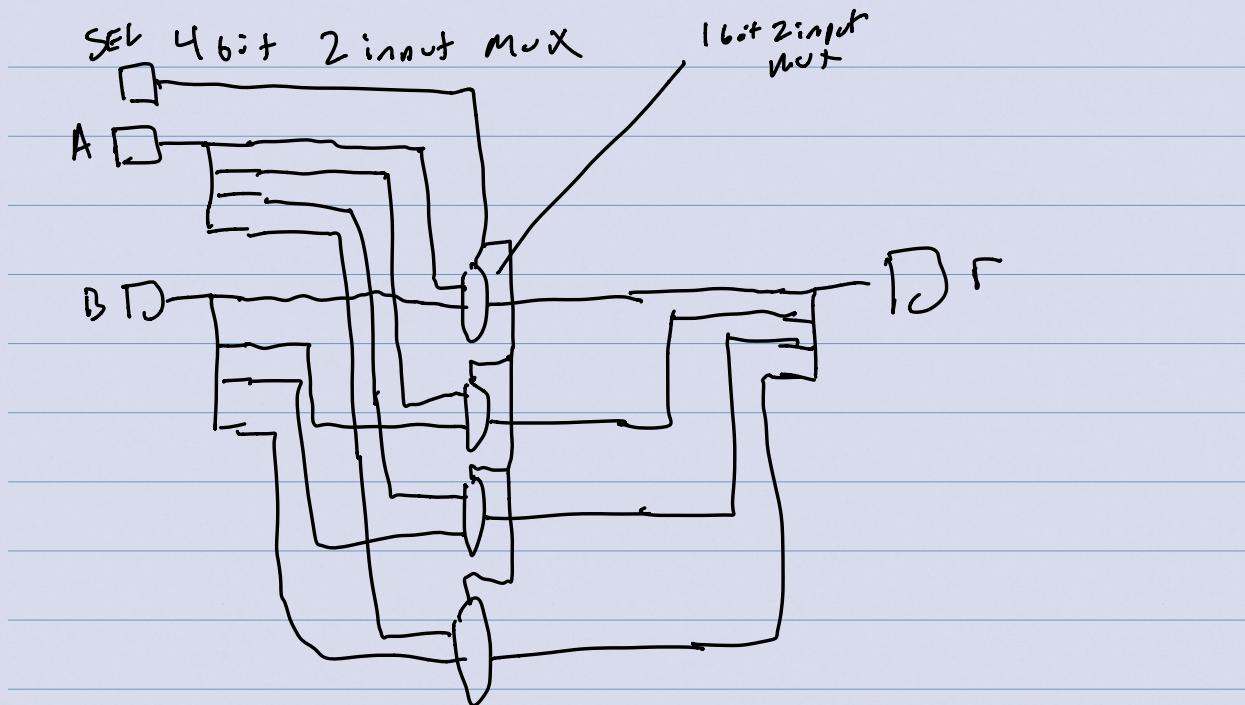
1bit 2 input MUX



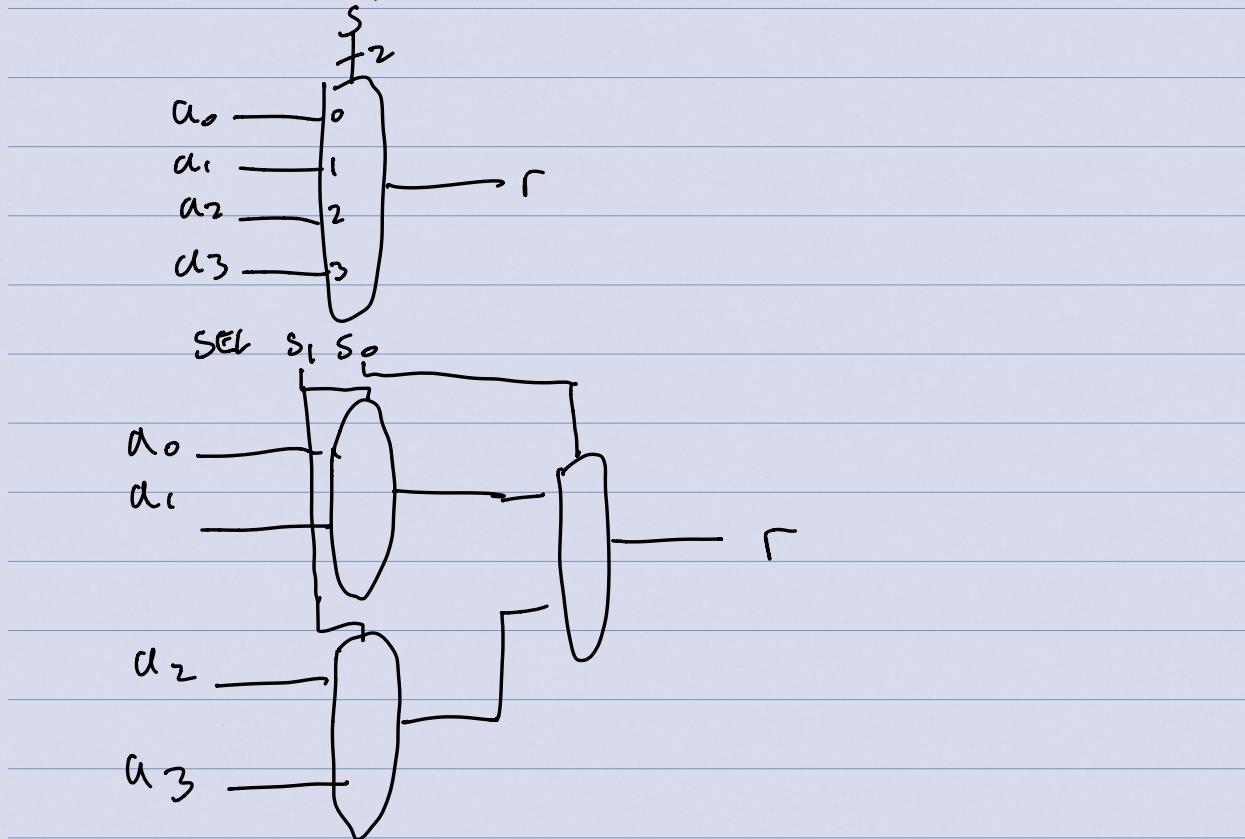
a	b	s	r
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

sum-of-products





1-bit 4 input MUX?



## Comparison Equality



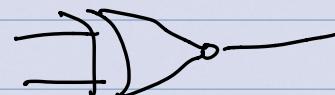
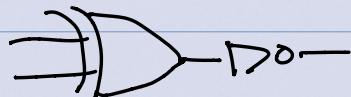
$1$  if equal  
 $0$  if not equal

$a$	$b$	EQ
0	0	1 *
0	1	0
1	0	0
1	1	1 *

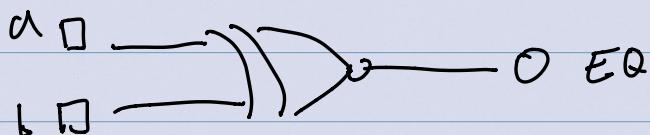
$$EQ = (\bar{a} \cdot \bar{b}) + (a \cdot b)$$

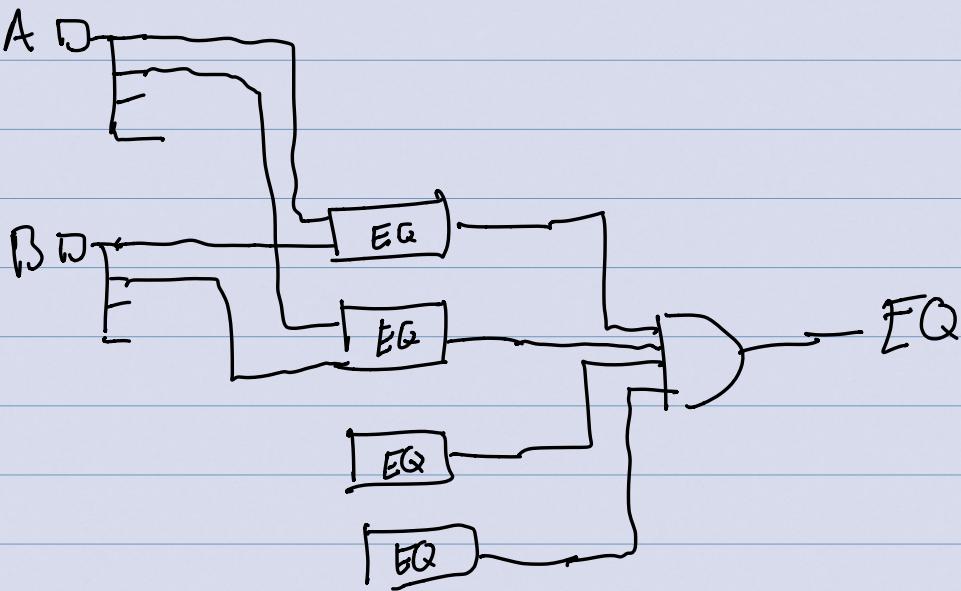
XNOR

$a$	$b$	XNOR
0	0	0
0	1	1
1	0	1
1	1	0



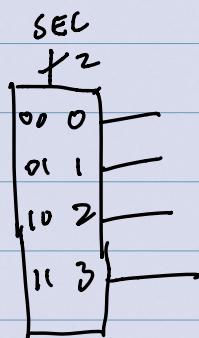
1 bit comparator





Decoder

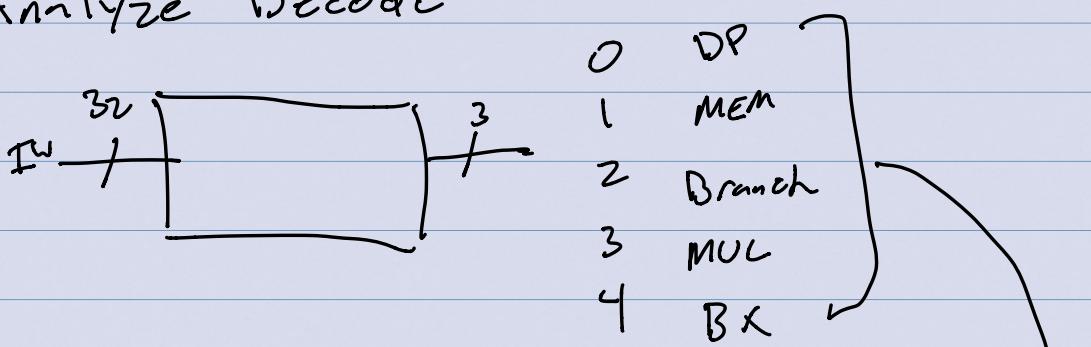
2bit decoder



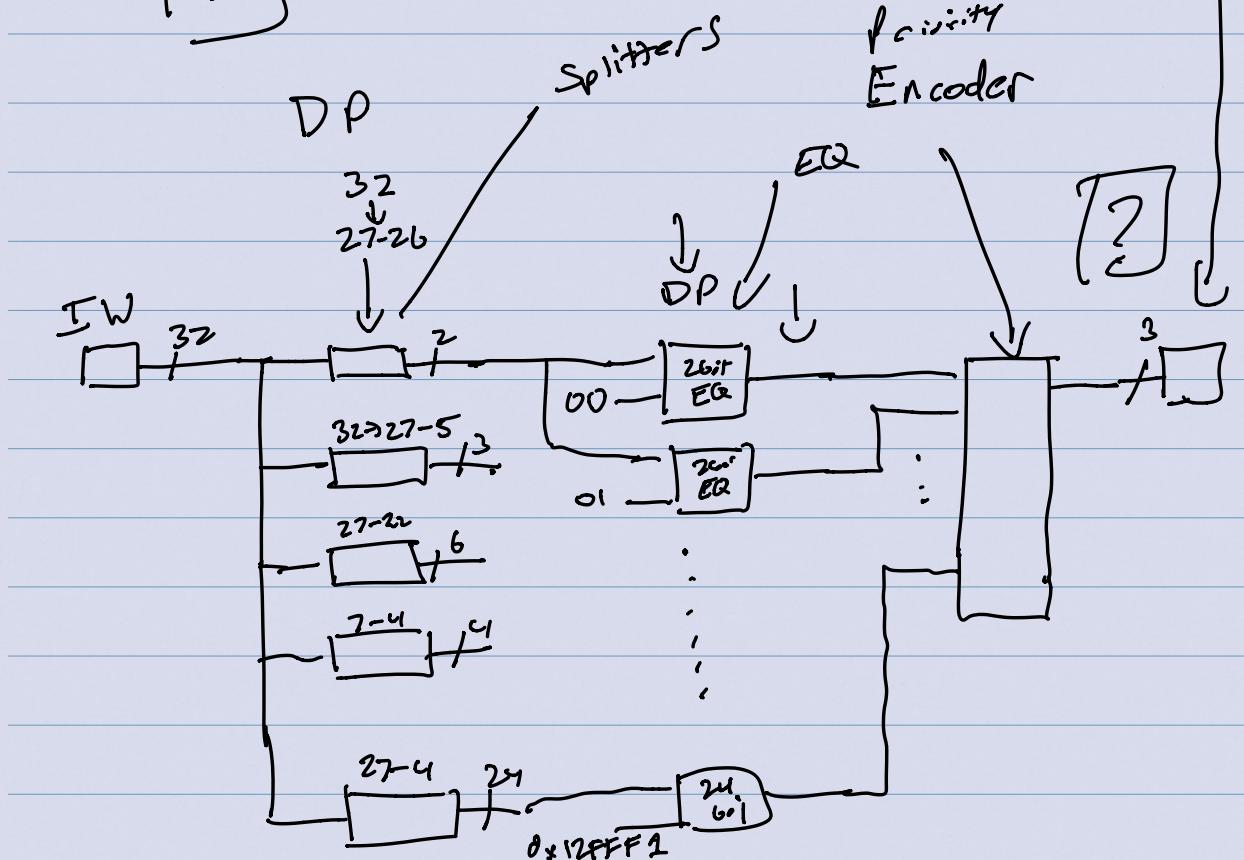
$s_1$	$s_0$	$r_0$	$r_1$	$r_2$	$r_3$
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



## Analyze Decode



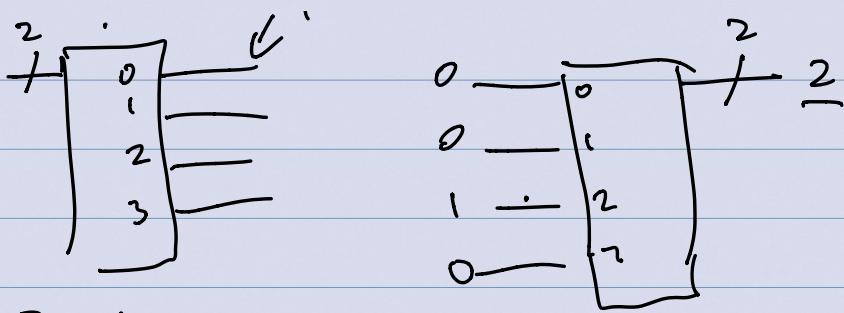
?



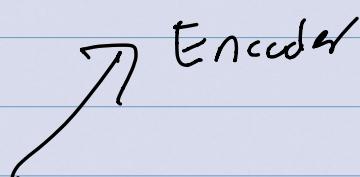
Priority  
Encoder

?

26-bit EQ    30-bit EQ    416-bit EQ    6-bit EQ  
24-bit EQ



Decoder



Encoder

Priority Encoder

