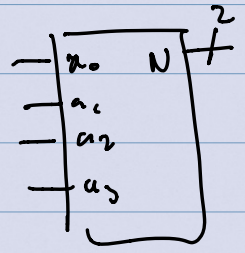
Project 05

Extra credit : Priority Encoder

Encoder



a_0	a_1	a_2	a_3	n_1	n_0
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

Priority Encoder

a_0	a_1	a_2	a_3	n_1	n_0
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
		⋮			

a_0	a_1	a_2	a_3	a_4	n_2 n_1 n_0
2^5 row					
			⋮		

Processor Components

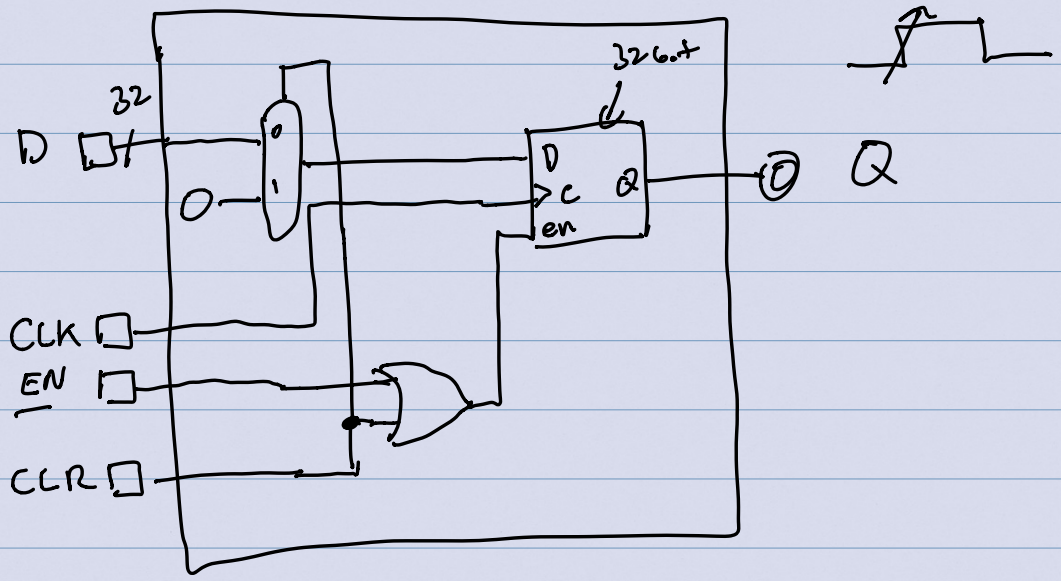
Digital Register with CLR

Register File

ALU

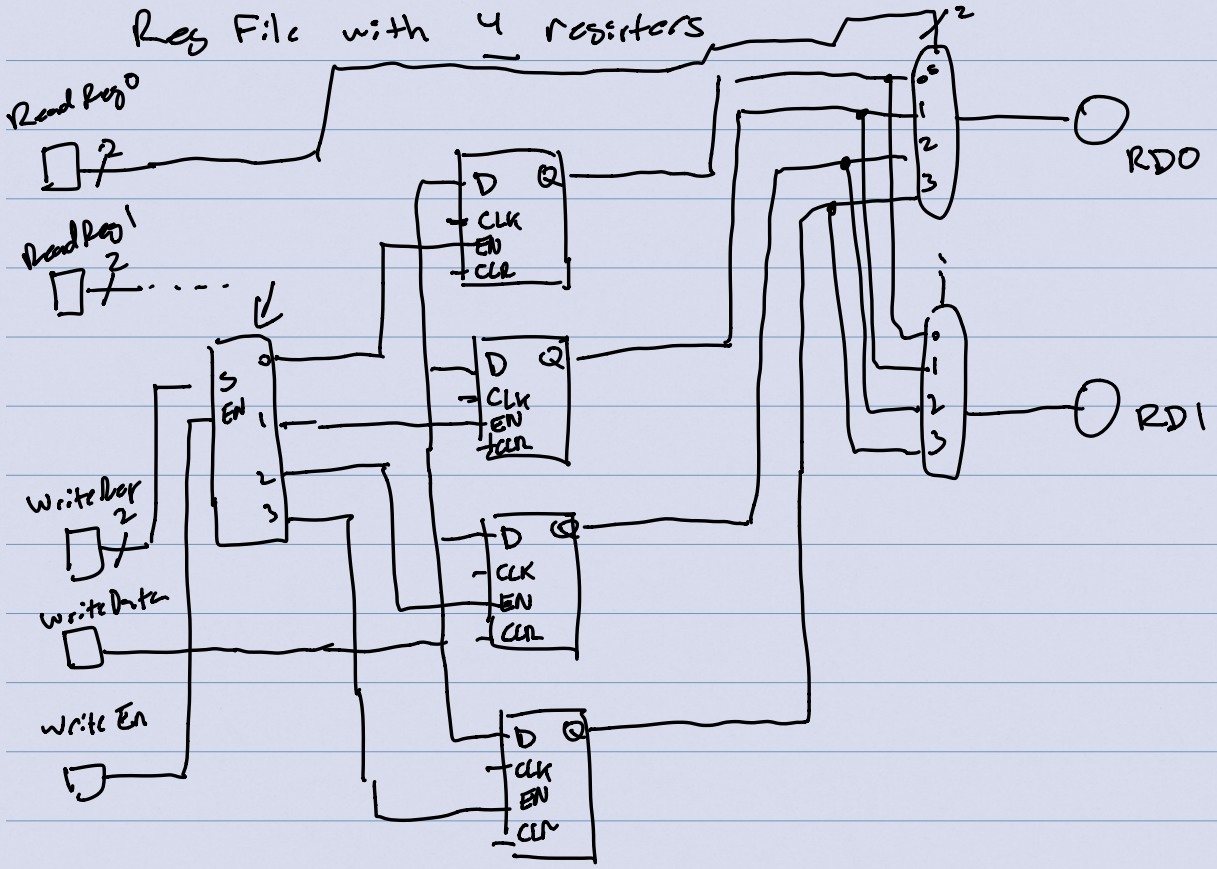
Register w/ CLR

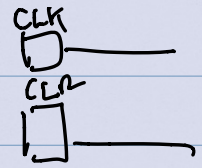
Synchronous clear



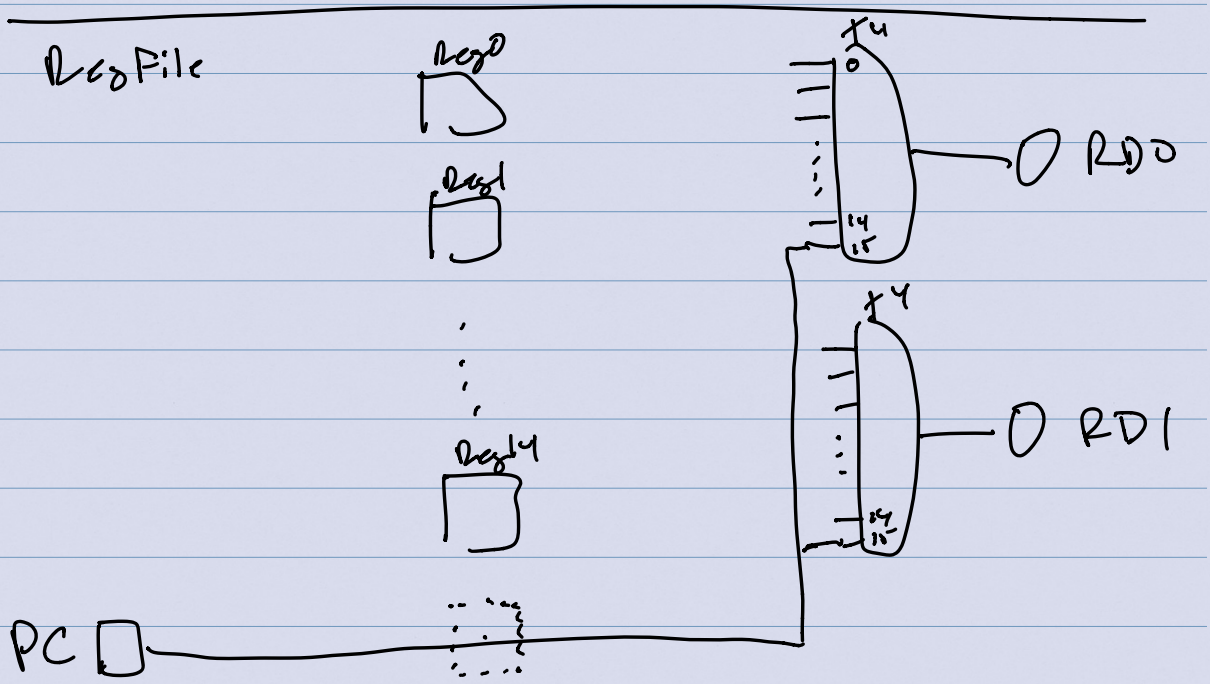
Register File

add r0, r1, r2
W R R

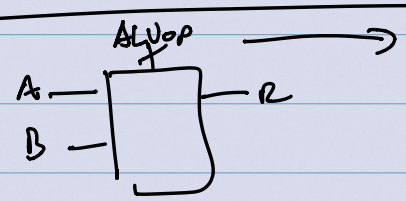




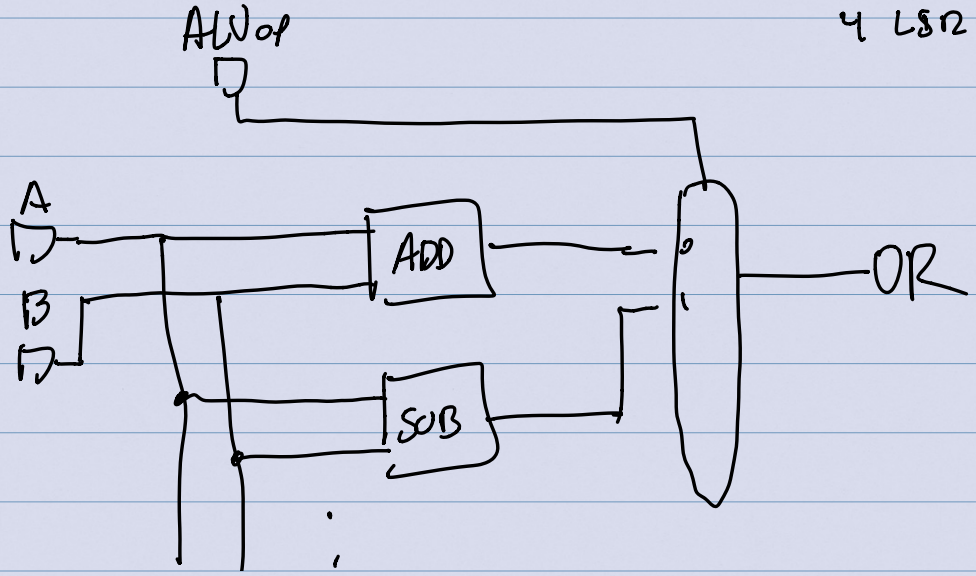
RegFile

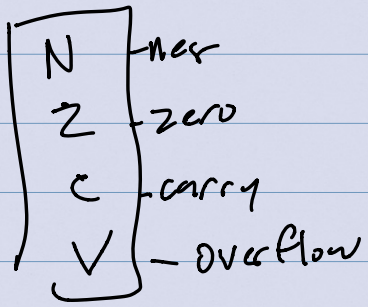


ALU

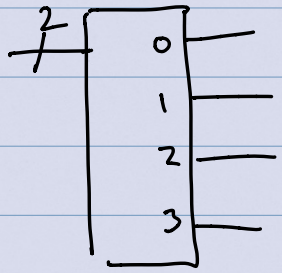
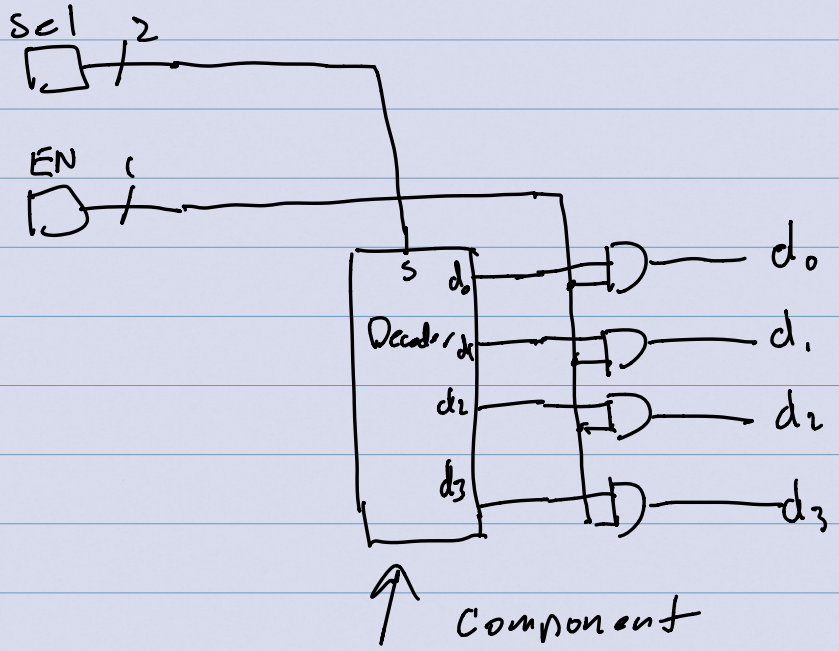


0 ADD
1 SUB
2 MUL
3 LSL
4 LSR





Decoder



Decoder with Enable