

## ProjectOS

### Review

wires, gates (and, or, not)

inputs and outputs

combinational logic

sum-of-products

Adder 1bit 4bit Ripple Carry Adder

Sequential Logic

clock, circuits that can hold values



SR latch  $\rightarrow$  D Latch  $\rightarrow$  D flipflop (1bit reg)

D Latch w/ CLR      D flipflop w/ CLR

n-bit Register

n-bit Counter (adder + register)

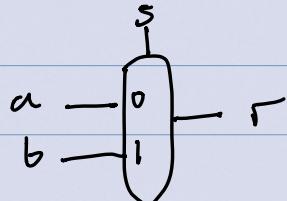
Digital's ROM component

Read Only Memory

c-analyze (ProjectOS implemented in C)

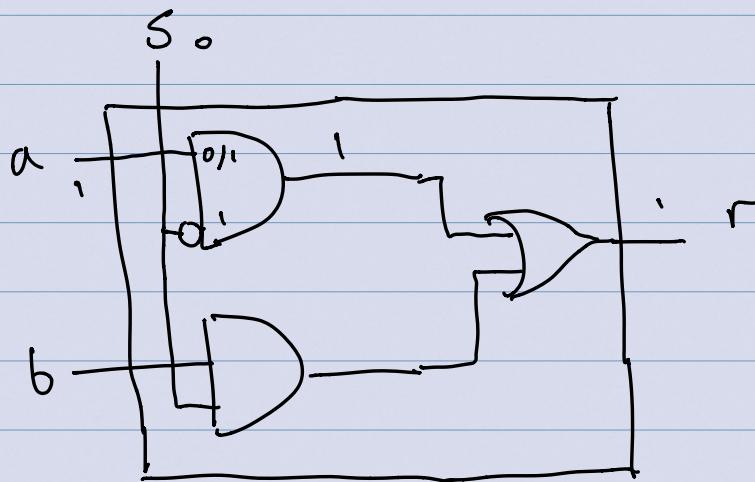
## Multiplexors (MUX)

1 bit 2 input MUX



a	b	s	r
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

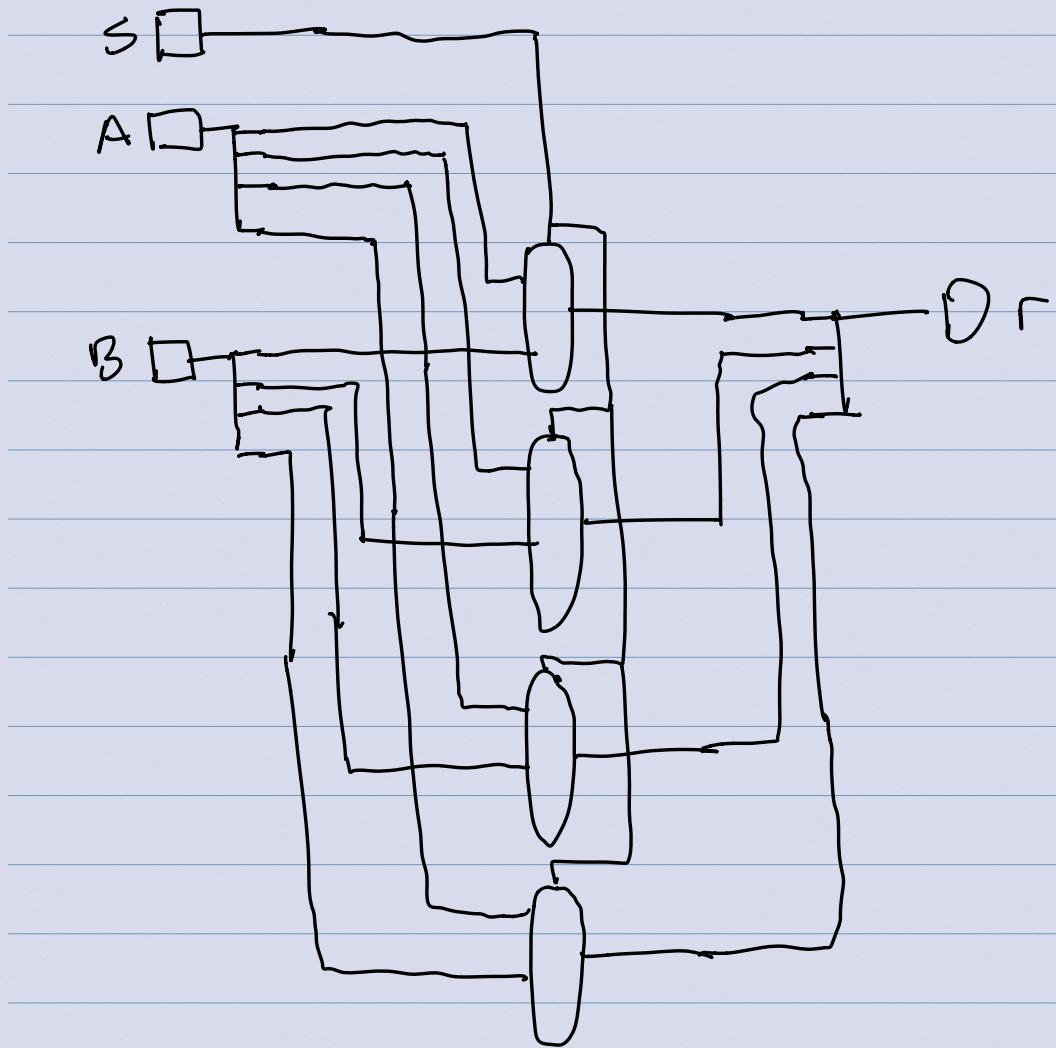
sum of products



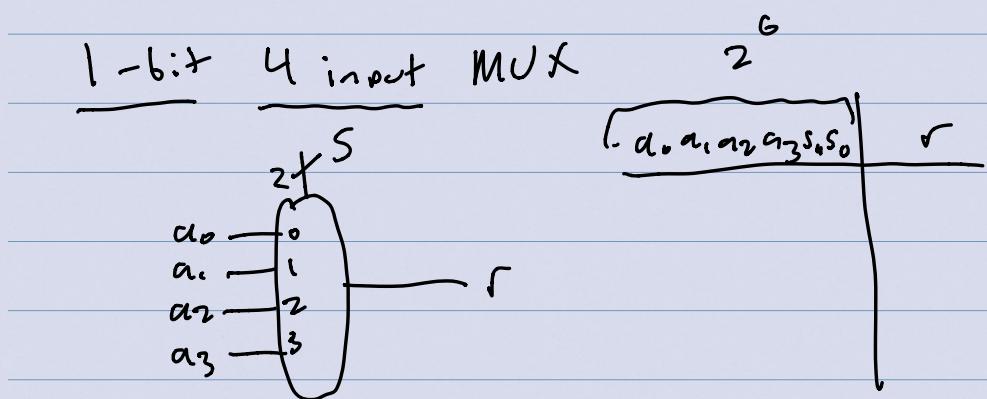
1 bit, 2 input MUX

↑      ↑

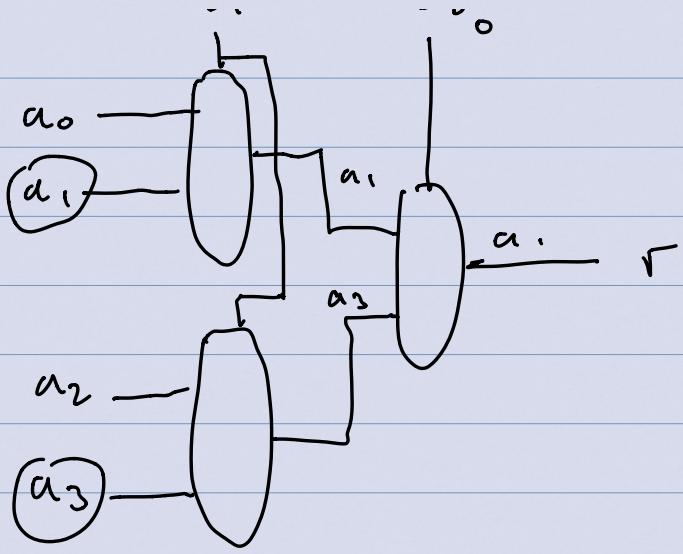
4 bit 2 input MUX



1-bit 4 input MUX



S<sub>1</sub>      S<sub>n</sub>



## Comparison - Equality

$$a \underset{EQ}{=} b \rightarrow EQ \quad \begin{cases} 1 & \text{if } a = b \\ 0 & \text{if } a \neq b \end{cases}$$

<u>a</u>	<u>b</u>	<u>EQ</u>	$\downarrow \downarrow$
0	0	1	$EQ = (\bar{a} \cdot \bar{b}) + (a \cdot b)$
0	1	0	
1	0	0	
1	1	1	$\nearrow$

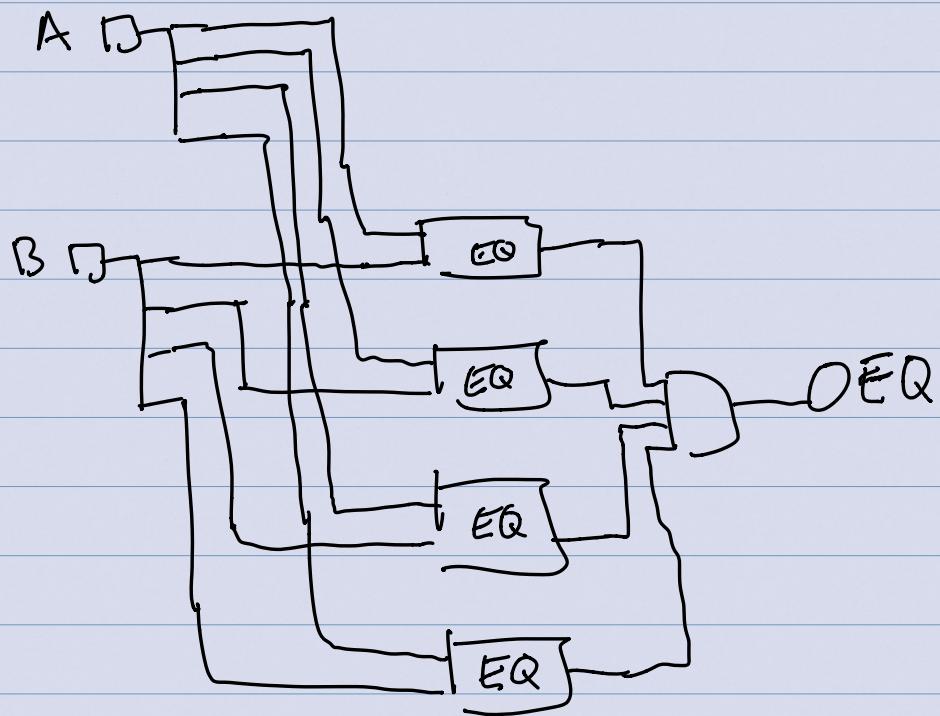
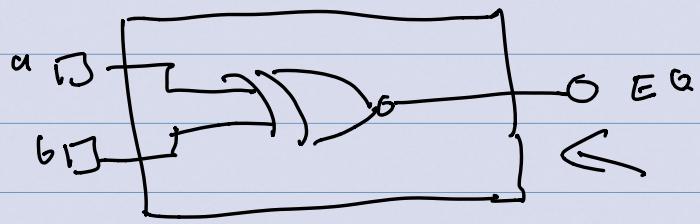
XOR      NOT

<u>a</u>	<u>b</u>	<u>XOR</u>
0	0	0
0	1	1
1	0	1
1	1	0

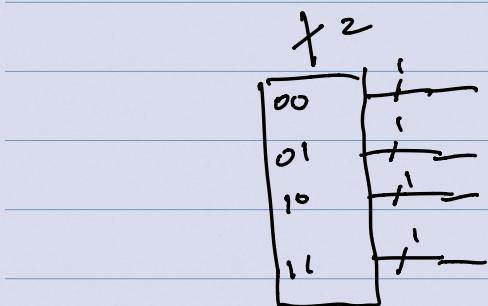
$\Rightarrow$   $\Rightarrow$

$\Rightarrow$

1 bit EQ comparator



Decoder



2 bit decoder

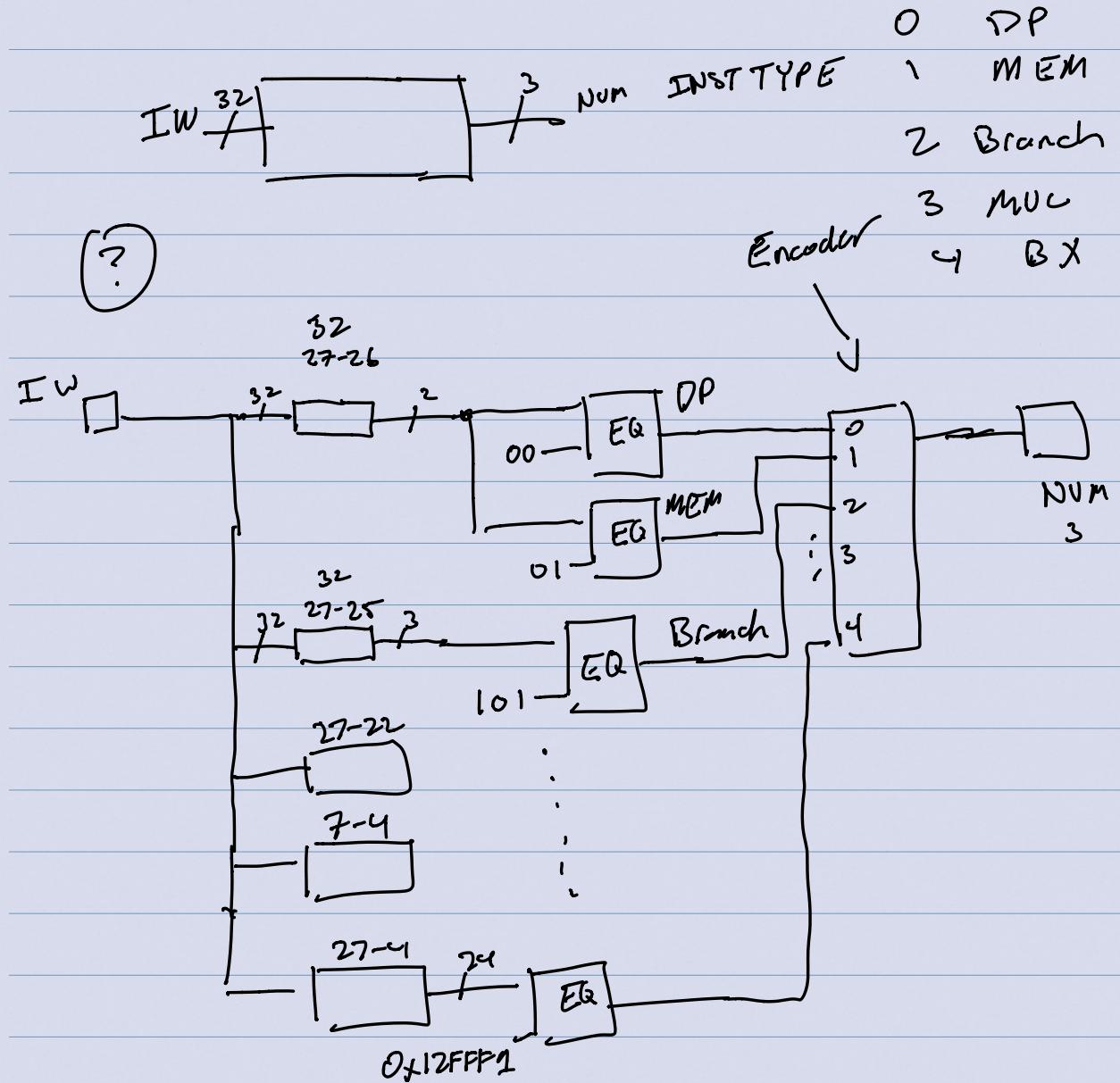
s <sub>1</sub> s <sub>0</sub>	r <sub>0</sub> r <sub>1</sub> r <sub>2</sub> r <sub>3</sub>
0 0	1 0 0 0
0 1	0 1 0 0
1 0	0 0 1 0
1 1	0 0 0 1

$$\begin{aligned} r_0 &= \\ r_1 &= \end{aligned}$$

$$r_2 =$$

$$r_3 =$$

## Analyze Decode



2 6-bit EQ 26-bit EQ 4-bit EQ  
 6-bit EQ  $\Rightarrow$  24-bit EQ 32-bit EQ

## Priority Encoder

