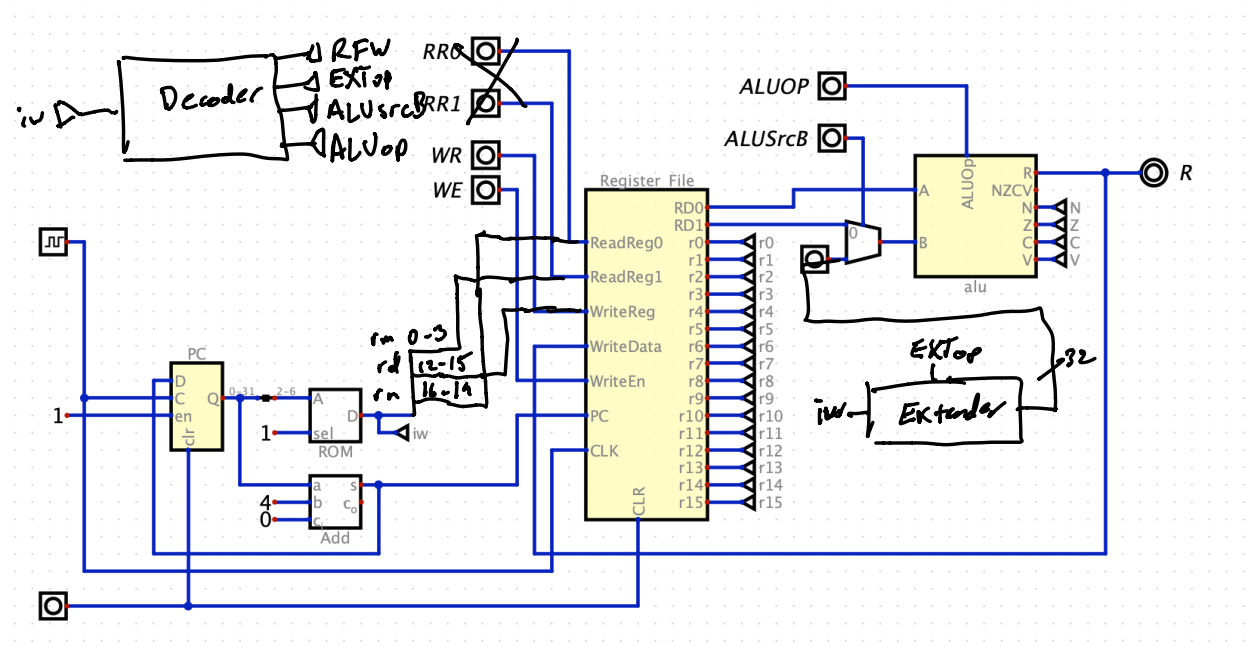
Lab10 due Friday night

Project 06 due wed Dec 2

Lab09



Lab10 part 1

add r2, r0, r1

Extend the data path

Add control

mov r0, #1

add r2, r0, r1 ←

Decoder

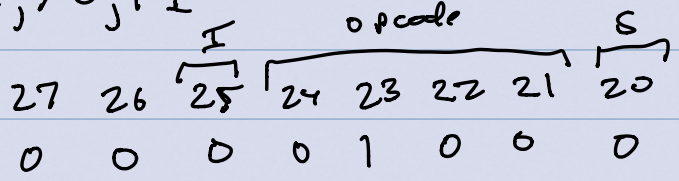
Like a hash table

Key → iw bits

Value → control output bits

RFW	EXTop	ALUsrcB	ALUop
(1)	(2)	(1)	(3)

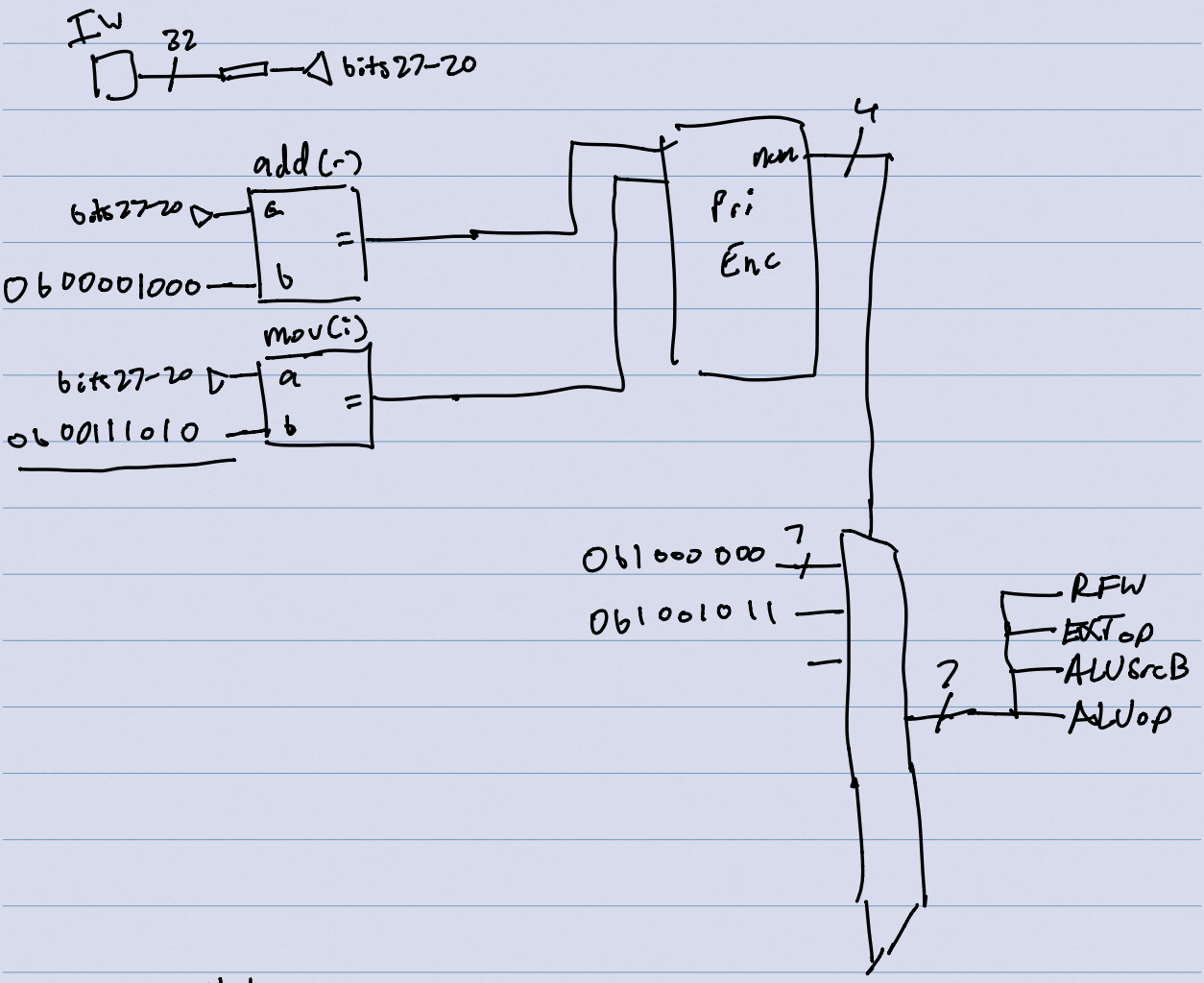
add r2, r0, r1



RFW	(WriteEn)	1	1000 000
EXTop	(Extender)	00	
ALUSrcB		0	
ALUop		000	

0000 1000 ⇒ 1000 000

Decoder Logic



mov r0, #1

		I	opcode				S
27	26	25	24	23	22	21	20
0	0	1	1	1	0	1	0

RFW	1	
EXTop	00	1001011
ALUSrcB	1	
ALUop	011	

Extender

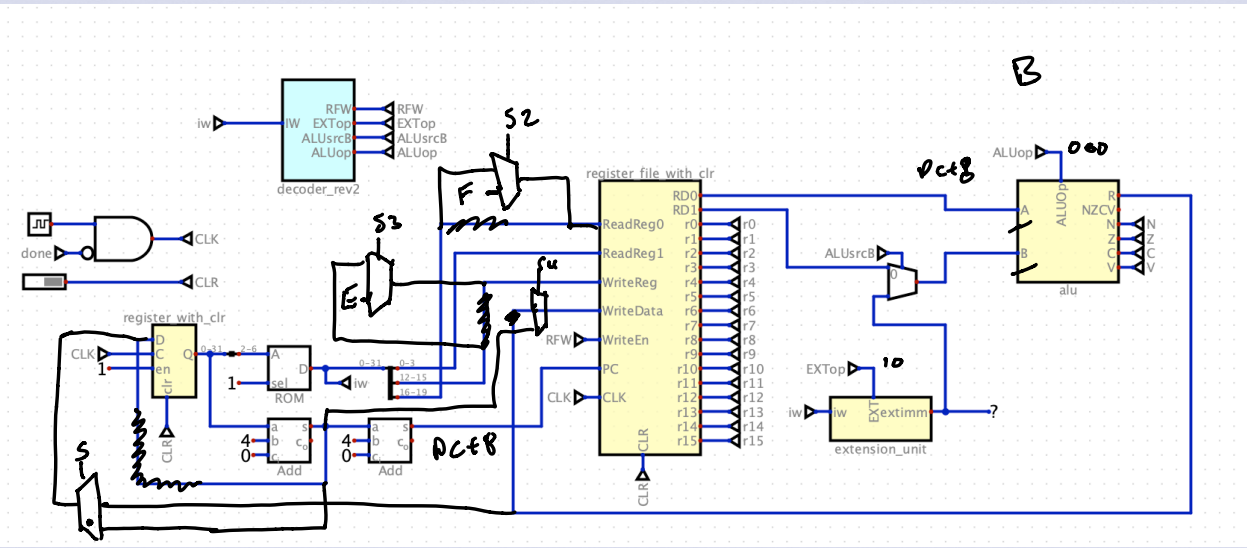
(00) DP immediate → 8 bit zero extend

(01) SDT (ldr/str) → 12 bit zero extend

(10) B/BL/BEQ → 24 bit sign extend with a multiply by 4

(11) Shift

Lab 10 part 2



bl

PC → bl foo

LR → ?

PC = foo:

bx lr

branch

Branch Target Address = (PC+8) + (offset x 4)

branch and link