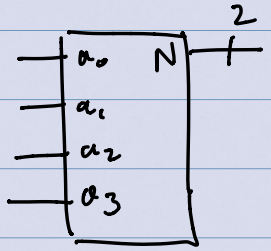
Project 05

Extra Credit: Priority Encoder

Encoder



a_0	a_1	a_2	a_3	n_1	n_0
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

a_0	a_1	a_2	a_3	n_1	n_0
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	1	0
0	0	1	1	1	1
				⋮	⋮

a_0	a_1	a_2	a_3	a_4	n_2 n_1 n_0

2^5 rows

$= 32$

MUX

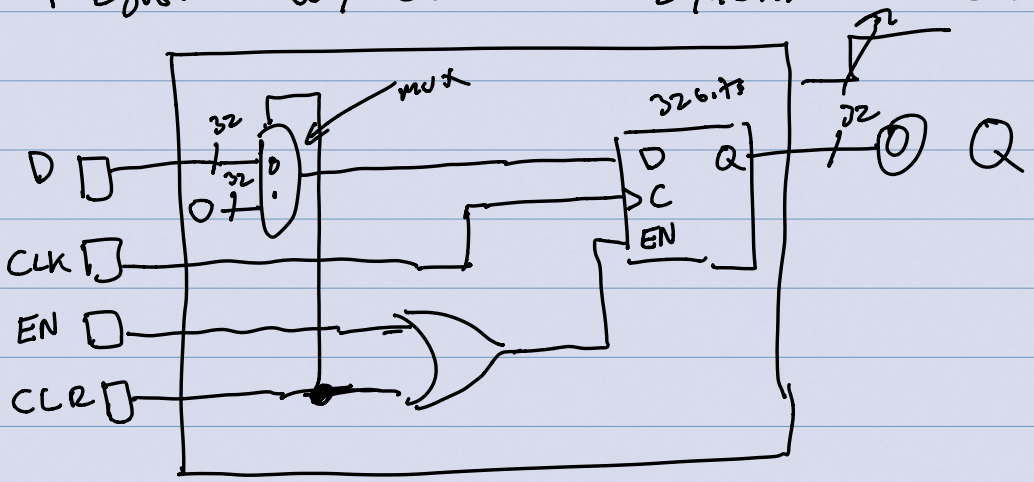
Processor Components

Digital Register with CLR

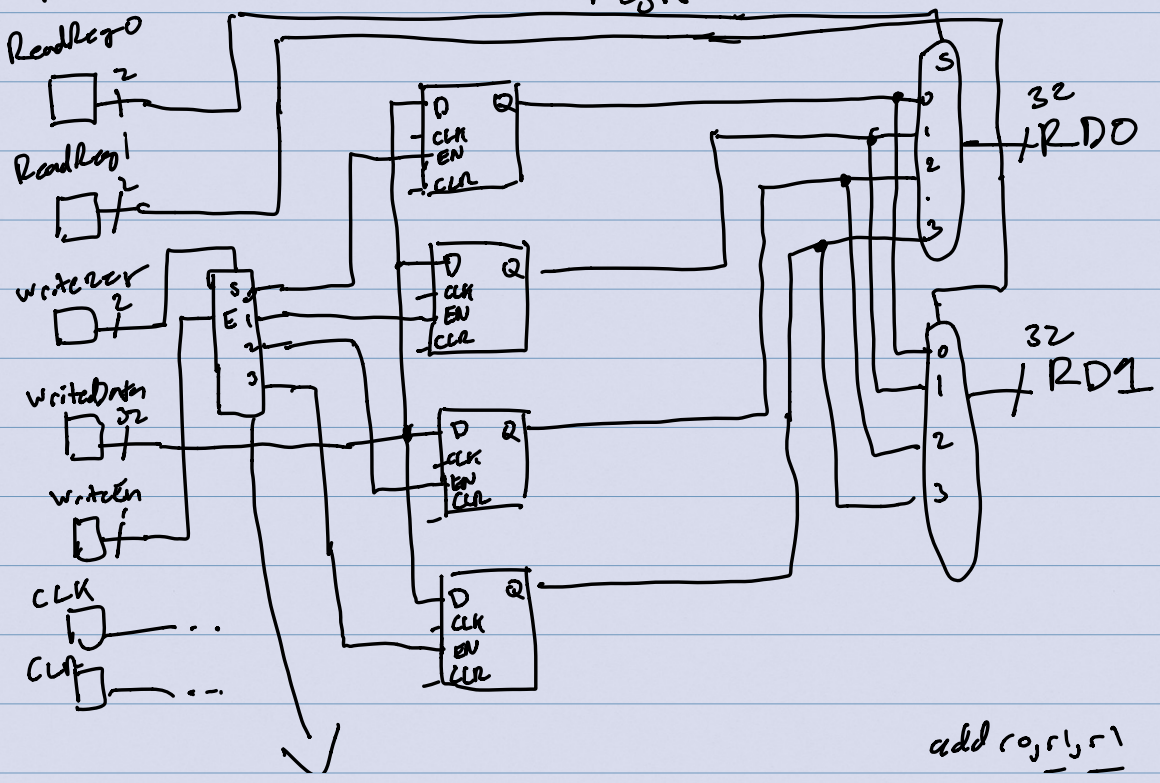
Register File → Decoder with Enable

ALU

32 bit Register w/ CLR — synchronous clear

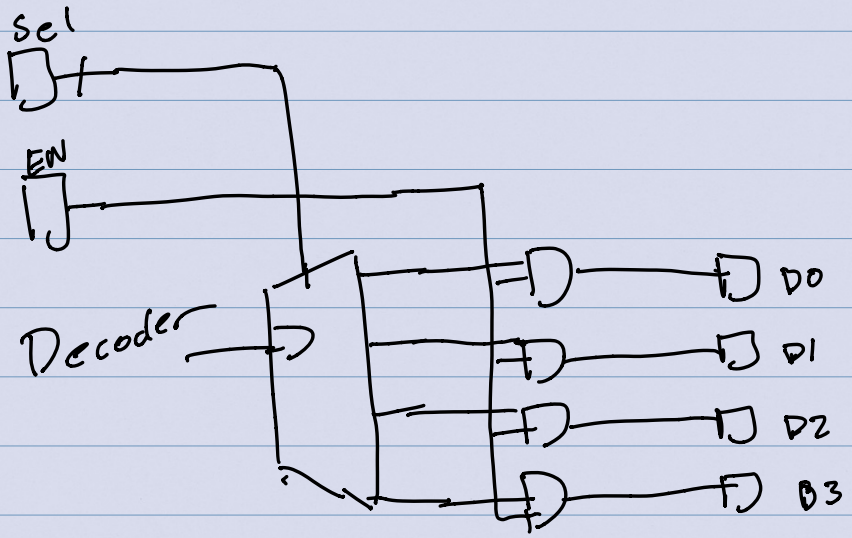


Register File with 4 registers

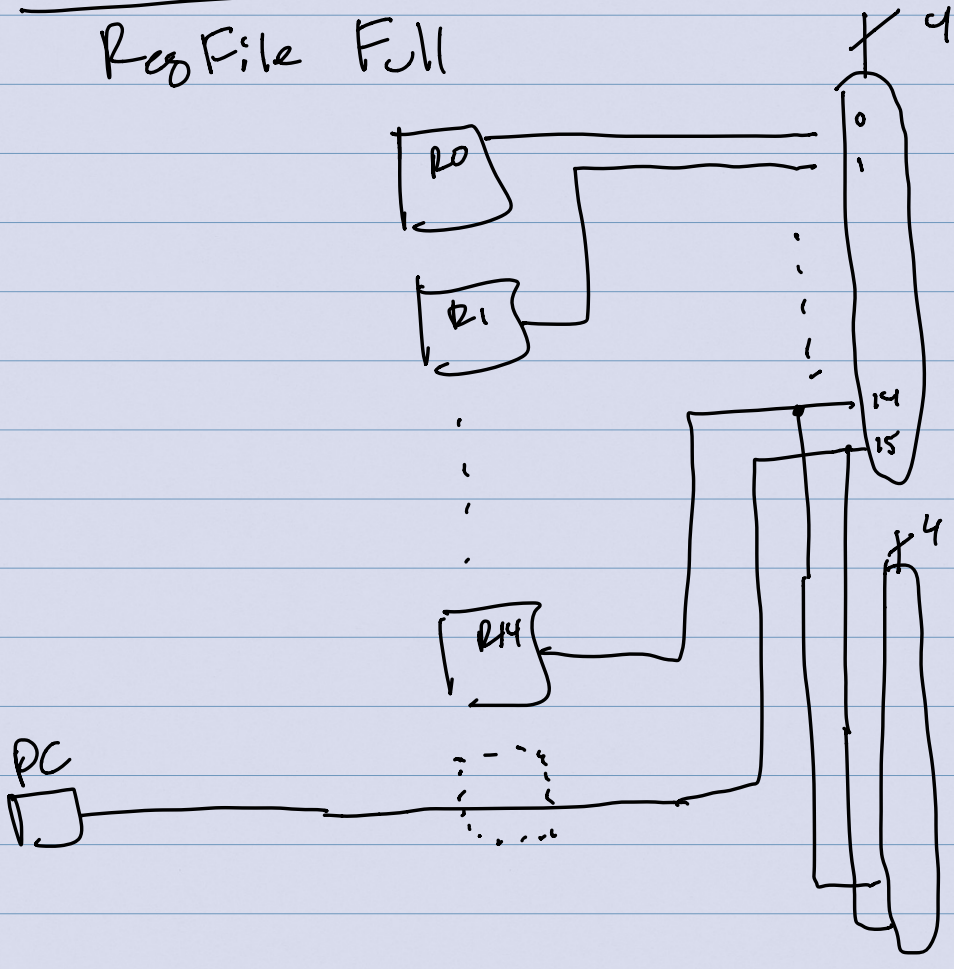


add rs,rt,rd

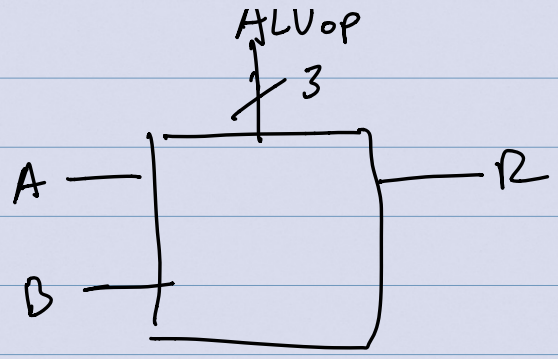
Decoder with Enable



RegFile Full

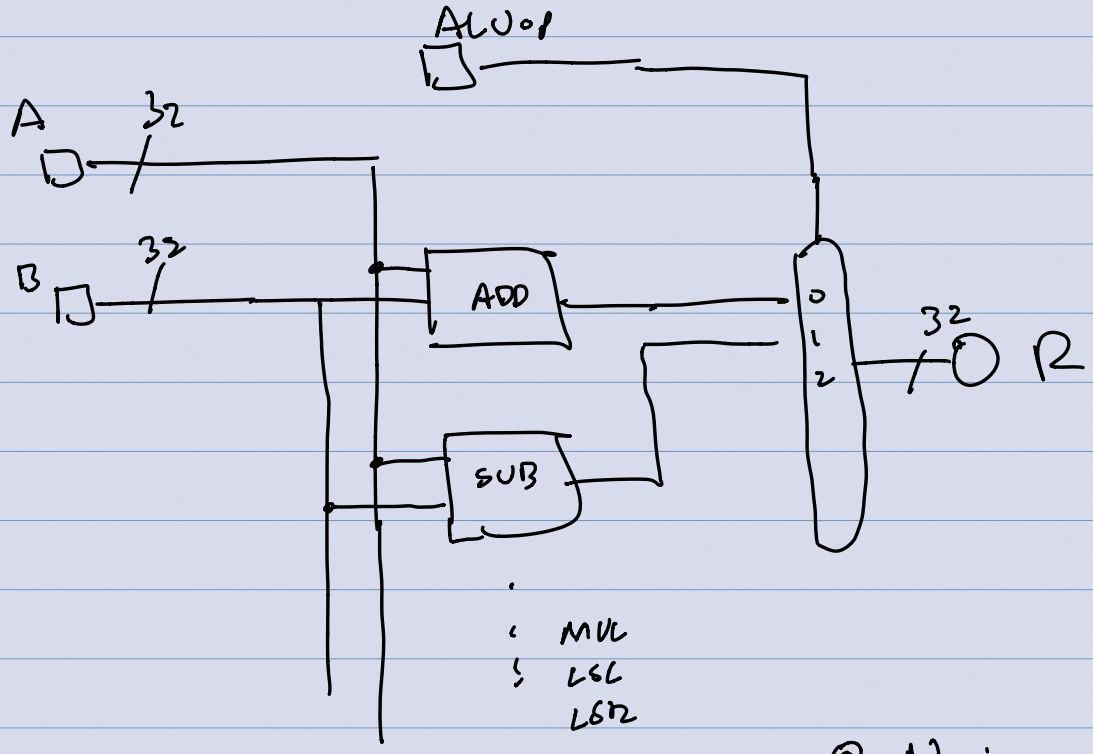


ALU



0	ADD
1	SUB
2	MUL
3	LSL
4	LSR

5



- N neg
- Z zero
- C carry
- V overflow