

Project 04 - finish makeup points

Project 05 - overview

Lab 08 - Part 3

4-bit adder - Ripple carry adder, splitters

Sequential Logic - state

1-bit register - latches and flip-flops

Lab 08 Part 3

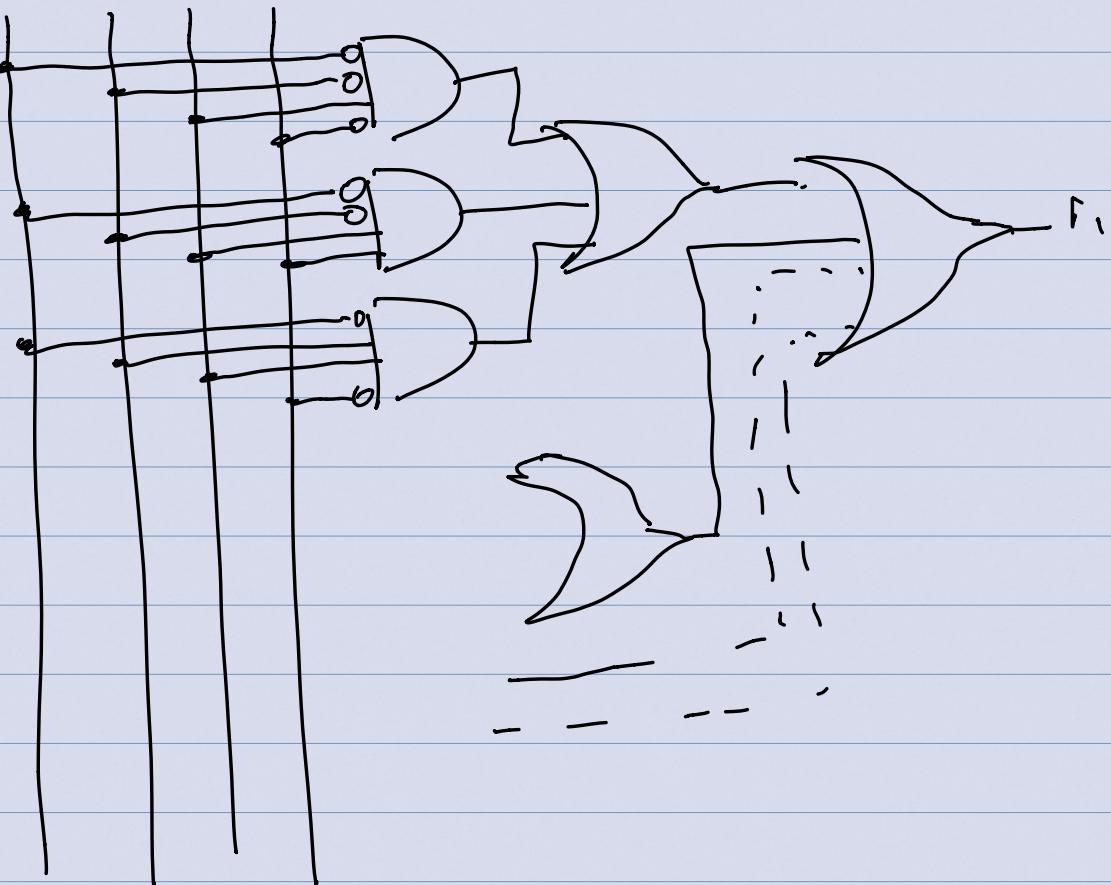
$a \ b \ r \quad r = \max(a, b) \text{ 2 bit values}$

a_1	a_0	b_1	b_0
0	0	0	0
0	0	0	1
x	0	1	0
x	0	1	1
0	1	0	0
0	1	0	1
x	0	1	0
x	0	1	1
x	1	0	0
x	1	0	1
x	1	1	0
x	1	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

$r_1 \ r_0$

$$\begin{aligned} r_1 &= (\bar{a}_1 \cdot \bar{a}_0 \cdot b_1 \cdot \bar{b}_0) + (\bar{a}_1 \cdot \bar{a}_0 \cdot b_1 \cdot b_0) + (\bar{a}_1 \cdot a_0 \cdot b_1 \cdot \bar{b}_0) \\ &\quad + (\bar{a}_1 \cdot a_0 \cdot b_1 \cdot b_0) + (a_1 \cdot \bar{a}_0 \cdot \bar{b}_1 \cdot \bar{b}_0) + (a_1 \cdot \bar{a}_0 \cdot \bar{b}_1 \cdot b_0) \\ &\quad + (a_1 \cdot \bar{a}_0 \cdot b_1 \cdot \bar{b}_0) + (a_1 \cdot \bar{a}_0 \cdot b_1 \cdot b_0) + (a_1 \cdot a_0 \cdot \bar{b}_1 \cdot \bar{b}_0) \\ &\quad + (a_1 \cdot a_0 \cdot \bar{b}_1 \cdot b_0) + (a_1 \cdot a_0 \cdot b_1 \cdot \bar{b}_0) + (a_1 \cdot a_0 \cdot b_1 \cdot b_0) \end{aligned}$$

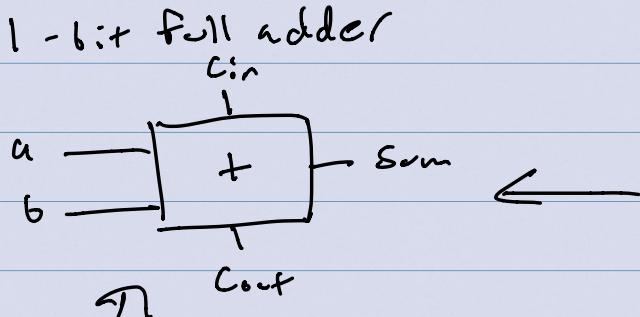
a_1, a_0, b_1, b_0



Can override $S_{input max}$ for gates.

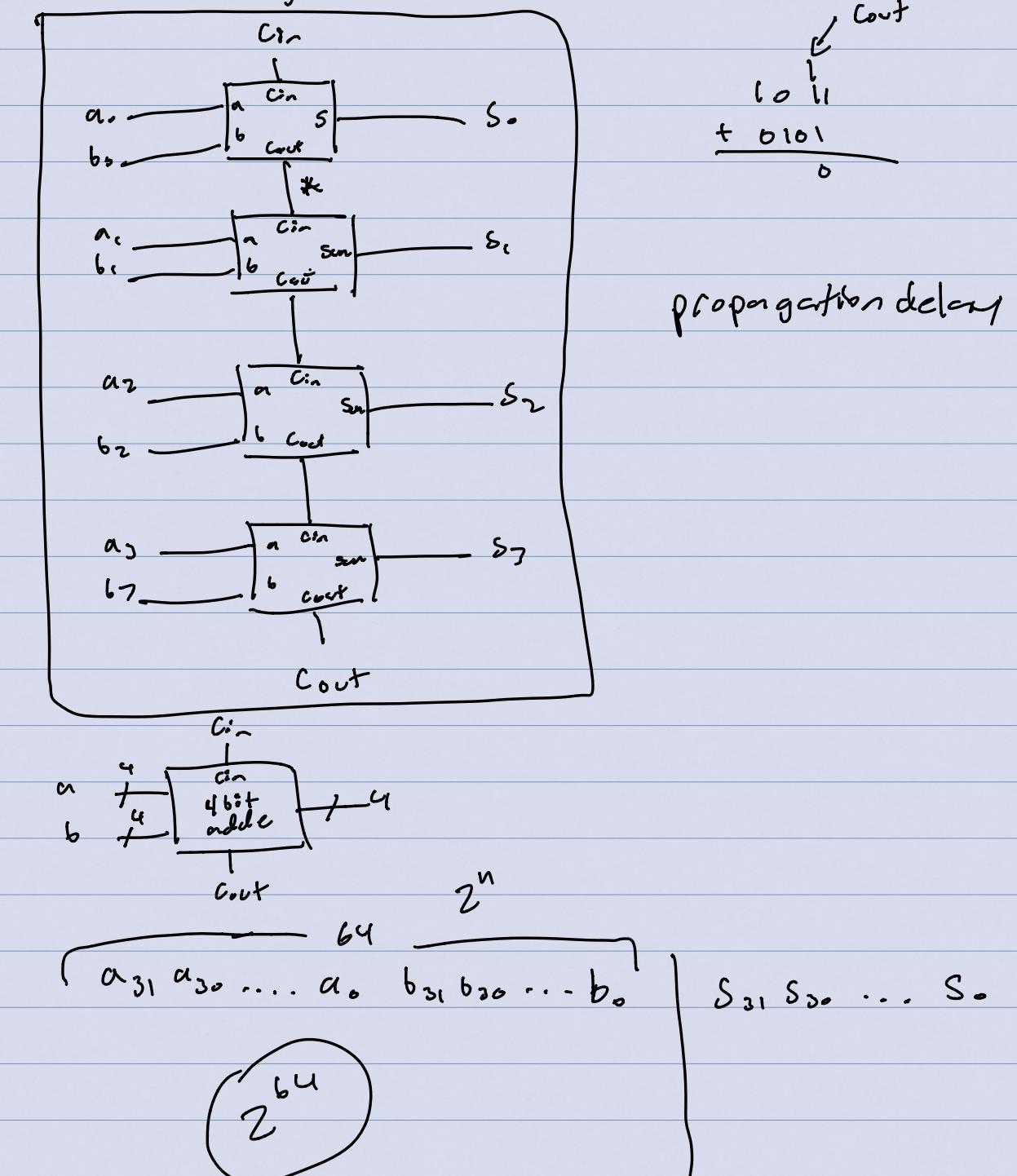
Adder

1-bit full adder



Ripple carry adder

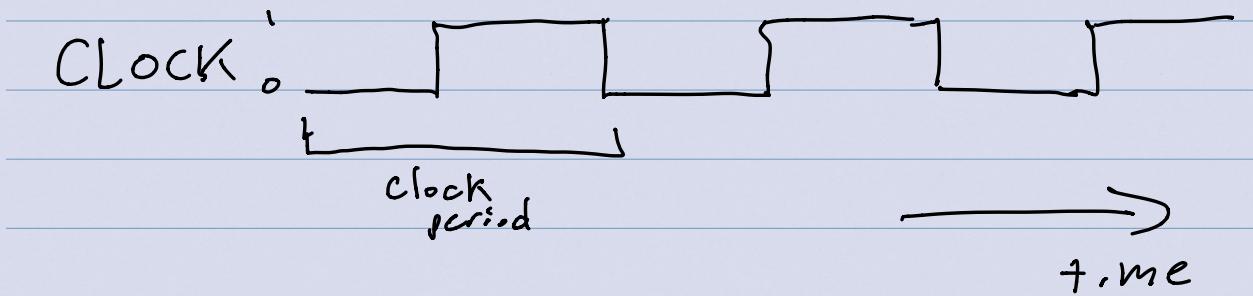
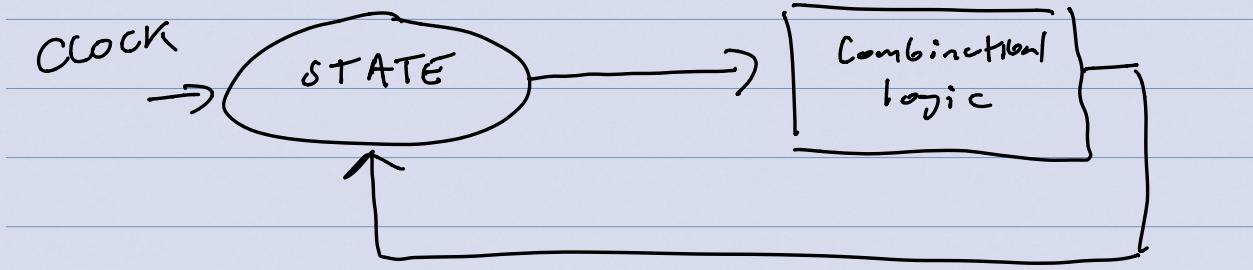
Splitter \rightarrow multi-bit inputs/outputs



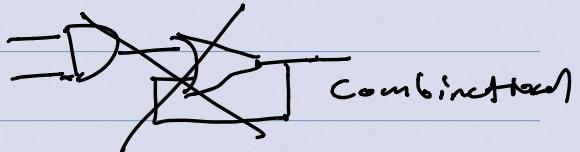
Carry Lookahead adder

Sequential Logic

processor



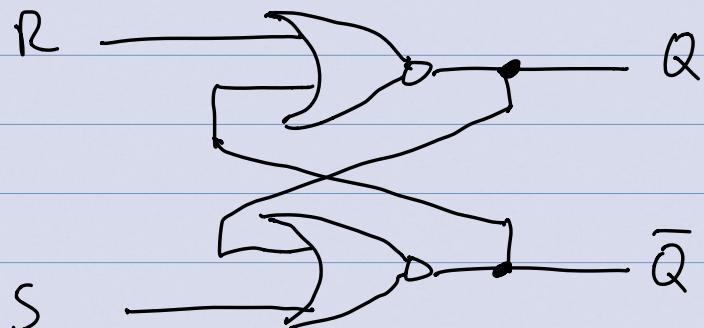
STATE?



How to store 1-bit of information

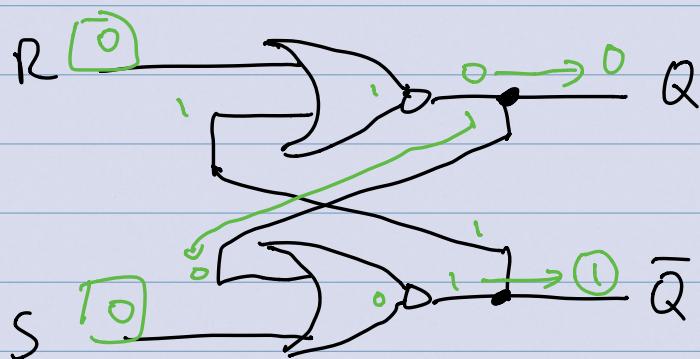
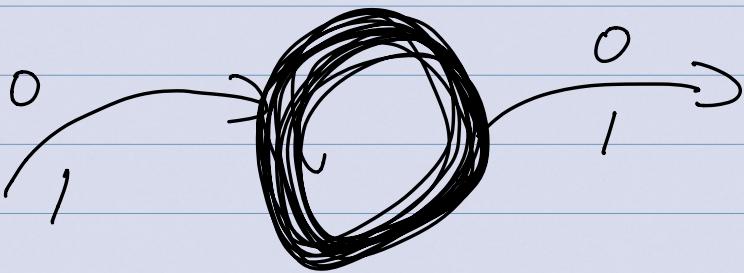
SR Latch Set/Reset

NOR



If $R=1$ (high) \Rightarrow set latch to 0

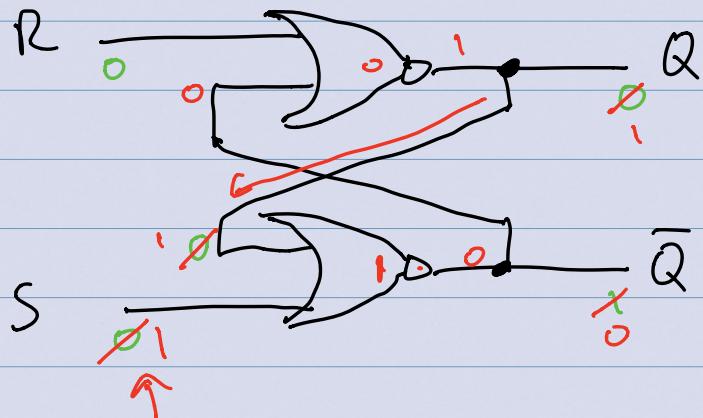
If $S=1$ (high) \Rightarrow set latch to 1

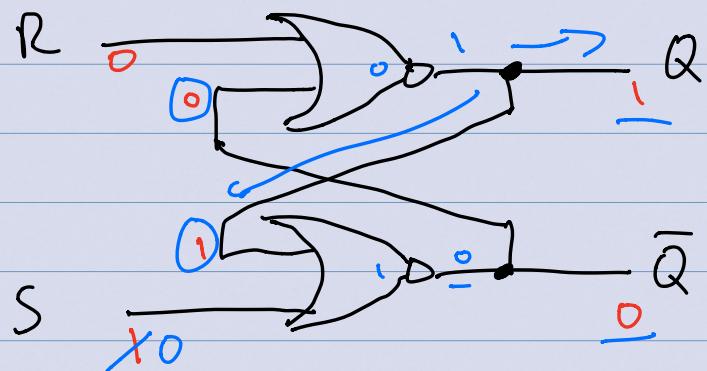


$$\begin{array}{r}
 R \quad S \quad Q \quad \bar{Q} \\
 \hline
 0 \quad 0 \quad 0 \quad 1 \\
 0 \quad 1 \quad 1 \quad 0 \quad \leftarrow \\
 \hline
 0 \quad 0 \quad 1 \quad 0 \quad \leftarrow * \\
 1 \quad 0 \quad 0 \quad 1 \\
 \hline
 \end{array}$$

ILLEGAL

$$\boxed{\begin{array}{l} R = 1 \\ S = 1 \end{array}}$$





STATIC RAM

Registers

Cache Memory



DYNAMIC RAM

Capacitor