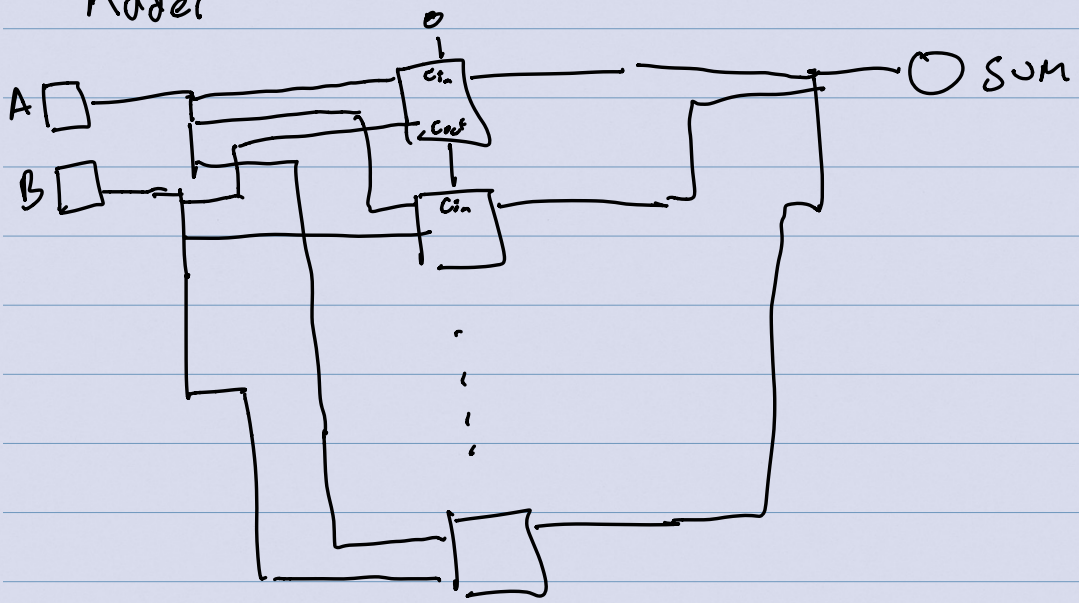
Project05

Repo : .dig , .hex

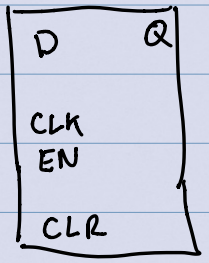
analyze_main.dig

Adder

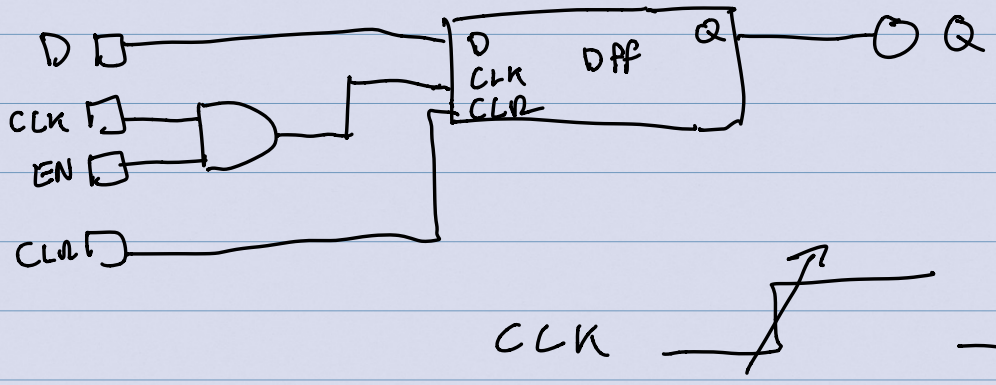


Register with Enable

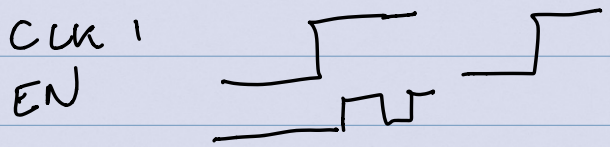
8bit Register

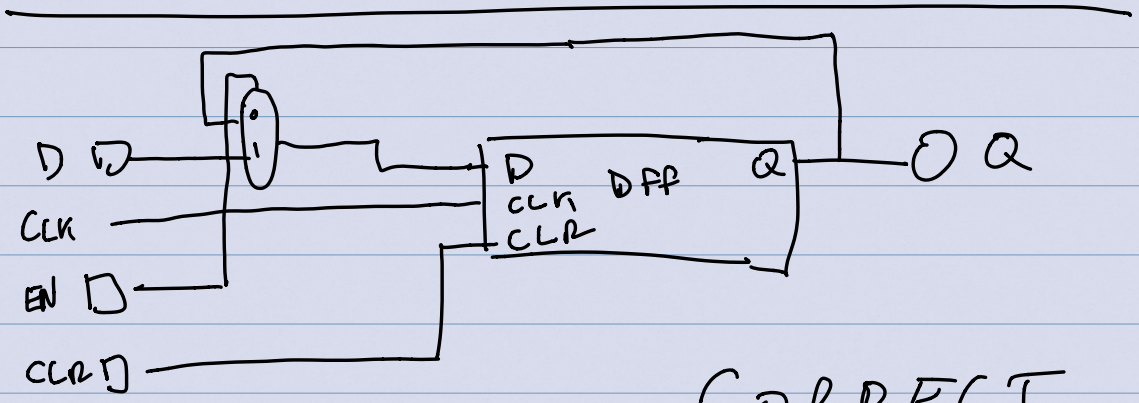


1 bit D flipflop (Dff)



WRONG





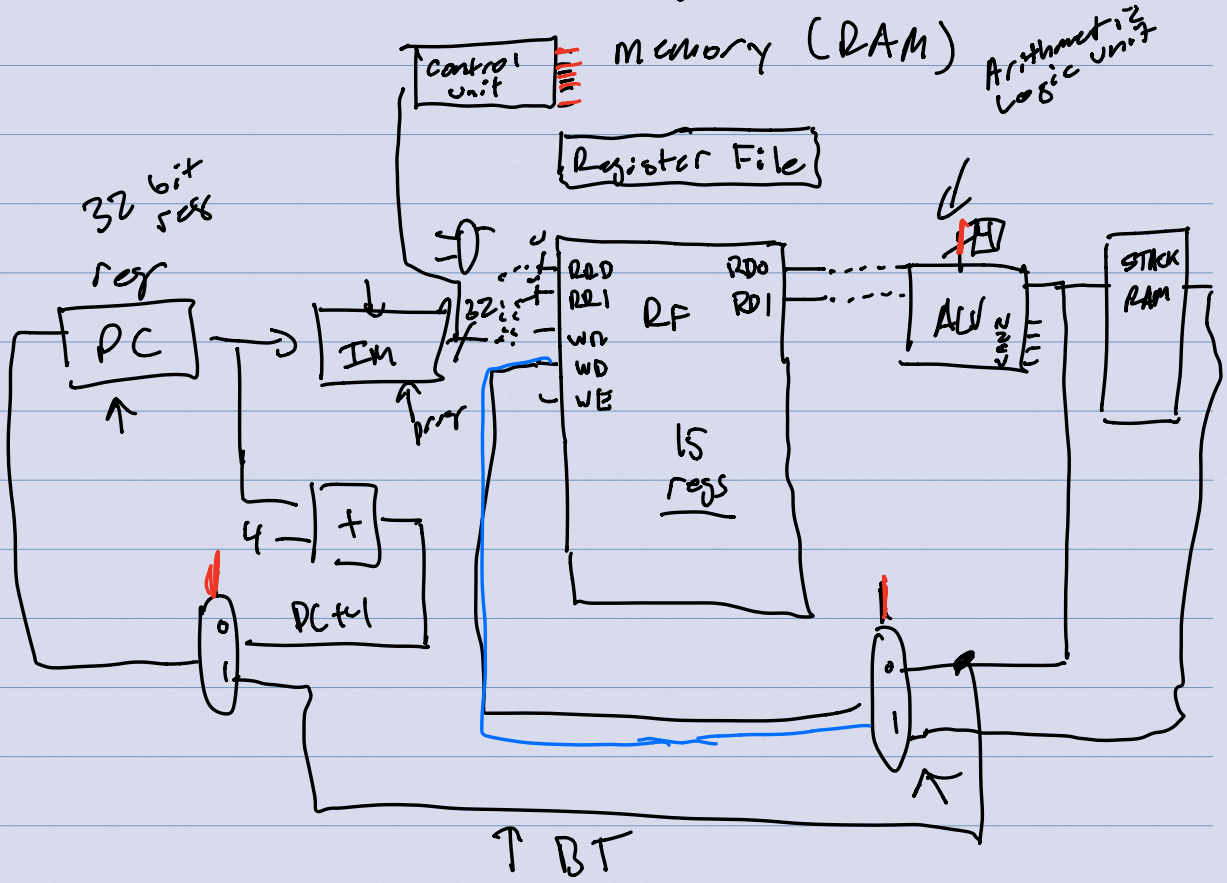
CORRECT

Project 06

ARM Processor Implementation

Processor state: registers

memory (RAM)



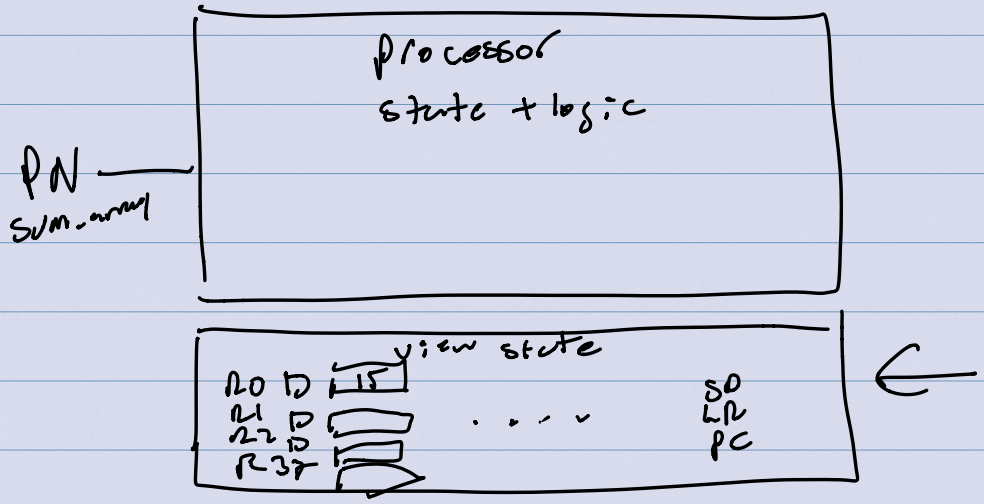

```
add r0, r1, r2
mov r1, #4
ldr r3, [r4]
```

Data Path

Control Path

High Level

processor_main circuit



Programs

main:

```
mov r0, #2
mov r1, #2
mov r2, #3
mov r3, #4
bl  quadratic_S
add r0, r0, #0   <- End Marker
```

quadratic_S:

```
mul r12, r0, r0
mul r1, r12, r1
mul r2, r0, r2
add r0, r1, r2
add r0, r0, r3
bx lr
```

Unchanged