# Question 1 - Sum-of-Products

Consider implementing the Majority function of 3 1-bit inputs, `r = majority(a, b, c)`. The the value of the Majority function is true if and only if the majority (at least two) inputs are true. For example:

```
majority(1, 0, 1) = 1
majority(0, 1, 0) = 0
```
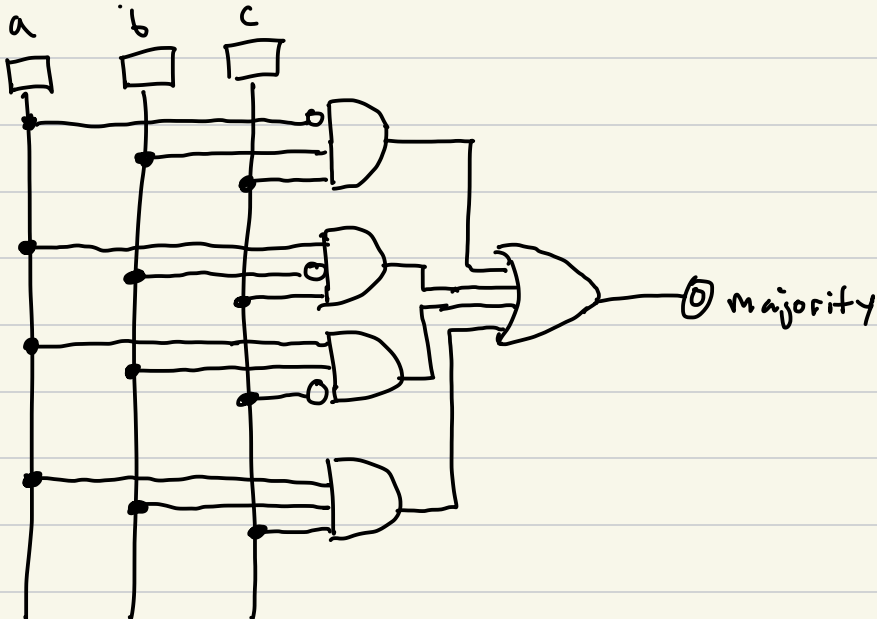
Build a truth table for this function. Next, derive the sum-of-products boolean algebra equation for this function. Finally, draw a circuit that implements this function in terms of AND, OR, and NOT gates.

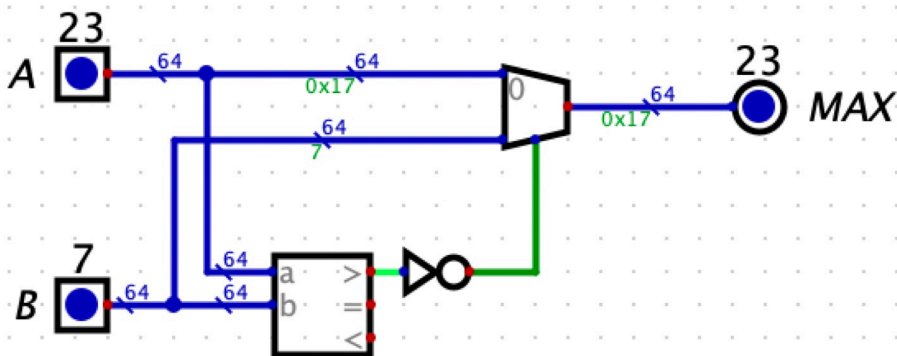| a | b | c | Majority |
|---|---|---|----------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

$$Majority(a, b, c) =$$
$$(\bar{a} \cdot b \cdot c) + (a \cdot \bar{b} \cdot c) + (a \cdot b \cdot \bar{c}) + (a \cdot b \cdot c)$$

# Question 2 - Digital Design

Consider the following circuit called Max2, that determines the maximum of two 64-bit inputs. That is, the circuit take inputs A and B and the output is A if A > B, otherwise the output is B.



Build a new circuit called Max3 that determines the maximum value of 3 inputs: A, B, and C. You can use the library circuits use above (the comparator and multiplexor) and any additional gates you may need. Give a brief explanation in English how your new circuit works. Draw neatly. Note, you cannot implement Max3 in terms of Max2, you must use components and gates.
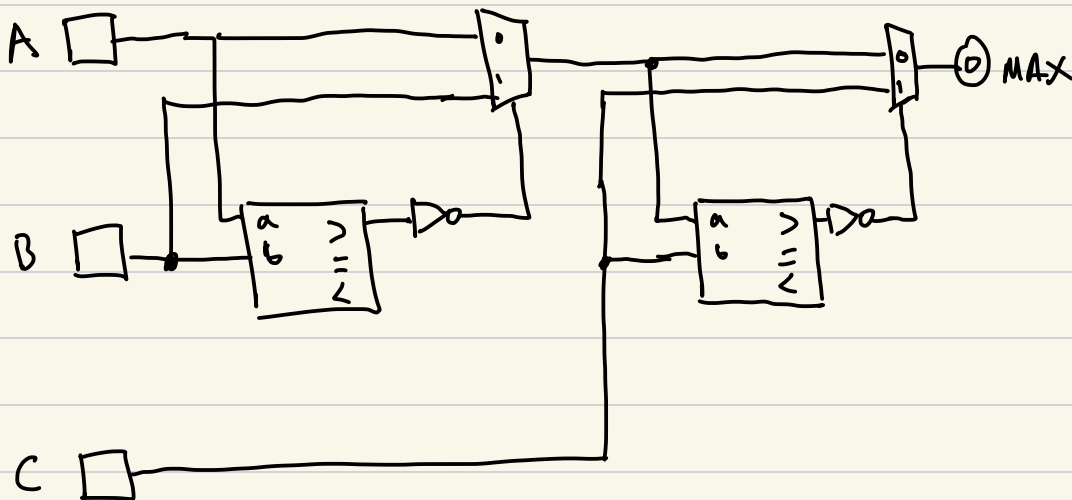
# Question 3 - Single Cycle Processor

Consider the following version of the RISC-V single-cycle processor you developed for Project06. For this problem you are going to answer some questions about the implementation then explain how to add some new instructions.
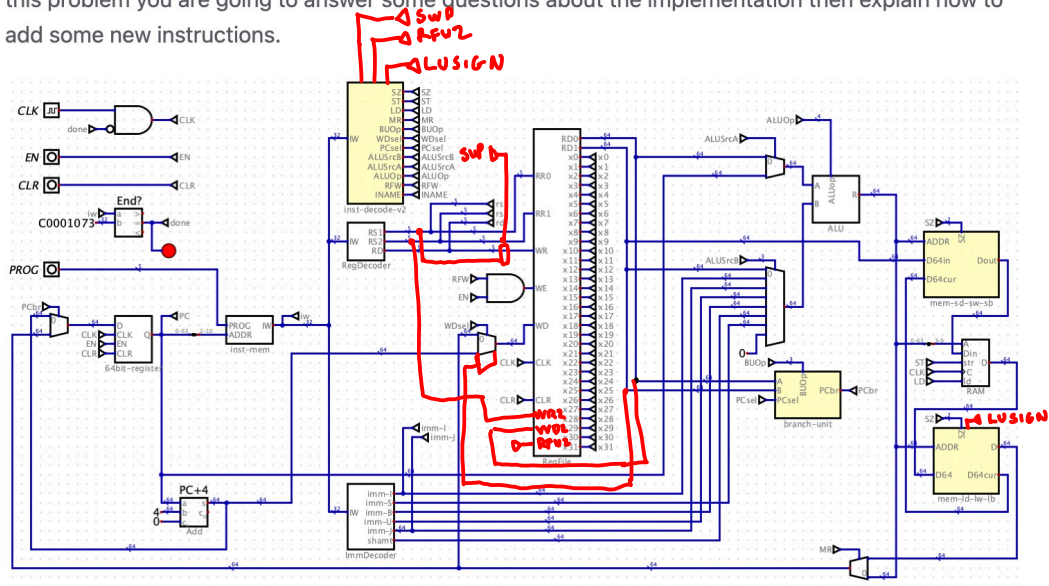


Answer the following questions below. Justify your answers. Answers without justification will receive 0.

- (1) What is the maximum number of instructions a single program can have in this processor?
- (2) How many registers can be updated in a single clock cycle?
- (3) Which instruction uses the second input to the ALUSrcA MUX?
- (4) What is the purpose of the SZ input to `mem-sd-sw-sb` and `mem-ld-lw-lb`?

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① 512 instructions. The address splitter is 2-10, which is 9 bits. $2^9 = 512$.

② Only one register can be updated in a single clock cycle because the register file only has one WD input, one WR input, and one RFW input. Note that the PC can be updated separately from the one register that can be updated in the register file.

③ JAL and the conditional branches (BEQ, BNE, BLT, BGE) all use the second input to the ALUSrcA MUX, which is the current PC. This is used to calculate the target address.

④ SZ is used to determine if we are loading or storing a double (0), a word (1) or a byte (2).

Now you are going to explain how to add new instructions to this processor. For each instruction, describe any additions or changes needed to the data path, the control path, and components. Also, explain changes needed in the instruction decoder. Completeness and details in your answer are important. You should assume that each of these instructions are currently not supported by this processor.

- (5) LWU (load word unsigned) This instruction loads a word (32 bits) from memory and puts the value into a 64 bit register. However, the word is not sign extended, like with LW (load word).
  Example usage: `lwu t0, (a0)`

- (6) SWPR (swap registers). This new instruction swaps two register values. Without this instruction, to swap register values, say `a0` and `a1` you need to do the following:

```
mv t0, a0
mv a0, a1
mv a1, t0
```

With SWPR, you can just do `swpr a0, a1`

⑤ For LWU we need a new control line to send to the load component (mem-ld-lu-lb) to select between signed loads and unsigned loads. Call it LUSIGN. This needs to be added to the decoder spreadsheet and the instruction decoder, and as an input to the load component. It will control a MUX that picks between sign extend (0) and zero extend (1). See LUSIGN above.

⑥ For SWPR, we need to modify the register file so that two registers can be updated on a single clock cycle. This means the register File needs 3 new inputs: WD2, WR2, RFW2. The register file will need to be modified to allow two registers to updated at the same time with these new control lines. They need to be added to the decoder spreadsheet and instruction decoder.

Now, for SWPR, we need to read rs1 on RD0 and rs2 on RD1. The new SWP control line selects writing to rs1 instead of rd. Whereas we connect RD0 to WD2, and RD1 to the WDsel MUX, which will need to be expanded. See the modifications to the two level circuit above.

# Question 4 - Pipelined Processor

Consider the project07 starter pipelined processor below.
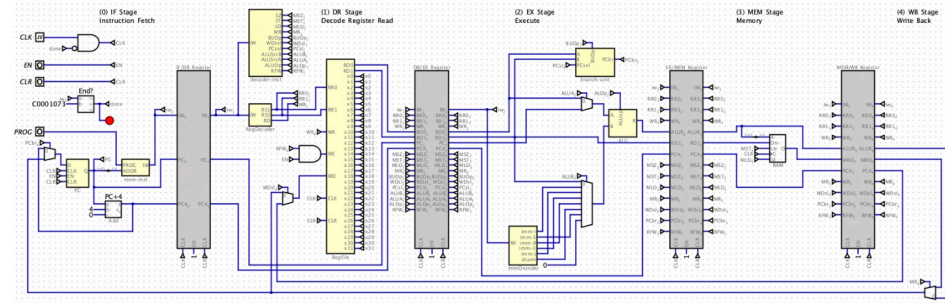


Answer the following questions and provide justification for answers. Answers without justification will receive 0.

Consider running the following code on the starter pipeline processor.

```
addi a1, zero, 3
addi a2, zero, 4
add a0, a1, a2
unimp
```

- (1) Explain why the code above produces the wrong result on the starter pipeline processor.

- (2) What result does this give? That is, what value will be in `a0` after executing this code?

- (3) Without modifying the processor implementation, how could you modify this code to make it run correctly?

① When the add instruction reaches the EX stage
RD0 and RD1 will not have the correct values because
the two addi instructions will not have completed
their WB stages.

② On our processor, a0 will be 0 because all register
values are initialized to 0 at startup.

③ We can add nops:
```
addi a1, zero, 3
addi a2, zero, 4
nop
nop
nop
add a0, a1, a2
unimp
```
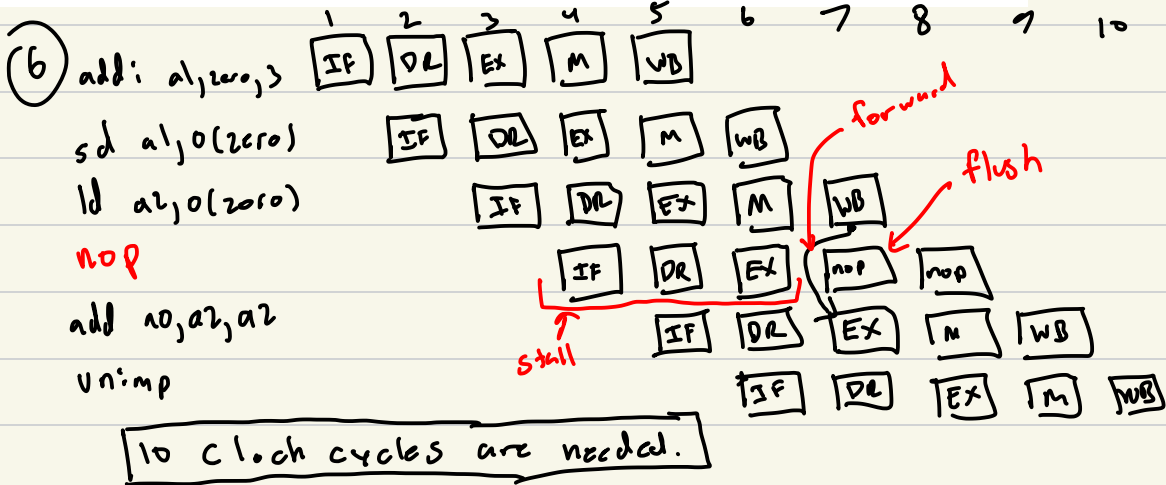
Now consider running this code on a complete solution to project07. That is a version of this pipeline with a proper hazard unit that supports forwarding, stalling and flushing.

- (4) How many clock cycles will it take to complete the code given above?

- (5) When the code executes, are any flushes or stalls needed?

Now consider the following code on a complete solution to project07:

```
addi a1, zero, 3
sd a1, 0(zero)
ld a2, 0(zero)
add a0, a2, a2
unimp
```

- (6) How many clock cycles are needed to execute this program?

- (7) Is flushing needed when executing this code? If so, explain when it is needed.

- (8) Is stalling needed when executing this code? If so, explain when it is needed?

- (9) Is forwarding needed when excuting this code? If so, explain when it is needed.



(6) addi a1,zero,3   IF De EX M WB

sd a1, 0(zero)   IF De EX M WB

ld a2, 0(zero)   IF De EX M WB

nop

add a0,a2,a2

unimp

forward

flush

stall

10 clock cycles are needed.

(7) Yes, on clock cycle 6, when we need to insert a nop.

(8) Yes, on clock cycle 6, we need to stall the add

(9) Yes, in clock cycle 7, we forward from WB to RD0 and RD1 in EX.