Lab 05 Q & A

immediates

Sign extension

jal

immediates

    goal : create a signed 64 bit
             value from the immediate bits

steps
    ① extract immediate sequences
    ② combine sequences into one immediate
        in the proper order
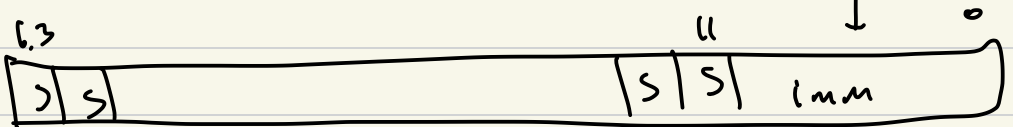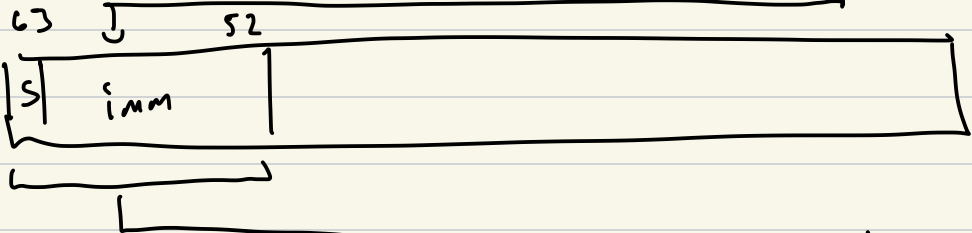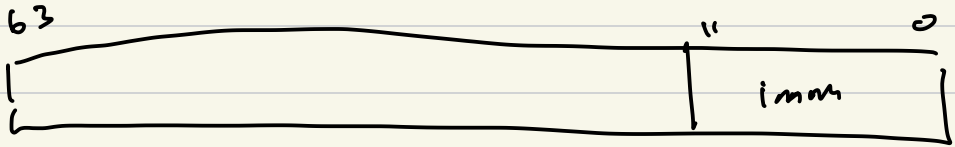   ③ sign extend to 64 bits

i-type   vint32_t iw;

31   (20)
| imm[11:0] | rs1 | funct3 | rd | opcode |

31   12 11   0
| 0   . . . 0 0 |s| imm[11:0] |

int64_t imm64;
vint32_t imm11_0;
imm11_0 = get_bits (iw, 20, 12);

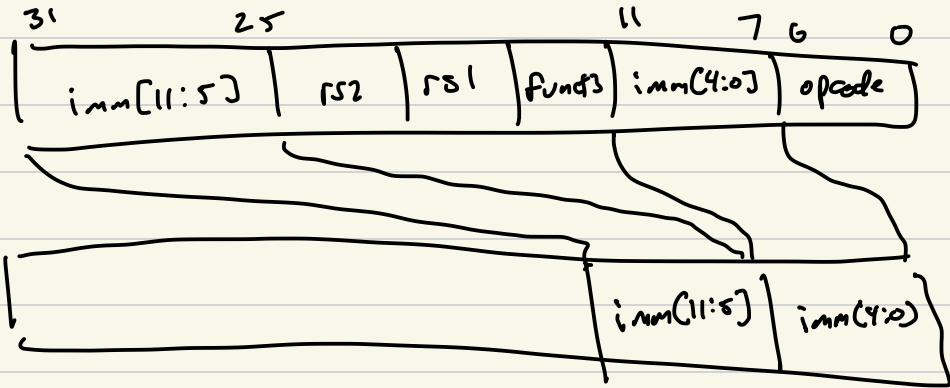imm64 = sign_extend (imm11_0, 11);

63   11   0
| | imm |

63   J   52
|s| imm |

6.3   11   0
| > |s| |s|s| imm |

S type

Sw t0, 32 (t1)
lw t0, 32 (t1)

```
 31          25                11      7 6     0
|                  |         |    |       |          |       |
|  imm[11:5]       |   rs2   | rs1| funct3| imm[4:0] | opcode |

                                        | imm[11:5] | imm(4:0) |
```


uint32_t imm11_5;
uint32_t imm4_0;

imm11_5 = get_bits(iw, 25, 7);
imm4_0 = get_bits(iw, 7, 5);

int64_t imm64

imm64 = (imm11_5 << 5) | imm4_0

imm64 = sign_extend (imm64, 11);

B-type   no   zero   bit

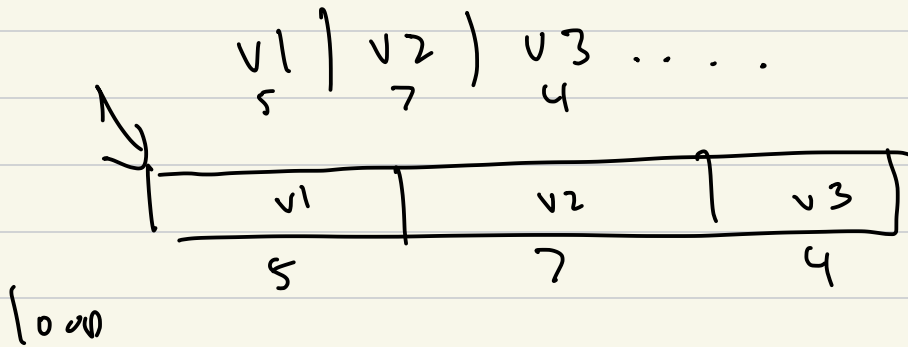imm 4-1

imm 64 = ⌣_____⌣ | (imm 4-1) << 1)

imm 64 = ⌣_____⌣ | (imm 10-5 << 5) | (imm 4-1 << 1)

Vint32_t combine (v1, len1, v2, len2, ...)

$$v1 \mid v2) v3 . . . .$$
$$\quad 5 \quad\quad 7 \quad\quad 4$$

v1	v2	v3
5	7	4

loop

v = v1
v = v1 << len1

Project03 — Full RISC-V Emulator

① Additional instructions

② Dynamic Analysis

    instruction count
    branch count
    branch not taken

③ Cache Simulator

Memory PRAM

STACK

Processor
lw

DATA

CODE

processor speed

↑
gap
↓

Memory speed

time

Memory

Processor — addr → CACHE → Memory

?
hit   miss
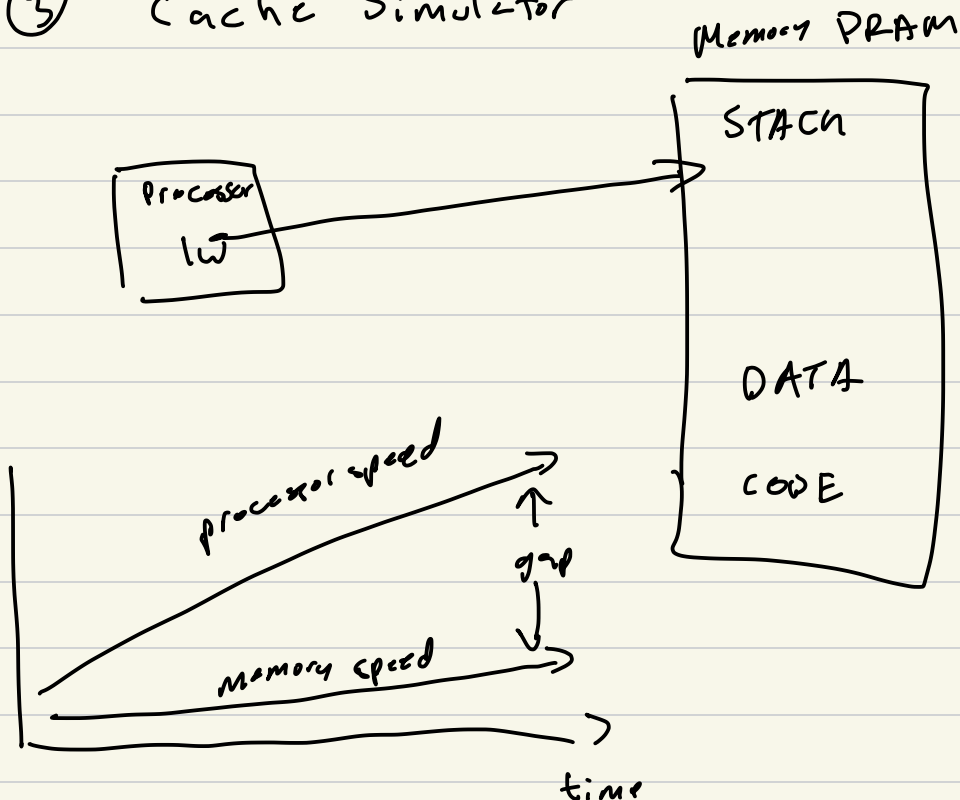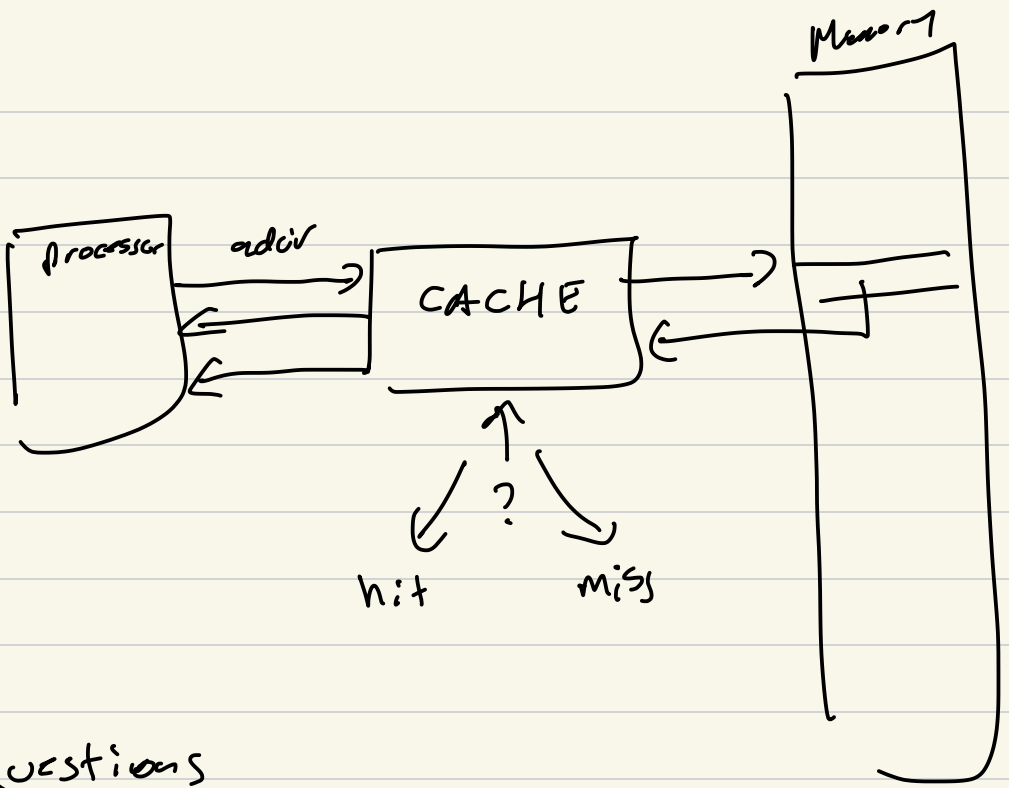
Questions

1) Where to look for a given addr ?

2) How to know if an addr is in the cache?

3) How to resolve a conflict?