CS 631-01 RISC-V Emulation

Memord RISC-V STACK Processor ress HEAP DATA CODE emu addaojaajal 10+00BS 05 23 RISC-V (code) Emulation e Processor Struct ress Stack

RISC. V Emulator Implementantion

Incremental approach

1 Identify an instruction ADDI

3 Identify instruction format i-type

(3) Implement of add to current implementation

(4) Decede IW
get fields

5 Construct an immediate from IW

(6) Undating state
update rd
update memory
update pc

STACK init stack ru-state ress(32) evholated SP

now instruction francts

immediates

jump and branches

Menucy

JAL J-type immediate jal call 12-1 10:1 1 19:12 10 opcode 20 19; 2 III 10:1 inm21 int 64_t = imm 64 = sisn_ext (imm 21, 20). B- type beg rsi, rsz, label LW |W rd, offset (151)

wint (4-t base + offset

target, add r = base + offset vint 32-+ volue = * ((vint 32-+*) + - ro=t-add/)