MBED - Data Processing and Branching

NXP LPC1768 Manual, 34.2.5 & 34.2.9

Table 620. Data processing instructions

Mnemonic	Brief description
ADC	Add with Carry
ADD	Add
ADDW	Add
AND	Logical AND
ASR	Arithmetic Shift Right
BIC	Bit Clear
CLZ	Count leading zeros
CMN	Compare Negative
CMP	Compare
EOR	Exclusive OR
LSL	Logical Shift Left
LSR	Logical Shift Right
MOV	Move
MOVT	Move Top
MOVW	Move 16-bit constant
MVN	Move NOT
ORN	Logical OR NOT
ORR	Logical OR
RBIT	Reverse Bits
REV	Reverse byte order in a word
REV16	Reverse byte order in each halfword
REVSH	Reverse byte order in bottom halfword and sign extend
ROR	Rotate Right
RRX	Rotate Right with Extend
RSB	Reverse Subtract
SBC	Subtract with Carry
SUB	Subtract
SUBW	Subtract
TEQ	Test Equivalence
TST	Test

Add and Subtract

- ADD - Add source register and value to destination register.
- ADC - Similar to ADD, also adds the Carry flag.
- SUB - Subtract value from source register, store in destination.
- SBC - Similar to SUB, also subtract inverse of Carry flag.
- RSB - Subtract source register from value.

Add and Subtract

op{S}{cond} {Rd,} Rn, Operand2

op{cond} {Rd,} Rn, #imm12 (ONLY ADD/SUB)

S - update the status flags

Logical Operations

op{S}{cond} {Rd,} Rn, Operand2

- AND - Bitwise AND
- ORR - Bitwise OR
- EOR - Exclusive OR (XOR)
- BIC - Bit Clear (Inverted AND)
- ORN - Bitwise Inverted OR

Shift Operations

op {S}{cond} Rd, Rm, Rs

op {S}{cond} Rd, Rm, #n

- ASR - Arithmetic Shift Right (1-32)
- LSL - Logical Shift Left (0-31)
- LSR - Logical Shift Right (1-32)
- ROR - Rotate Right (1-31)
- RRX - Rotate Right with Extend

Count Leading Zeros

CLZ{cond} Rd, Rm

Count the leading zeros (From msb) in Rm

Compares

- Compare (like SUBS)

  CMP{cond} Rn, Operand2

- Compare Negative (like ADDS)

  CMN{cond} Rn, Operand2

  *Discards the result (only for setting status bits)

Move

- Move register or 16 bit value

  MOV{S}{cond} Rd, Operand2

  MOV{cond} Rd, #imm16

- Move Inverse (Bitwise NOT)

  MVN{S}{cond} Rd, Operand2

Move Top

MOVT{cond} Rd, #imm16

- Place given value in top halfword of Rd
- Bottom halfword is not affected
- Combine with MOV to create ANY 32-bit constant!

Reverse Bits or Bytes

op{cond} Rd, Rn

- REV - Reverse BYTE order in word
- REV16 - Reverse BYTE order in each halfword
- REVSH - Reverse BYTE order in bottom halfword, sign extend
- RBIT - Reverse BIT order in word (all bits)

Test

- Test (like ANDS)

  TST{cond} Rn, Operand2

- Test Equivalence (like EORS)

  TEQ{cond} Rn, Operand2

* Discards result (only for setting status bits)

Table 623. Branch and control instructions

Mnemonic	Brief description
B	Branch
BL	Branch with Link
BLX	Branch indirect with Link
BX	Branch indirect
CBNZ	Compare and Branch if Non Zero
CBZ	Compare and Branch if Non Zero
IT	If-Then

Branch, Link, and Exchange

- B{cond} label
- BL{cond} label
- BX{cond} Rm
- BLX{cond} Rm

L (Link) - Save the return address in LR

X (Exchange) - Address come from register vice label

Branch

For BX and BLX:

lsb of Rm must be 1. Actual lsb of address will still be 0.

Bcond - Only conditional instruction allowed outside an IT block

Compare and Branch

Branch if Rn is zero

- CBZ Rn, label

Branch if Rn is non-zero

- CBNZ Rn, label

* Status flags are not affected!

If-Then Conditional Blocks

IT{x{y{z}}} cond

- Conditionally execute the following 4 instructions
- x,y,z can each be T (Then) or E (Else)
- Must include associated condition with each command in block
- Only the last instruction in the block may modify PC