MBED - Processor User Guide

NXP LPC1768 Manual, 34.3

Processor Modes

- Thread Mode
  - For executing software
- Handler Mode
  - For exceptions

Privilege Levels

- Unprivileged
  - Somewhat limited access
- Privileged

Table 626. Summary of processor mode, execution privilege level, and stack use options

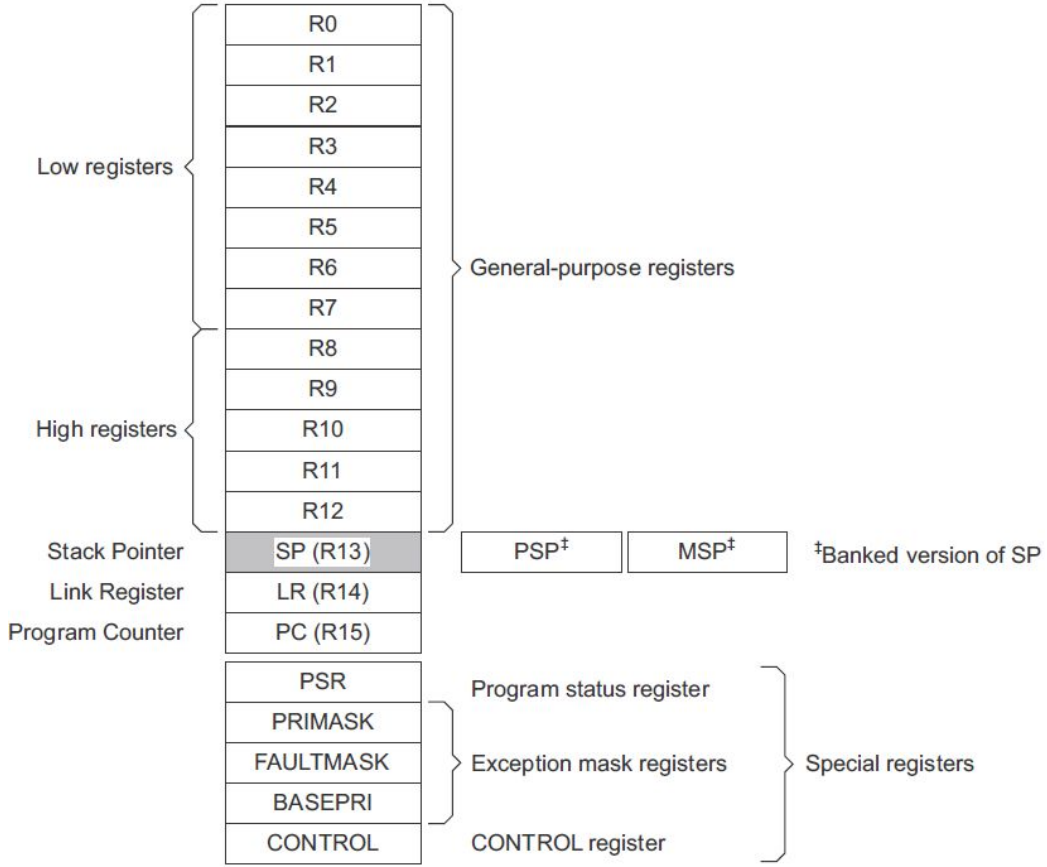
Processor mode	Used to execute	Privilege level for software execution	Stack used
Thread	Applications	Privileged or unprivileged[1]	Main stack or process stack[1]
Handler	Exception handlers	Always privileged	Main stack

Stacks

- Last In First Out (LIFO)
- Main Stack
- Process Stack

Core Registers

- General Purpose (R0-R12)
- Stack Pointer (SP)
- Link Register (LR)
- Program Counter (PC)
- Special Registers
  - Program Status Register
  - Exception Mask Registers
  - CONTROL Register



Stack Pointer

- R13
- Chosen by Thread Mode bit (CONTROL Register)
- Set from address 0x00000000 on Reset

Link Register

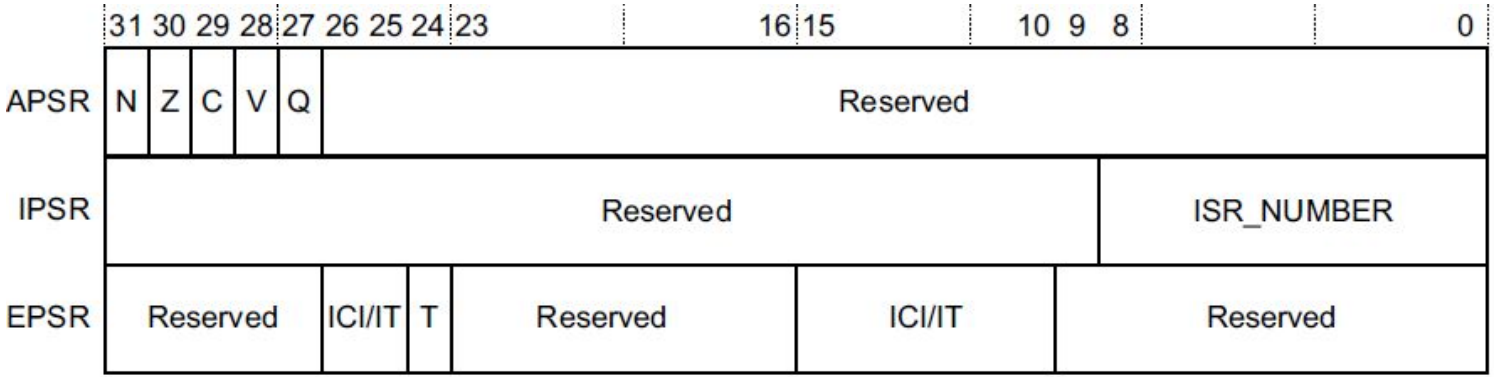
- R14
- Return address for subroutines/exceptions

Program Counter

- R15
- Current program address
- Lsb always 0 for halfword alignment
- Loads Reset Vector value (0x00000004) on Reset

Program Status Register

- Application PSR
  - Condition Flags from previous instructions
- Interrupt PSR
  - Exception type of current Interrupt Service Routine (ISR)
- Execution PSR
  - Thumb State bit
  - Execution State of IF-THEN or Interruptible-Continuable Instruction



APSR Status Bits

Table 629. APSR bit assignments

Bits	Name	Function
[31]	N	Negative or less than flag: 0 = operation result was positive, zero, greater than, or equal 1 = operation result was negative or less than.
[30]	Z	Zero flag: 0 = operation result was not zero 1 = operation result was zero.
[29]	C	Carry or borrow flag: 0 = add operation did not result in a carry bit or subtract operation resulted in a borrow bit 1 = add operation resulted in a carry bit or subtract operation did not result in a borrow bit.
[28]	V	Overflow flag: 0 = operation did not result in an overflow 1 = operation resulted in an overflow.
[27]	Q	Sticky saturation flag: 0 = indicates that saturation has not occurred since reset or since the bit was last cleared to zero 1 = indicates when an `SSAT` or `USAT` instruction results in saturation. This bit is cleared to zero by software using an `MRS` instruction.
[26:0]	-	Reserved.

CONTROL Register

- Determines Stack
  - MSP or PSP
  - Handler Mode always uses MSP
  - Thread Mode defaults to MSP
  - For an OS, threads should use PSP
- Determines Privilege Level (Thread Mode only)

Table 635. CONTROL register bit assignments

Bits	Name	Function
[31:2]	-	Reserved
[1]	Active stack pointer	Defines the current stack: 0 = MSP is the current stack pointer 1 = PSP is the current stack pointer. In Handler mode this bit reads as zero and ignores writes.
[0]	Thread mode privilege level	Defines the Thread mode privilege level: 0 = privileged 1 = unprivileged.

Exceptions and Interrupts

- NVIC prioritizes and handles all exceptions
- Handler Mode for all exceptions, except Reset

Data Types

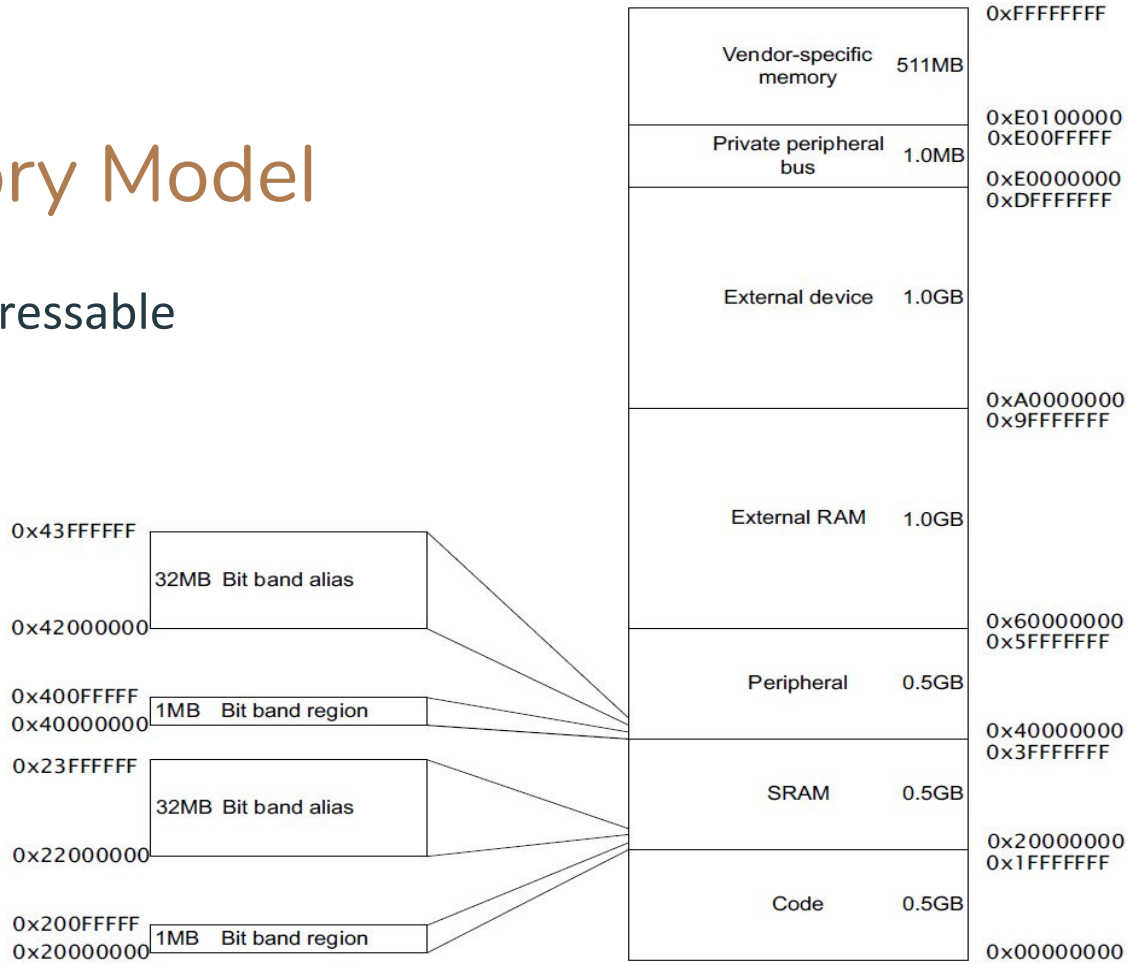
- 8 bits (BYTE)
- 16 bits (HALFWORD)
- 32 bits (WORD)
- Little Endian!

CMSIS

- Cortex Microcontroller Software Interface Standard
  - Meant to simplify development
- Access peripheral registers
- Define Exception Vectors
- Names of the above
- Device independent interface for RTOS kernels

Memory Model

4 GB Addressable



Memory Types

- Normal
  - Allows reordering transactions for efficiency. Allows Speculative reads.
- Device
  - Preserve transaction order relative to Device or Strongly-Ordered transactions
- Strongly-Ordered
  - Preserve transaction order relative to ALL other transactions
  - Writes cannot be buffered

Memory Attributes

- Shareable
  - Allows Bus Masters to synchronize data
  - Responsible for ensuring data coherency
- Execute Never (XN)
  - Prevents instruction access with Memory Management Fault

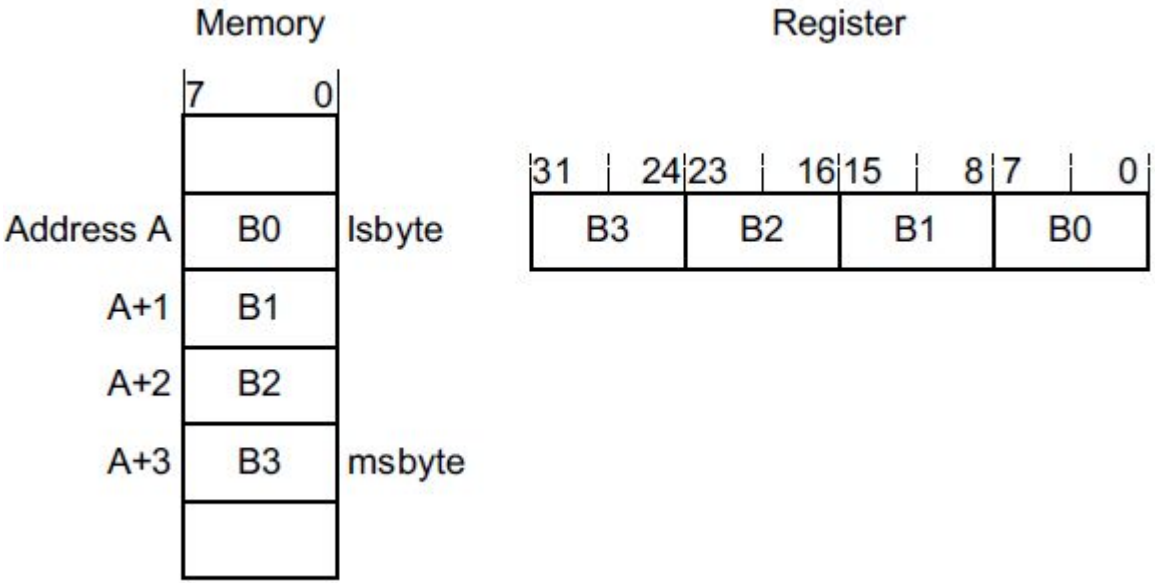
Memory Accesses

Table 636. Memory access behavior

Address range	Memory region	Memory type	XN	Description
0x00000000 - 0x1FFFFFFF	Code	Normal[1]	-	Executable region for program code. You can also put data here.
0x20000000 - 0x3FFFFFFF	SRAM	Normal[1]	-	Executable region for data. You can also put code here. This region includes bit band and bit band alias areas, see Table 637.
0x40000000 - 0x5FFFFFFF	Peripheral	Device[1]	XN[1]	This region includes bit band and bit band alias areas, see Table 638.
0x60000000 - 0x9FFFFFFF	External RAM	Normal[1]	-	Executable region for data.
0xA0000000 - 0xDFFFFFFF	External device	Device[1]	XN[1]	External Device memory
0xE0000000 - 0xE00FFFFF	Private Peripheral Bus	Strongly-ordered[1]	XN[1]	This region includes the NVIC, System timer, and system control block.
0xE0100000 - 0xFFFFFFFF	Vendor-specific device	Device[1]	XN[1]	Not used for NXP devices.

Defaults can be overridden by the MPU!

Memory Endianness



- Little Endian
- LSB stored first (Lowest address byte)

Exception States

- Inactive
- Pending
- Active
- Active and pending

Exception Types

- Reset
- Non-Maskable Interrupt (NMI)
- Hard Fault
- Memory Management Fault
- Bus Fault
- Usage Fault

Exception Handlers

- Interrupt Service Routines (ISR)
- Fault Handlers
- System Handlers

Vector Table

- At address 0x00000000 on Reset
- Contains initial value of SP
- Starting addresses for all exception handlers

Exception number	IRQ number	Offset	Vector
127	111	0x1FC	IRQ111
.	.	.	.
.	.	.	.
.	.	.	.
18		0x004C	IRQ2
17	2	0x0048	IRQ1
16	1	0x0044	IRQ0
15	0	0x0040	Systick
14	-1	0x003C	PendSV
13	-2	0x0038	Reserved
12			Reserved for debug
11			SVCall
10	-5	0x002C	Reserved
9			
8			
7			
6	-10	0x0018	Usage fault
5	-11	0x0014	Bus fault
4	-12	0x0010	Memory management fault
3	-13	0x000C	Hard fault
2	-14	0x0008	NMI
1		0x0004	Reset
		0x0000	Initial SP value.

Fig 149. Vector table

Exception Priorities

- Lower number means higher priority
  - -3 is highest
- Configurable, except for:
  - Reset (-3)
  - NMI (-2)
  - Hard Fault (-1)

Exception Handling

- Preemption
  - During another exception handler
- Return
  - Restore state prior to exception
- Tail-Chaining
  - For Speed. Forgo stack pop and move to handle next exception
- Late-Arriving
  - For Speed. Handle higher priority exception during exception state saving

Exception Entry

Pending exception with sufficient priority

- Thread mode
- Higher priority exception

Exception Stack Frame

- R0-R3, R12
- Return Address
- LR
- PSR

Exception Return

Handler Mode, load EXC_RETURN value into PC

- POP to PC
- BX
- LDR/LDM with PC destination

Power Management

Reduced power modes:

- Sleep Mode
- Deep Sleep Mode

Sleep Mode

- Wait for Interrupt
- Wait for Event
- Sleep on Exit

Return with Wake-Up Interrupt Controller (WIC)

Power Management Functions

ANSI C cannot generate Sleep commands.

Need help from CMSIS intrinsic functions

- void __WFE(void);
- void __WFI(void);