



Xilinx-FPGA 数字系统设计

B-509: 周五 5-6 节
(网通/嵌入...)

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助教: 叶景涛、杨佳雯



教材：+DVD实验源代码



“本书系统地介绍了Xilinx公司FPGA的结构特点和相关开发软件的使用方法，详细描述了VHDL语言的语法和设计方法，并深入讨论了Xilinx FPGA相关硬件的设计问题。全书共分为七章。第1章概要介绍了FPGA知识。第2章介绍了Xilinx FPGA开发的常用软件及一般的开发流程。第3章详细讲述了VHDL硬件描述语言。第4章讨论了Xilinx FPGA开发中常用的IP核及其使用方法，并着重描述了时钟管理IP核的参数配置。第3章和第4章的内容是Xilinx FPGA开发的基础。第5章讲述了Xilinx FPGA的相关硬件设计方法，并给出了参考电路。第6章和第7章是实验部分，包括程序设计实验和FPGA逻辑设计实验。本书是在Xilinx公司大学计划的支持下完成的，内容浅显易懂，简洁精炼，实验可操作性强，是Xilinx FPGA开发的入门教材，可作为高等院校电子类和通信类各专业本科生、研究生EDA课程的教材。”

目录： + VHDL-CPU 设计实例（PARWAN）



第1章 绪论 1.1 逻辑器件概述 1.2 可编程逻辑器件PLD的发展历程 1.3 FPGA的特点 1.4 CPLD/FPGA的基本结构
1.4.1 CPLD的基本结构 1.4.2 FPGA 的基本结构 1.4.3 CPLD与FPGA 比较 1.5 Xilinx FPGA产品介绍 1.5.1
Xilinx 公司概述 1.5.2 Xilinx FPGA产品 第2章 开发软件与开发流程 2.1 开发软件简介 2.1.1 ISE开发软件简介
2.1.2 ISE9.1i的安装 2.1.3 ModelSim仿真软件简介 2.2 一个简单的开发项目 2.3 开发软件使用进阶 2.3.1
ISE9.1i集成开发环境界面 2.3.2 设计输入 2.3.3 设计综合 2.3.4 功能仿真 2.3.5 工程实现 2.3.6 时
序仿真 2.3.7 器件配置 第3章 VHDL硬件描述语言 3.1 VHDL的历史和概况 3.2 VHDL基本设计思想 3.3 VHDL
语言设计的基本单元 3.3.1 实体 3.3.2 构造体 3.3.3 配置 3.3.4 包集合 3.3.5 库 3.4 VHDL语言的
对象和数据类型 3.4.1 VHDL语言的对象类型 3.4.2 VHDL语言的数据类型 3.4.3 不同数据类型之间的转换
3.5 VHDL语言运算操作符 3.6 VHDL语言的描述语句 3.6.1 有关规则和基本语句 3.6.2 并发描述语句
3.6.3 顺序描述语句 3.6.4 其他语句 3.7 VHDL的层次结构设计 3.7.1 参数与参数配置 3.7.2 元件与元件
例化 3.7.3 generate语句 3.7.4 子程序（Subprogram） 3.7.5 VHDL的行为级建模与RTL建模 3.8 有限状态
机（FSM） 3.8.1 有限状态机（FSM） 3.8.2 一个FSM的RTL代码实例 第4章 Xilinx IP核 4.1 Xilinx的IP介绍
4.2 Xilinx IP配置工具及使用方法 4.3 时钟管理IP 4.3.1 DCM模块 4.3.2 DCM的使用方法 第5章 FPGA的配置和
电源设计 5.1 FPGA的配置 5.1.1 FPGA的配置引脚 5.1.2 FPGA的配置模式 5.1.3 FPGA的配置流程
5.1.4 FPGA的配置电路 5.2 FPGA的电源设计 5.2.1 FPGA的电源指标 5.2.2 FPGA的功耗估计 5.2.3 FPGA
的电源解决方案

教材实验（动手）



第6章 VHDL程序设计实验

- 6.1 实验一 层次化工程的创建
- 6.2 实验二 仿真测试平台的创建
- 6.3 实验三 存储器和记录类型实验
- 6.4 实验四 n比特计数器及RTL验证实验
- 6.5 实验五 比较器实验
- 6.6 实验六 算术逻辑单元实验
- 6.7 实验七 状态机实验
- 6.8 实验八 计数器实验
- 6.9 实验九 IP核应用实验
- 6.10 实验十 数字时钟管理IP核实验

第7章 FPGA逻辑设计实验

- 7.1 实验一 熟悉Xilinx开发工具
- 7.2 实验二 结构体生成向导和PACE
- 7.3 实验三 全局时钟约束实验
- 7.4 实验四 综合技巧实验
- 7.5 实验五 IP核生成实验
- 7.6 实验六 Chipscope 调试实验
- 附录A VHDL关键字
- 附录B VHDL中的运算操作符
- 附录C VHDL中的描述语句及用法
- 附录D VHDL中的属性定义
- 附录E IEEE的标准库 参考文献

相关内容（会议、讲座、报告、实验等）



- 1、FPGA基本相关知识，语言等内容
- 2、XILINX FPGA逻辑设计
- 3、XILINX-FPGA动态可重构系统设计
- 4、XILINX-FPGA嵌入式系统设计
- 5、XILINX-FPGA DSP系统设计
- 6、XILINX-FPGA 多核系统设计
- 7、基于FPGA的系统实验
- 8、专业知识讲座

课程安排



- 1、实验平台： Spartan3E及Spantan6开发板
- 2、实验工具： ISE及EDK
- 3、课程考核标准：
 - 课程报告： 30%
 - 实验报告： 40%
 - 实验及课程点名签到： 30%
- 4、实验和授课结合方式，强调动手操作能力的培养

内容介绍



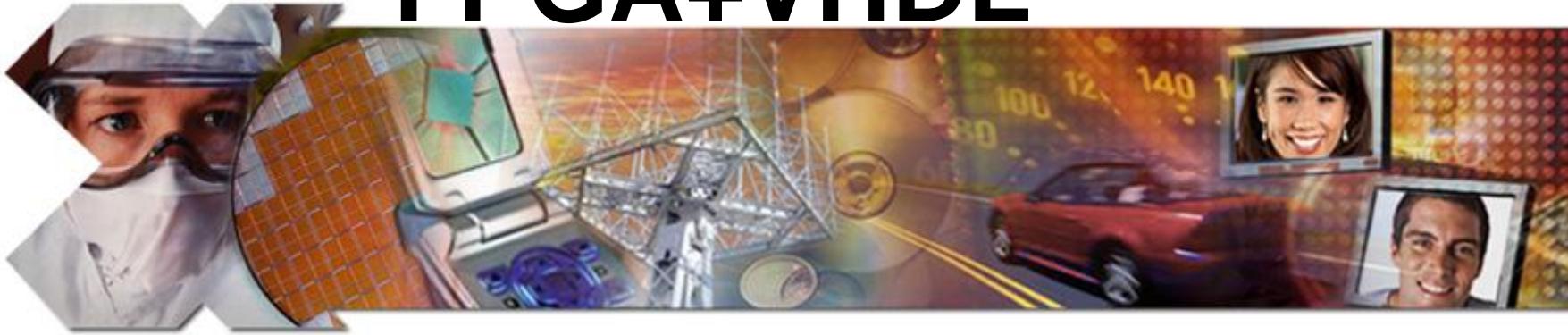
- 1、FPGA特性及功能介绍
- 2、XILINX公司简介及其FPGA产品介绍
- 3、XILINX-FPGA开发环境介绍
- 4、基于XILINX-FPGA的硬件逻辑设计介绍
- 5、基于XILINX-FPGA的嵌入式系统设计介绍

Something wrong?

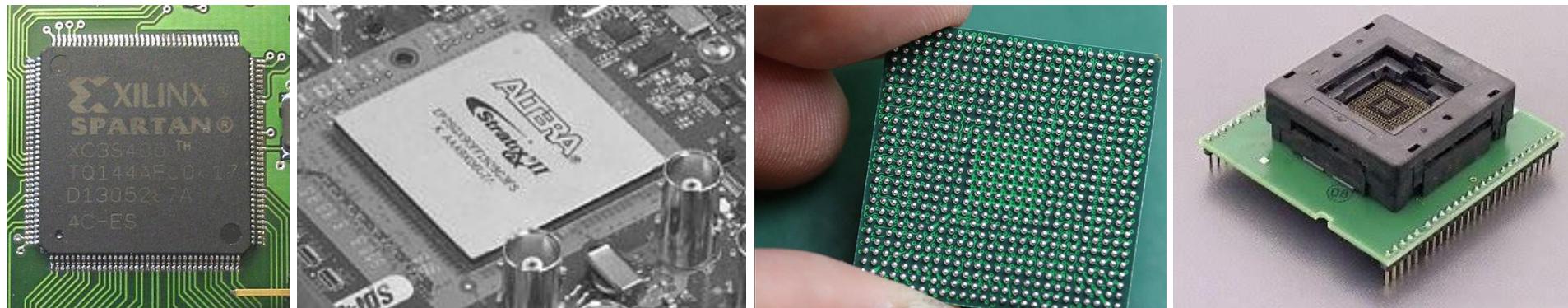


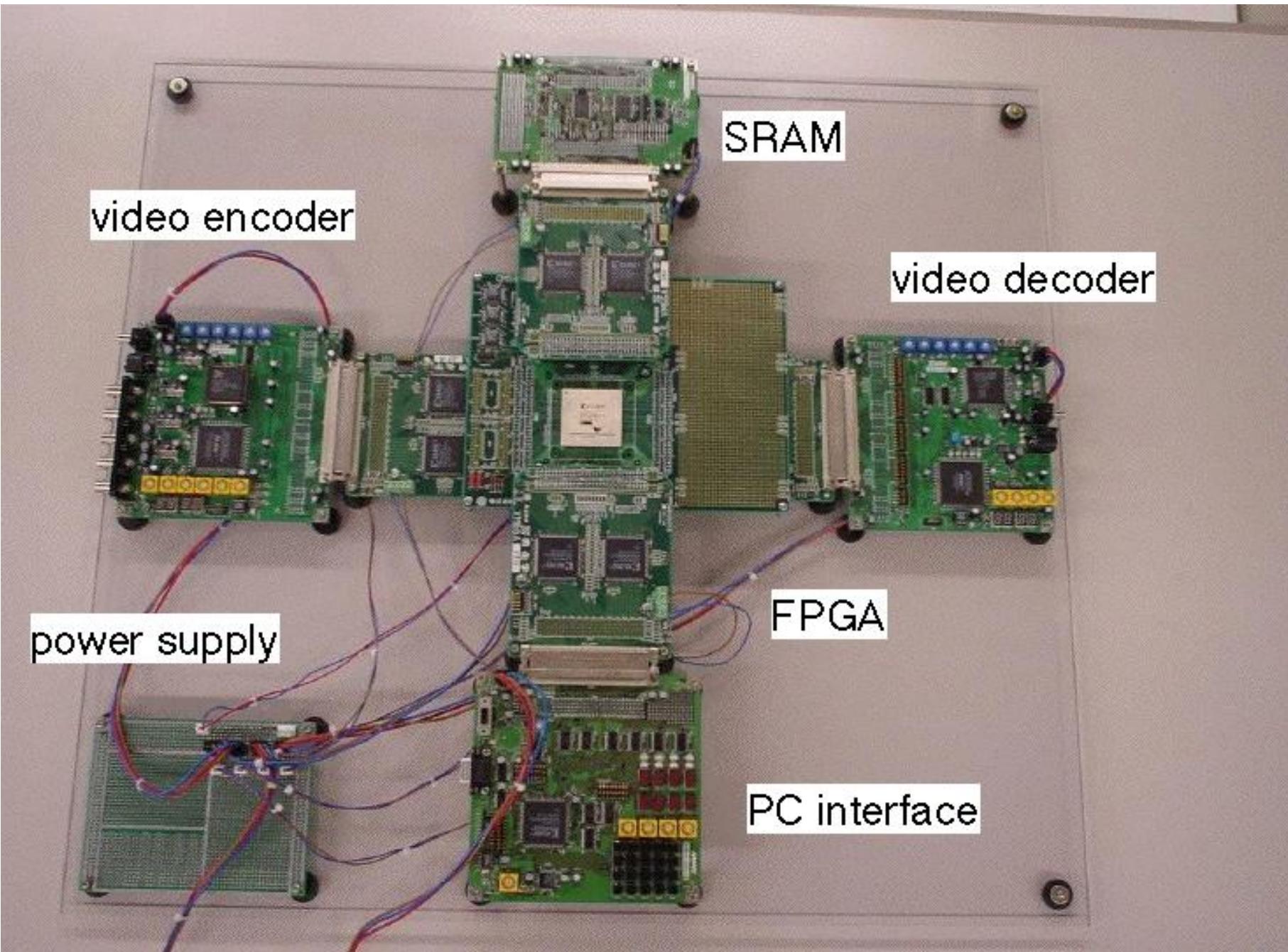
- Why should I enroll in this course? ...syllabus...
- Who am I? Looser or winner.
- Help: ...surfing...
- ... xilinx.com...
- ... no one else but you...(labs, labs, labs)

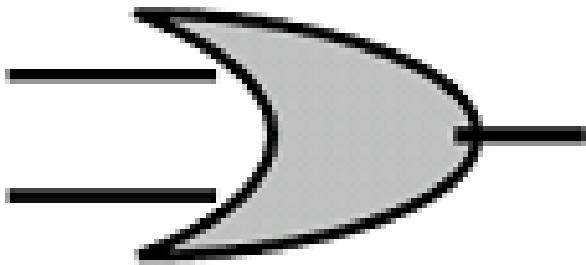
FPGA+VHDL



- FPGA: Field Programmable Gate Array
- VHDL: VHSIC Hardware Description Language
 - VHSIC: Very High-Speed Integrated Circuit





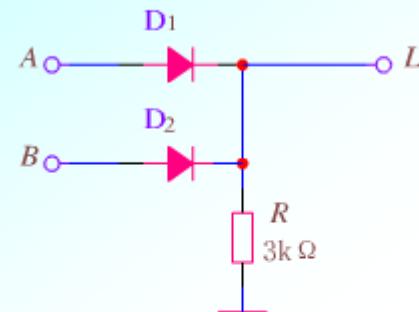


$$A=b+c$$

?

?

或门电路



输入、输出电压之间的关系

输入		输出
V _A (V)	V _B (V)	V _L (V)
0V	0V	0V
0V	5V	5V
5V	0V	5V
5V	5V	5V



或逻辑真值表

输入		输出
A	B	L
0	0	0
0	1	1
1	0	1
1	1	1



XILINX®

Just one statement?

Library ieee

Use ieee.std_logic_1164.all;

Use ieee.std_logic_arith.all;

Use ieee.std_logic_unsigned.all;

Entity device is

port(b: in std_logic; c: in std_logic; a: out std_logic);

End device

Architecture behavioral of device is

A<=b or c;

End behavioral

$$A = b + c$$

Agenda

- ◆ XILINX Overview
- ◆ Open Source Hardware Overview
- ◆ Xilinx University Program introduction



XILINX Introduction



Ross Freeman是Xilinx创始人之一，发明了“现场可编程门阵列”（FPGA）这种新型可编程逻辑。



Bernie Vonderschmitt是Xilinx创始人之一，提出了“无工厂-fabless”半导体这一创新理论。
outsourcing the fabrication

Foundries are typically located in China [1] [2] [3] [4]

References[edit]

"The UK manufacturer taking on China". [BBC Online](#). 2012-05-07.

Henry Blodget (2012-01-22). "[This Article Explains Why Apple Makes iPhones In China And Why The US Is Screwed](#)". [Business Insider](#).

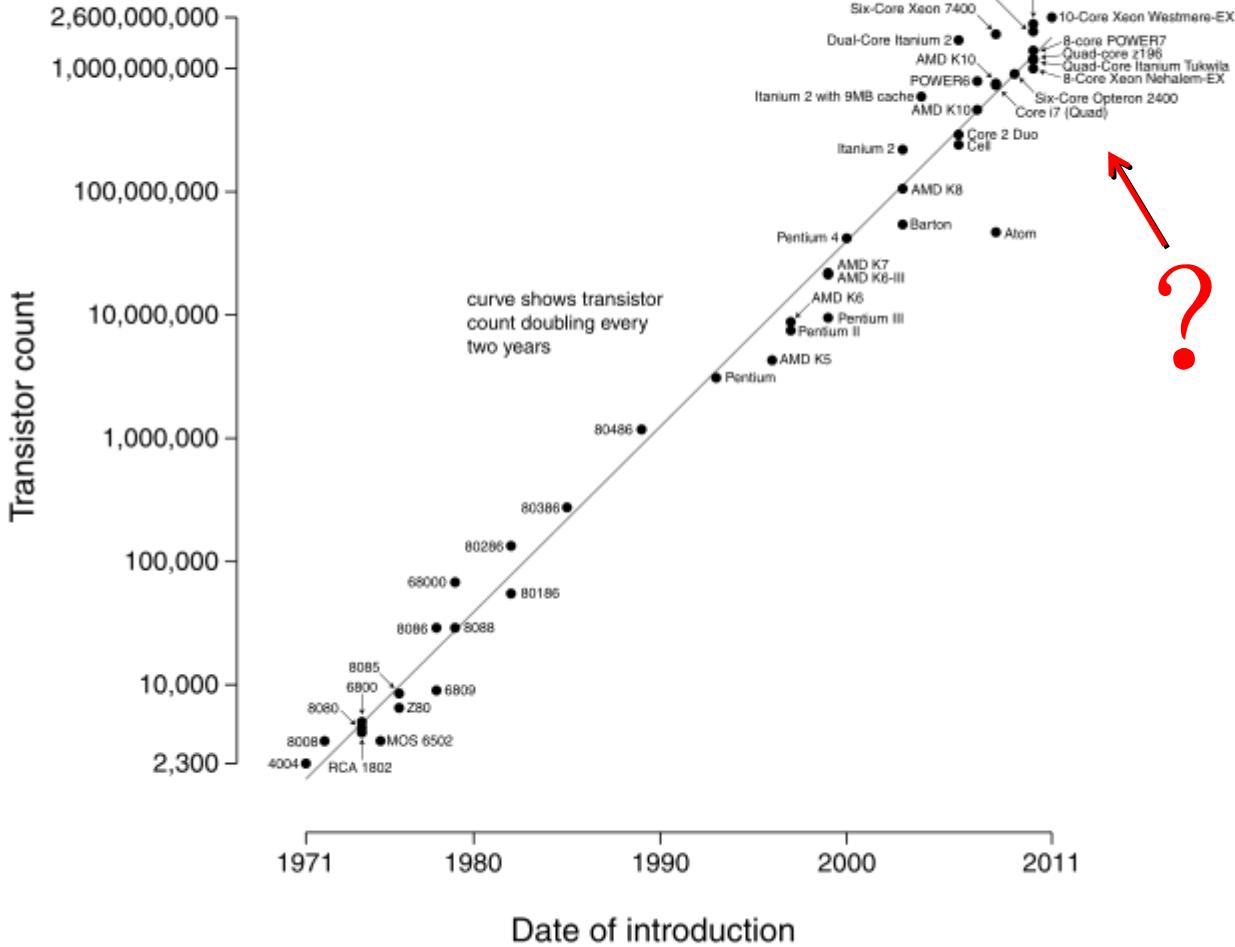
Jim Pinto. "[Global Manufacturing – The China Challenge](#)". Archived from [the original](#) on 2012-01-12.

Rounak Jain (2012-01-22). "[Why Does Apple Manufacture iPhone in Asia?](#)". [iphonehacks.com](#).

http://en.wikipedia.org/wiki/Fabless_semiconductor_company

now? ... Foundries are typically located in China ...

Microprocessor Transistor Counts 1971-2011 & Moore's Law



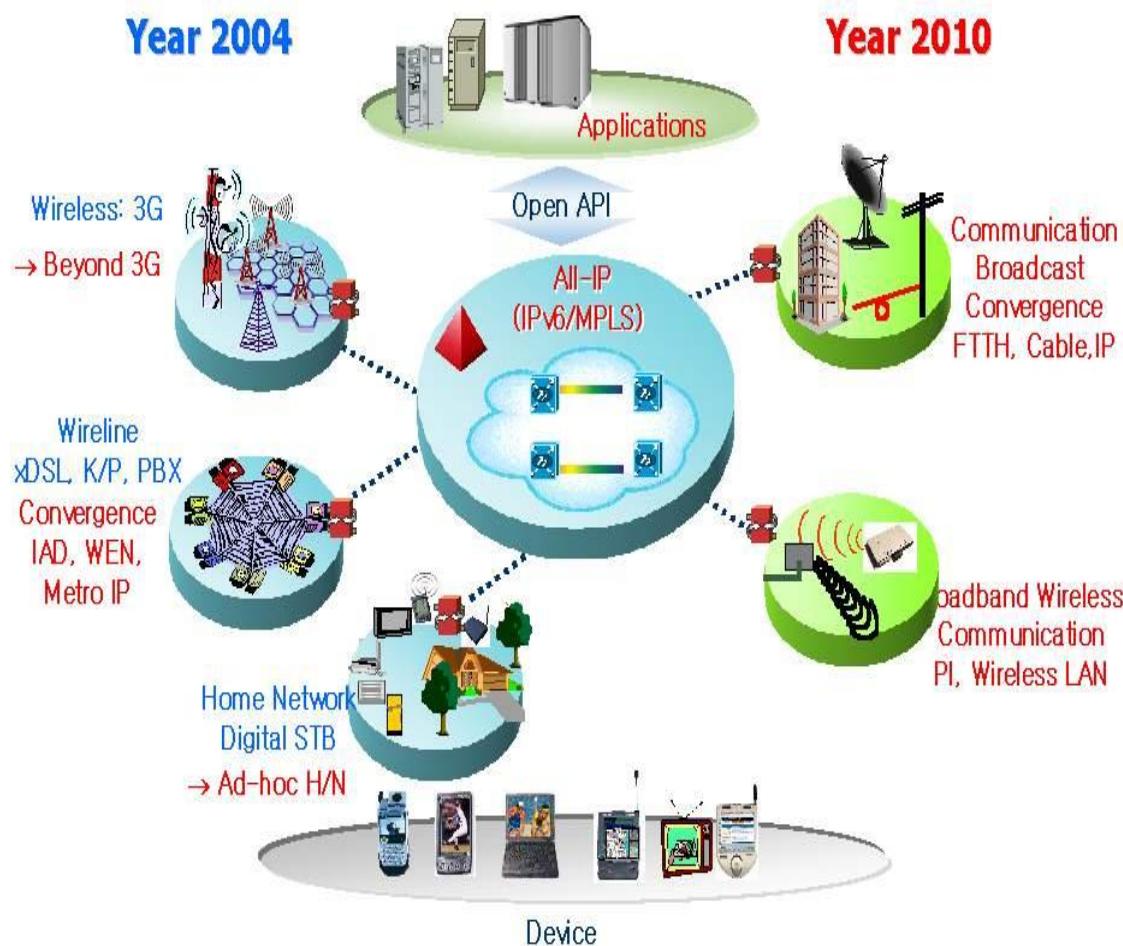
An Osborne Executive portable computer, from 1982 with a Zilog Z80 4MHz CPU, and a 2007 Apple iPhone with a 412MHz ARM11 CPU. The Executive weighs 100 times as much, has nearly 500 times as much volume, cost approximately 10 times as much (adjusted for inflation), and has about 1/100th the clock frequency of the smartphone.



Gordon Moore in 2004

Moore's law is the observation that, over the history of computing hardware, the number of transistors on integrated circuits doubles approximately every two years. The law is named after Intel co-founder Gordon E. Moore, who described the trend in his 1965 paper.^{[1][2][3]}

Driving Force : Triple Play



1. Digital Signal Processing

- Transforming data

2. Packet Processing

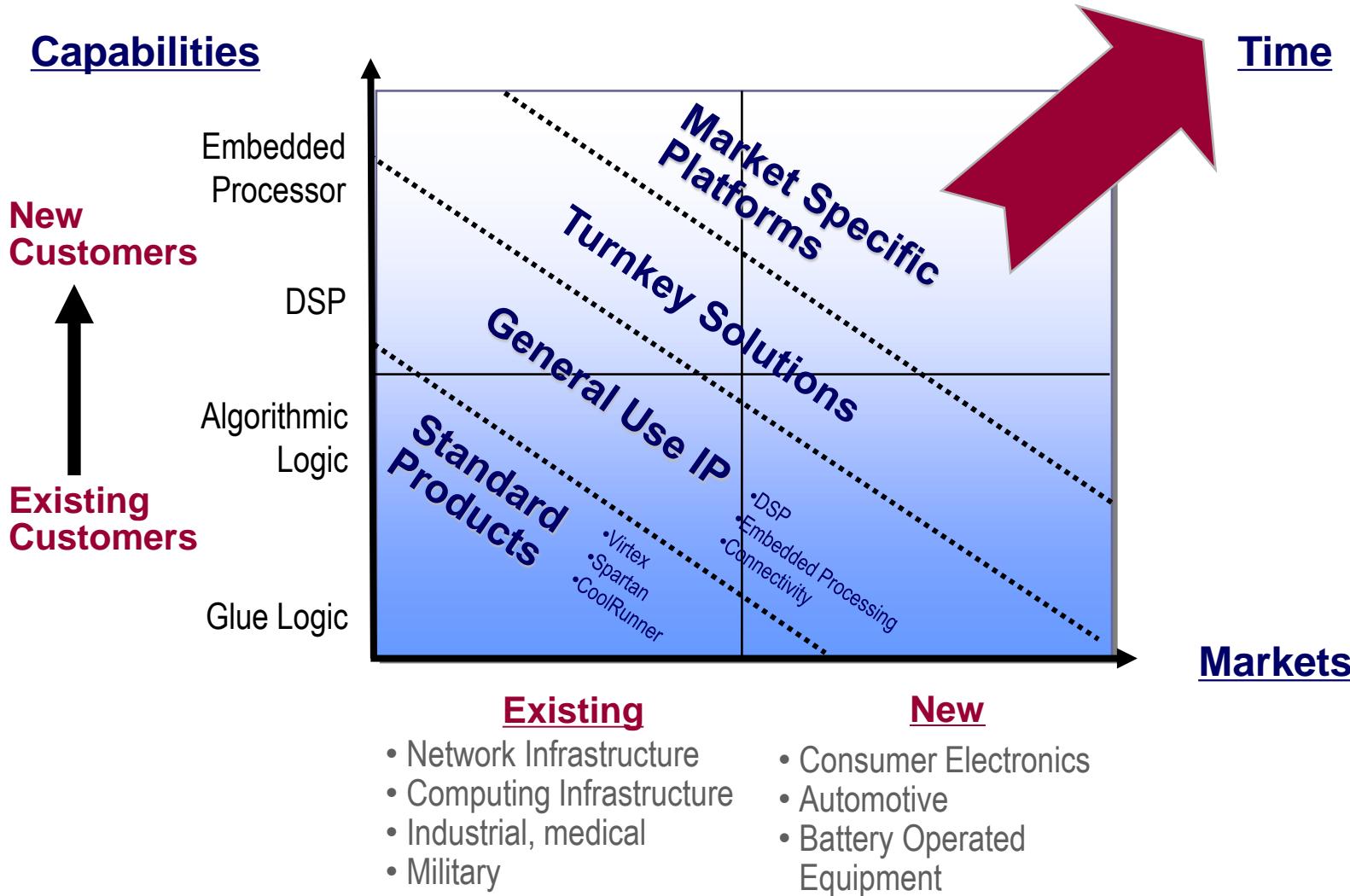
- Transporting data

3. Tera Computing

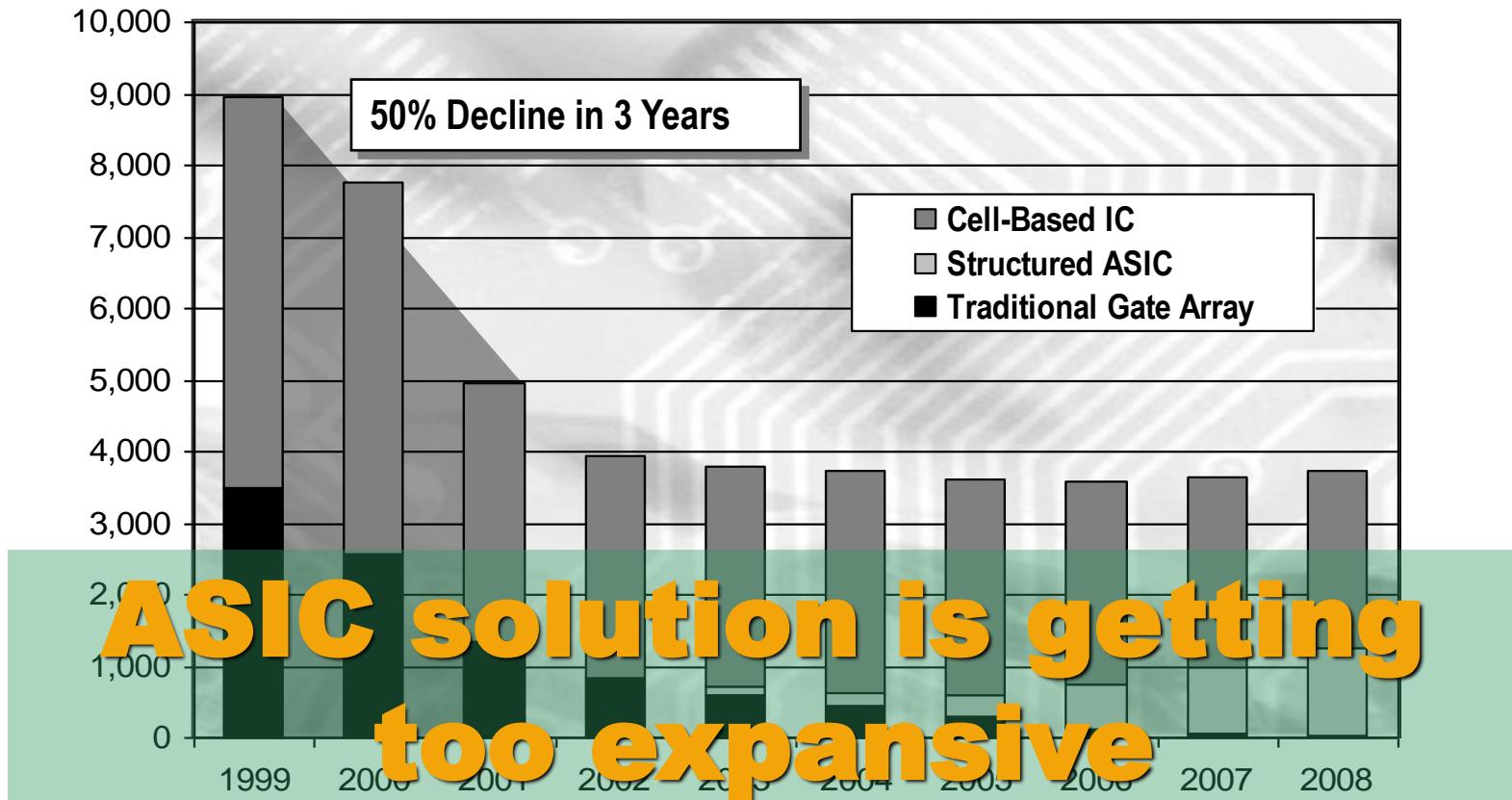
- Analyzing data

The Age of Specialization

个性化时代



Declining ASIC Design Starts



**ASIC solution is getting
too expensive**

*“Skyrocketing mask costs, high tool costs and high development costs have ensured that only very high-volume designs can be supported with cell-based ASICs. For mid-volume ASIC designs, the costs are simply becoming out of reach.” **

*John Gallagher
Director of marketing for Synplicity's ASIC synthesis technologies*

获奖的企业文化

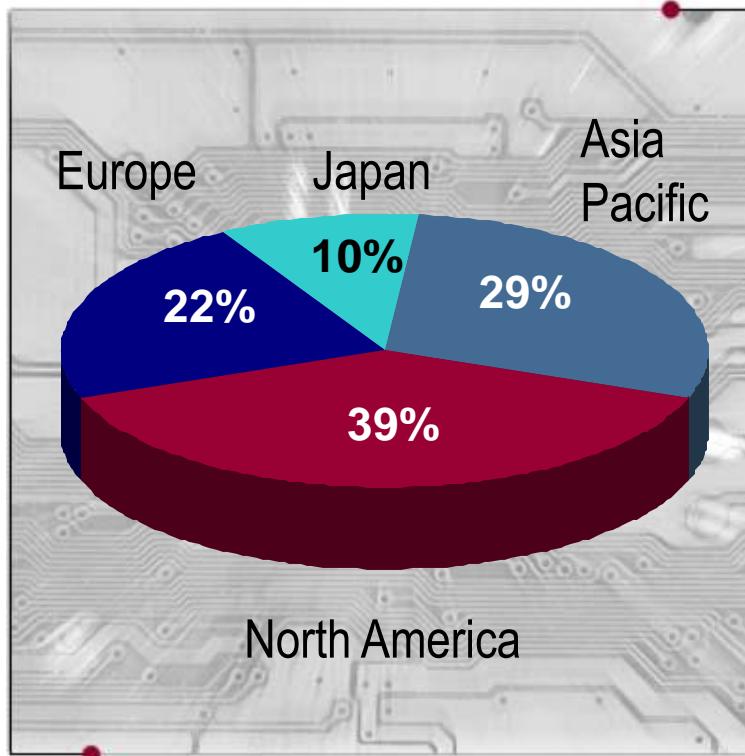
Xilinx连续5年成为财富杂志评选的百家最适宜工作的企业之一：

- 2001: #14
- 2002: #6
- 2003: #4
- 2004: #10
- 2005: #5

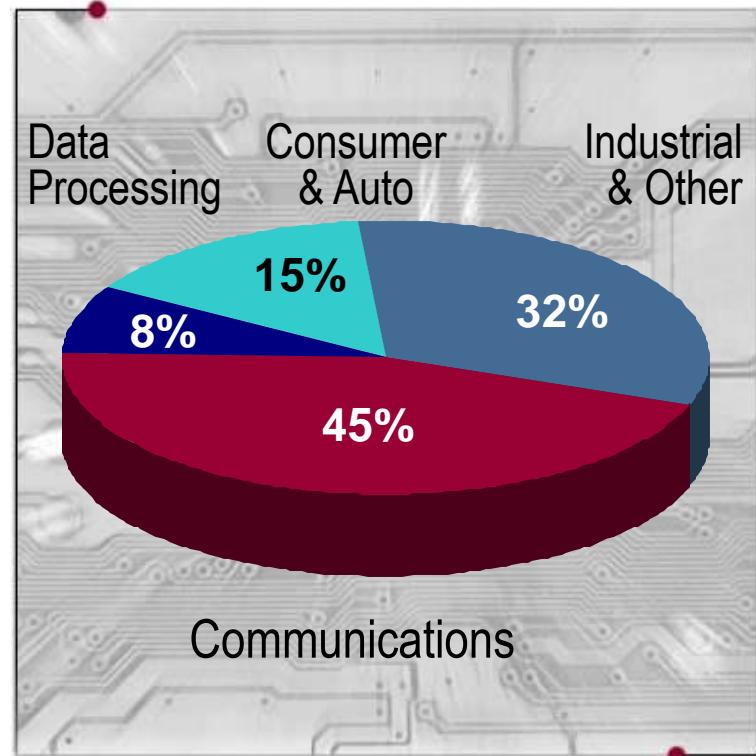
Company	
1	QUALCOMM (QCT Division)
2	Broadcomm
3	NVIDIA Corporation
4	ATI Technologies
5	SanDisk Corporation
6	Agilent (SPG Division)
7	Xilinx, Inc.
8	Marvell Technology Group Ltd.
9	MediaTek Incorporation
10	Altera

Xilinx Revenue Calendar Year 2007

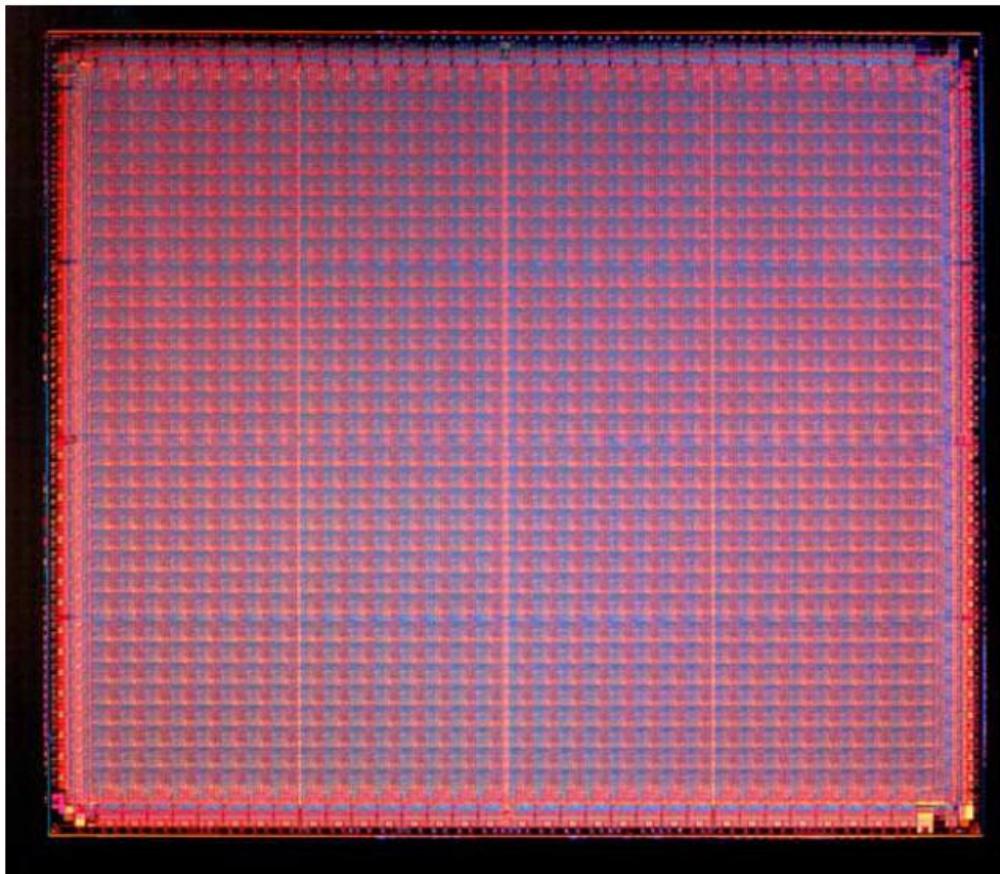
Revenue by Geography



Revenue by End Market



RAM-based FPGA



Courtesy Xilinx

Xilinx XC4000ex

Focus on Core Competencies

Differentiating



Non-differentiating

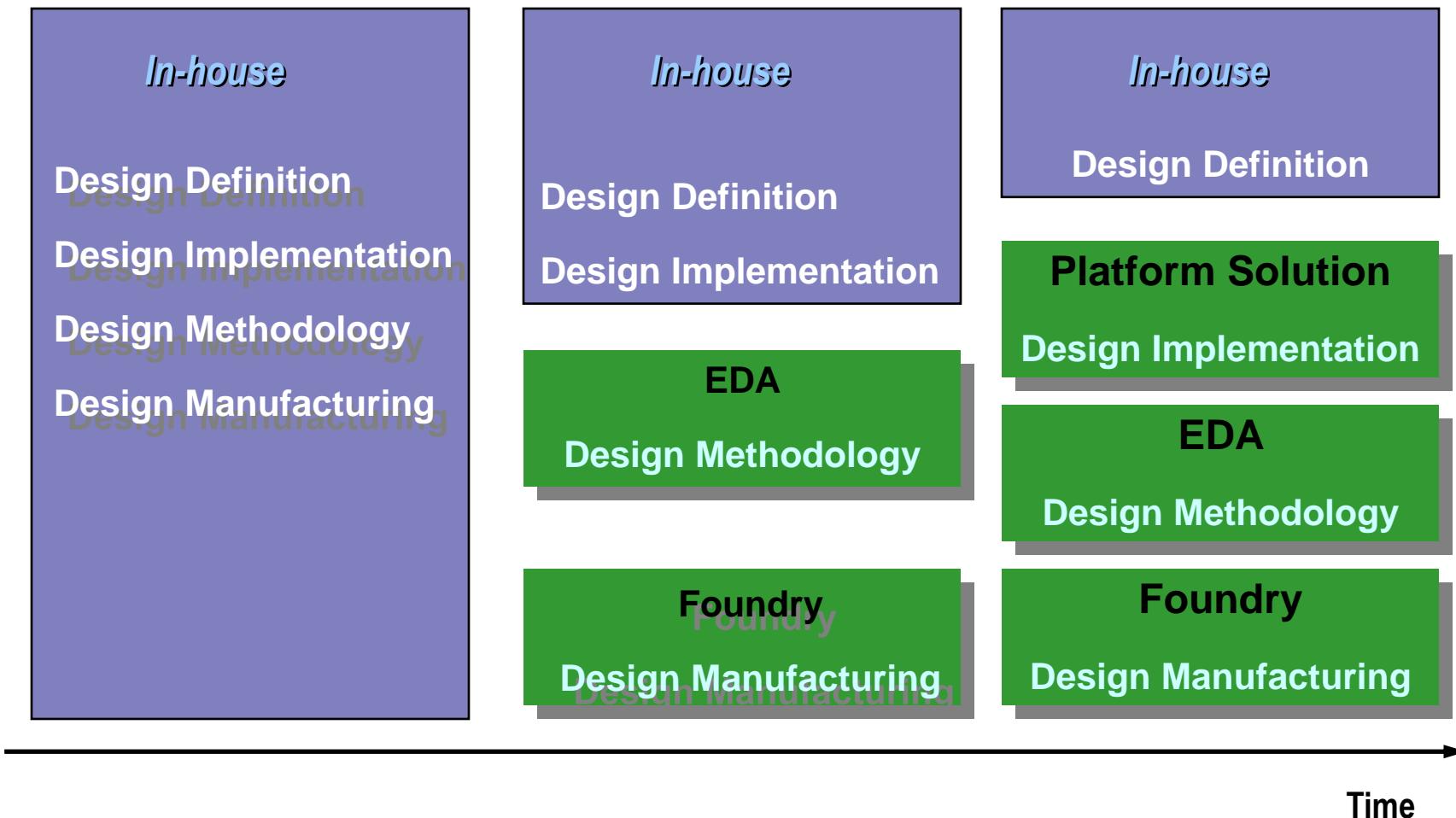
- Deep sub-micron engineering
- IC Design Tools
- Fabric architecture
- Non-differentiating, pre-verified, hard & soft IP
- Prototyping
- Signal integrity
- Advanced packaging
- Programmability & field upgradability



YOUR VALUE ?

Xilinx VALUE

The Business Model Evolves



So Does the Electronics Age...

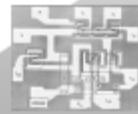
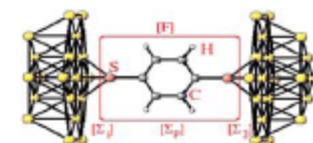


1950's

Pre-silicon

Silicon

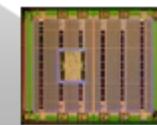
Late 2010's



70's



Late 90's



Early-Silicon

Silicon

Late-Silicon

The Custom Era

The ASIC Age

??

Case study: 1000 Picoblaze



在美国纽约的时代广场的JP Morgan Chase大楼，有一块硕大的LED广告屏。这块广告屏在当时(2004年)是世界上最大的高亮解析度的LED显示屏，而驱动这块显示屏的，正是 PicoBlaze，整个设计中用到了10块XC2V1000 Virtex-II, 323块XC3S200 Spartan-3, 以及333块XCF00 Platform Flash PROM和3800块XC9572XL72 PLD宏单元。使用到的PicoBlaze的数量更是超过了1000个。

FPGA Computing

- Xilinx Virtex-5 FPGA in standard Intel Xeon server platform socket
 - Interfaces to Intel Front-Side Bus (FSB)
 - Only FPGA capable of achieving full FSB performance
 - Implements customizable application-specific accelerators
 - Increased performance in the available power budget
- FSB: An excellent interface for accelerated computing
 - Move to more BW (PCIe x8: 2.0 GB/s, FSB1066: 8.5 GB/s)
 - Much lower latency
 - Coherent system protocol



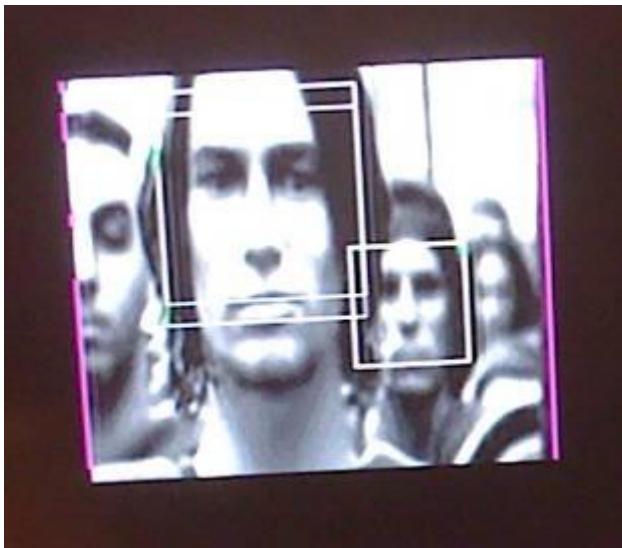
A Happy FPGA Customer
... rolling on Mars with a
Virtex-based controller
in each wheel



Accelerated face detection



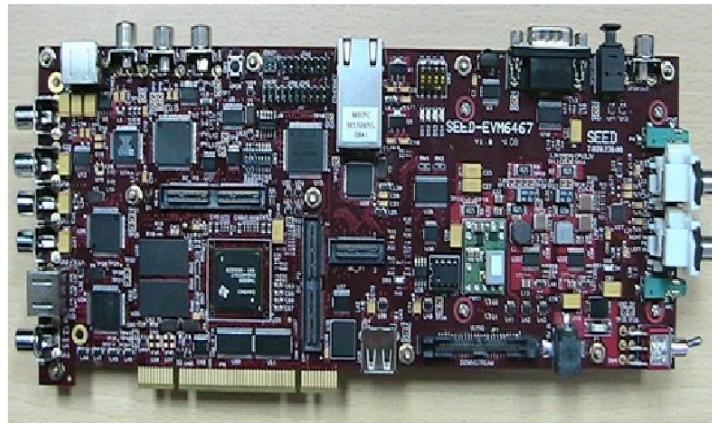
Prof. Feng Zhao
Shanghai Jiao Tong
University



- Started with software and XUP board
- Re-implemented entirely in hardware on a Xilinx Spartan 3A 1800 DSP
- 50MHz, 15~25 FPS
 - Faster than face detection on TI's DM642 DSP (600MHz VLIW)

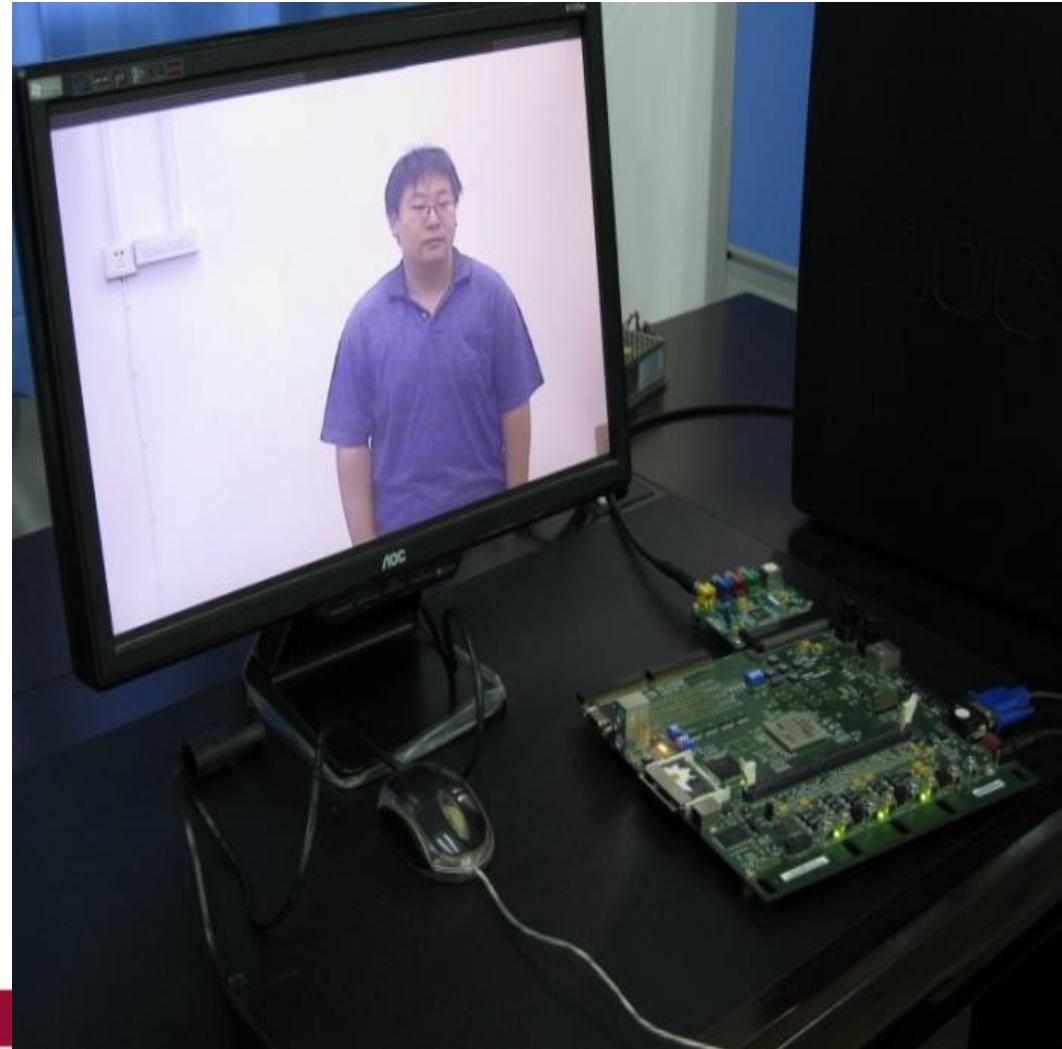
我们的研究基础

- 嵌入式系统开发-1: XILINX-V4, TI-DSP-6467

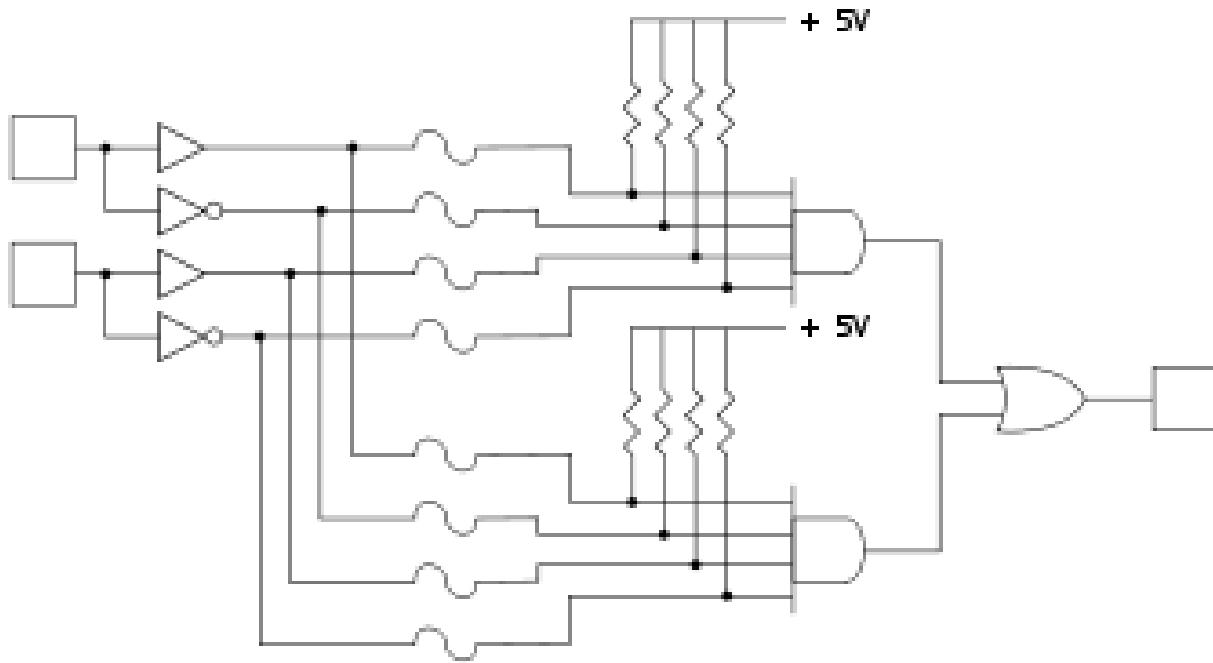


我们的研究基础

- 嵌入式系统开发-2:

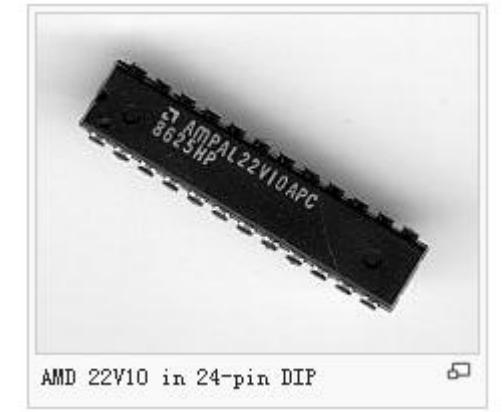


PAL

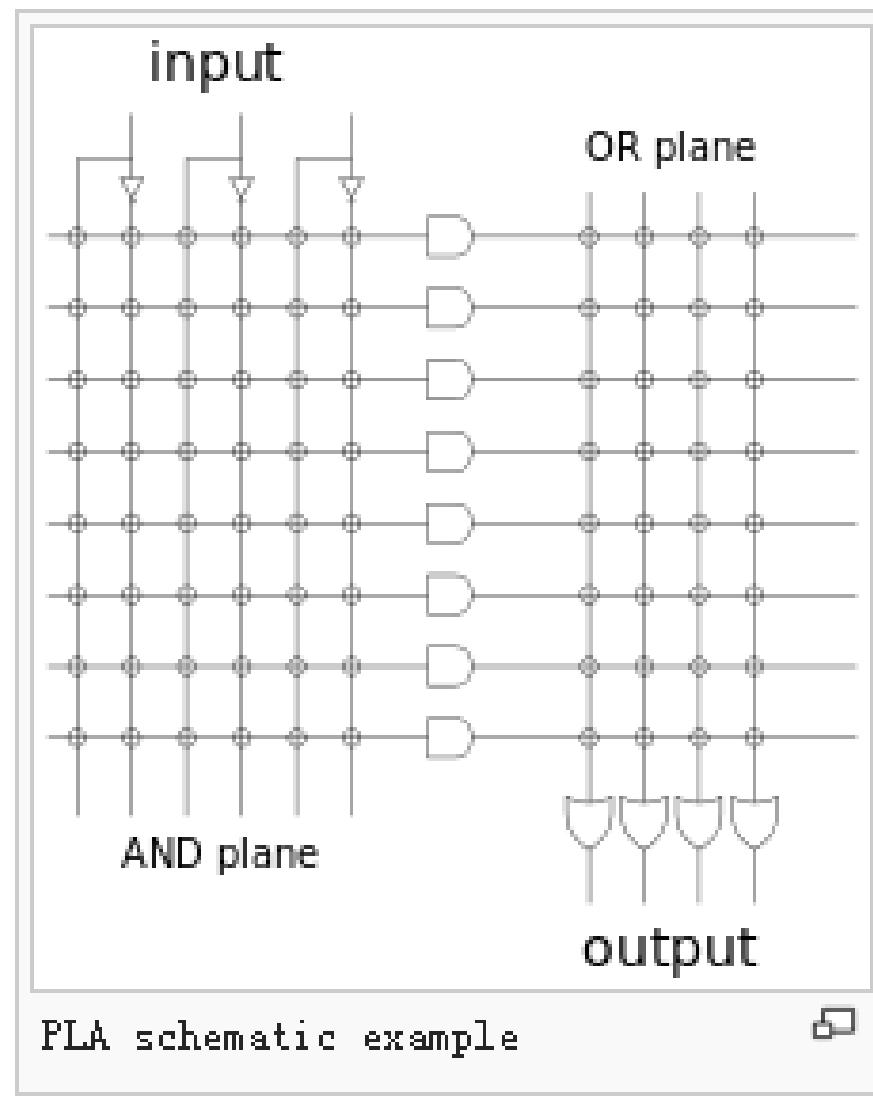


Simplified programmable logic device

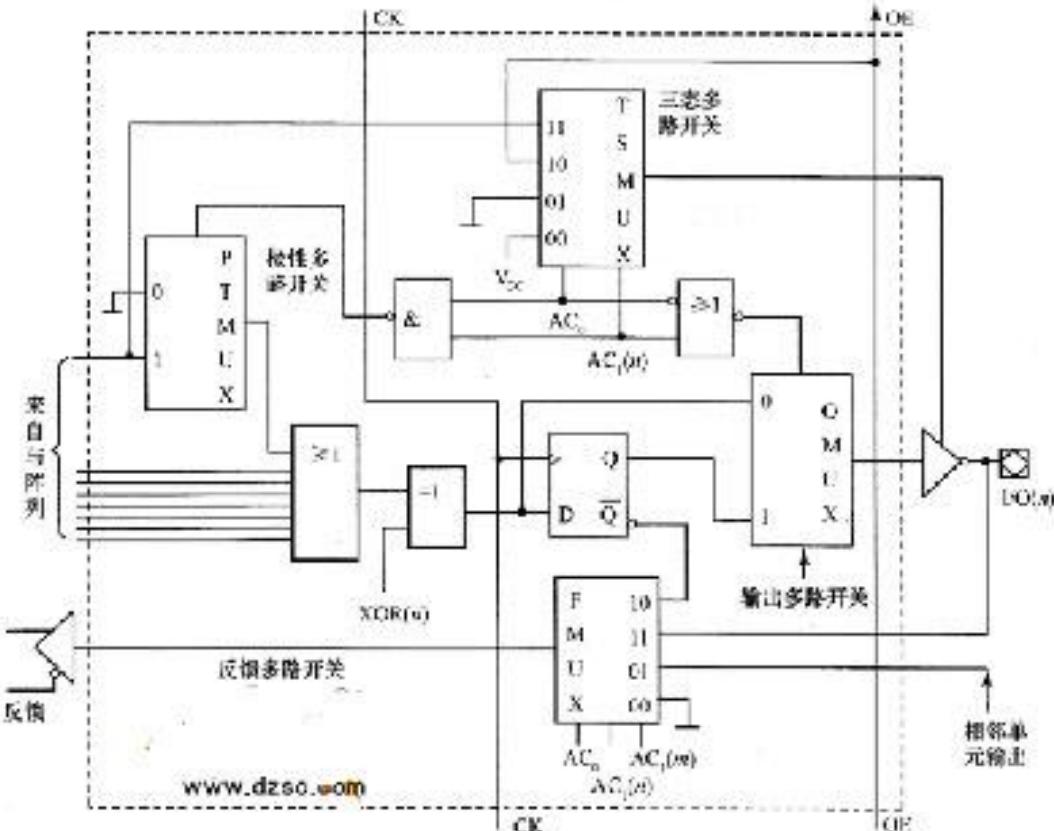
The programmable elements (shown as a fuse) connect both the true and complemented inputs to the AND gates. These AND gates, also known as *product terms*, are ORed together to form a *sum-of-products* logic array.



PLA



GAL



Output Logic Micro Cell

Lattice Semiconductor



Type	Public (NASDAQ: LSCC [1])
Industry	Integrated Circuits
Founded	1983, public since 1989
Headquarters	Hillsboro, Oregon, United States
	45.527216° N
	122.926626° W
Key people	Darin Billerbeck, CEO
Products	FPGAs, CPLDs
Revenue	\$332.5 million (2013) [1]
Net income	▲ \$22.3 million (2013) [1]
Number of employees	700 (2011) [2]
Website	www.latticesemi.com [3]

Virtex 5

- 65nm

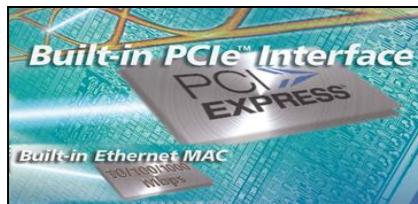
终极系统
集成平台



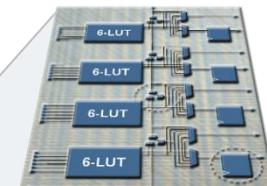
Advanced Programmable System



36Kbit Dual-Port Block RAM / FIFO
with ECC
Higher Bandwidth



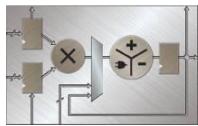
FPGA Industry's First Built-in PCIe & Ethernet Blocks
Protocol Support



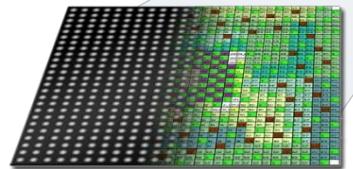
ExpressFabric™
Real 6-input LUT, Up to 330,000 Logic Cells
30% Higher Performance



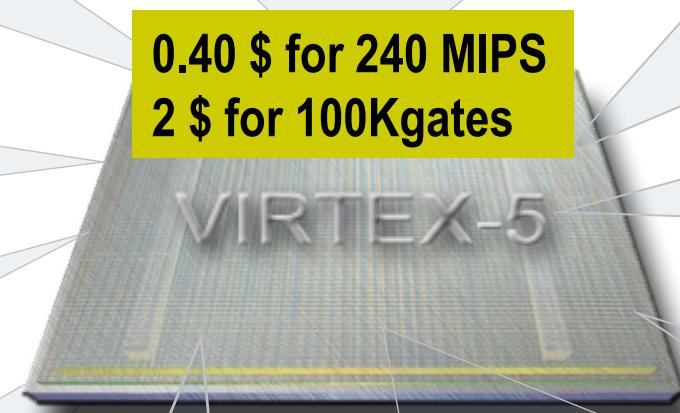
3.2 Gbps Serial Transceivers
Lowest Power



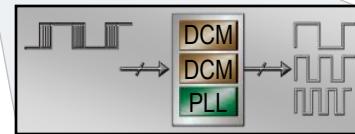
25x18 DSP Slice
Higher Precision



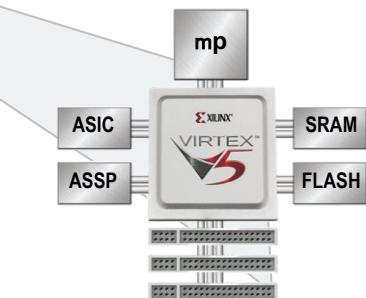
2nd Generation Sparse Chevron
Superior Signal Integrity



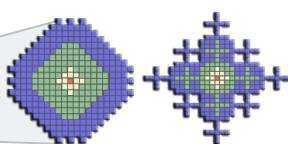
Second Generation Triple-oxide,
Advanced 65nm Process,
1 Volt Core, Strained Silicon
Low Power



550 MHz Clock Management DCM
(precision synthesis)
+ PLL (Low jitter)



3.3V SelectIO with ChipSync
1.25 Gbps LVDS,
800 Mbps Single-Ended



Virtex-5 Virtex-4
ExpressFabric™
New Interconnect Architecture
Enhanced Routing

Spartan Devices Optimized for High-Volume Applications

Addresses the cost and flexibility requirements in Edge applications



Imagine...

FPGA-based System-in-Package

Specialized Layers of

DSP fabric,
Memory fabric,
FPGA fabric, ...

Optimized for Technology

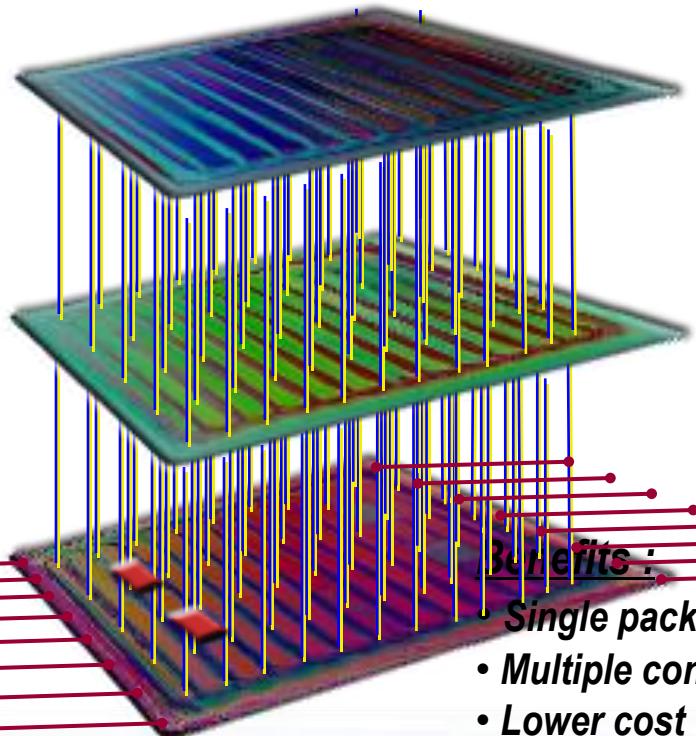
130nm,
90nm,
32nm, ...

With 3D Interconnect

And at its heart...

An FPGA SoC with:

- Embedded Processing
- Embedded DSP
- High-speed Serial Connectivity
- Reprogrammable FPGA Logic Fabric as the Base



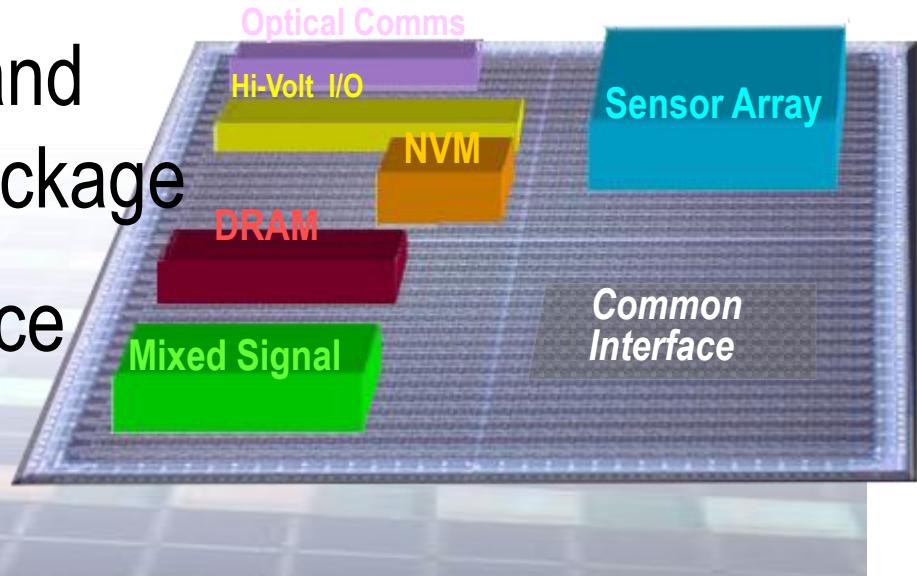
Benefits :

Single package of heterogeneous die

- Multiple configurations of standard products
- Lower cost
- Lower power
- **Ultimate customization**
- **Ultimate flexibility**

“Motherboard” for Mixed Technology in a Package

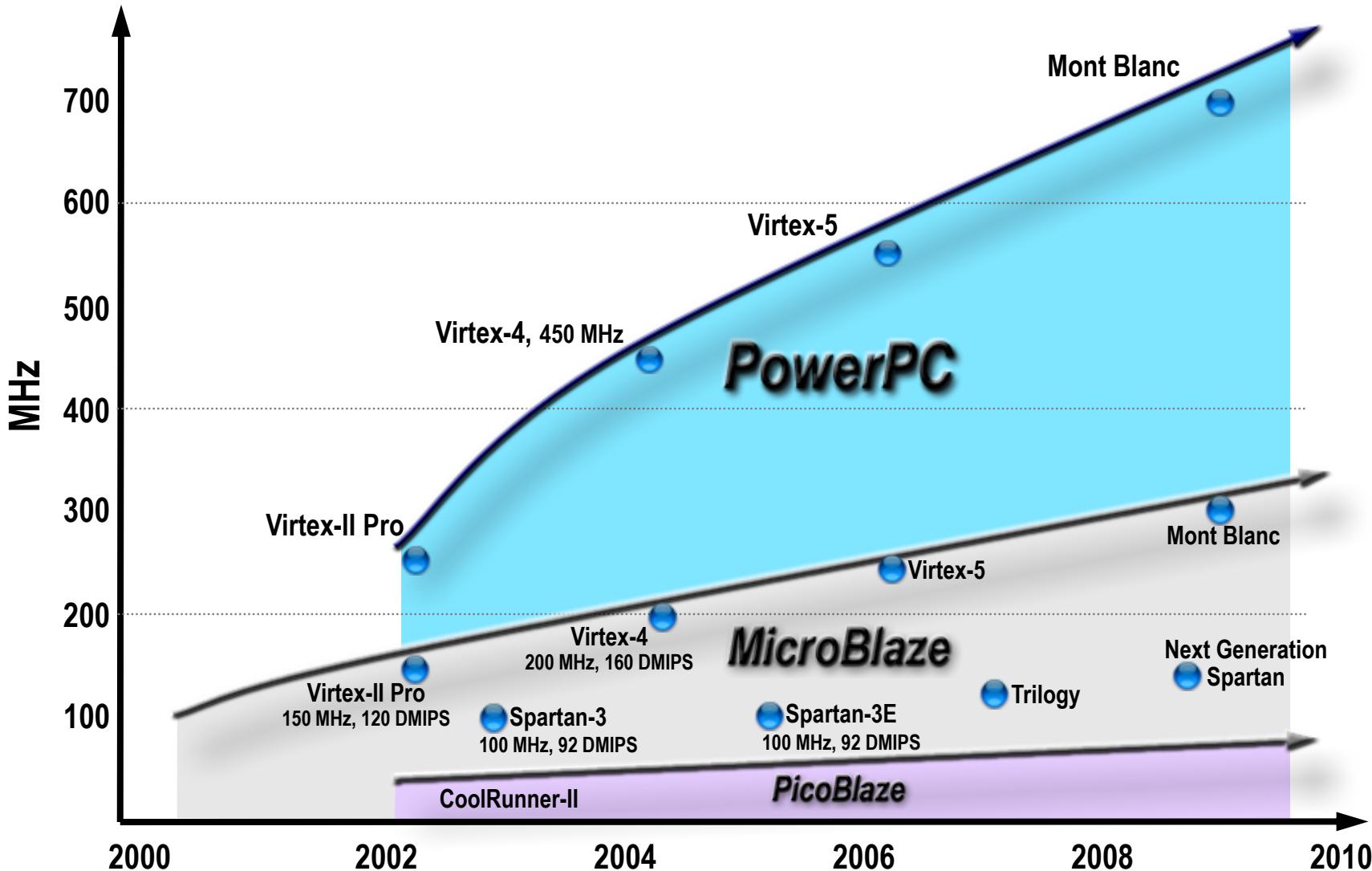
- Alternative to big die with hardened IP “Virtual SoC”
- Enables mixed-process and mixed-voltage die in a package
- Common bumped interface for 3rd parties



“New packaging options enable the decoupling of the overlying architecture from the underlying process technology, allowing the use of the best process for a given feature, e.g. memory, logic, transceivers, and processors.”

- Suresh Menon, VP, FPGA Products

Broad Range of Price/Performance



PowerPC

- Hard core
- Open hardware license from Power.org if migrate to ASIC
- Up to 4 core
- Up to 500MHz
- Standard OS support: Vxwork, Linux, BSD

Microblaze: 32 bit soft core

MicroBlaze



uClinux

Embedded Linux/Microcontroller Project

[Home](#)

[What is uClinux?](#)

[Status](#)

[Getting started with uClinux](#)

[FAQ](#)

[uCsimm Hardware Project](#)

uClinux has successfully been ported to the Cisco 2500, 3000, 4000 routers. The patch allowing uClinux to run on the Cisco 2500/3000/4000 routers was completed by Koen De Vleeschauwer. The picture on the left is of a CISCO 3000 running uClinux at Arcturus Networks' Toronto office. The picture was taken by an AXIS 2100 web camera (also running uClinux).

uClinux is the leader in portability. The wide range of Open Source ports is proof of this. Community members from all over the world have been porting uClinux since its release in 1998. While originally developed for the Motorola 68000 chip, the number of available ports is always expanding. If your port is not listed here, or your commercial product using uClinux is not listed, drop us a note at info@uclinux.org.

• uClinux on the Microblaze

Microblaze is a highly-parameterized 32 bit RISC soft-core processor targetted for Xilinx FPGAs. The ability to customise the processor (e.g. hardware architecture, instruction set, memory, flexible bus architecture) creates both opportunities and challenges for Linux kernel configuration.

The uClinux port to Microblaze was done by Dr John Williams in the Embedded Systems group at the University of Queensland in Brisbane, Australia, and is part of their reconfigurable computing research program. The project home page is <http://www.itee.uq.edu.au/~jwilliams/mblaze-uclinux>. More information on the Microblaze can be found at <http://www.xilinx.com/edk>.



Picoblaze

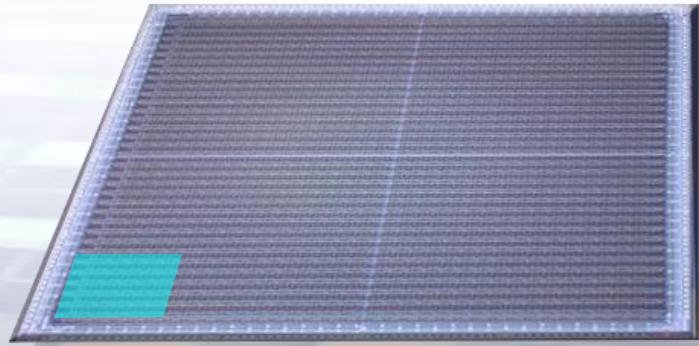
- 8 bit Microcontroller
- Soft core
- Source code available
- Tiny size, can fit into CPLD



Low Cost of Embedded Processing

<u>2006</u>		<u>2010</u>
\$0.4	32-bit MicroBlaze soft processor	\$0.0
0	8-bit PicoBlaze soft processor	5
\$0.0		\$0.0

8



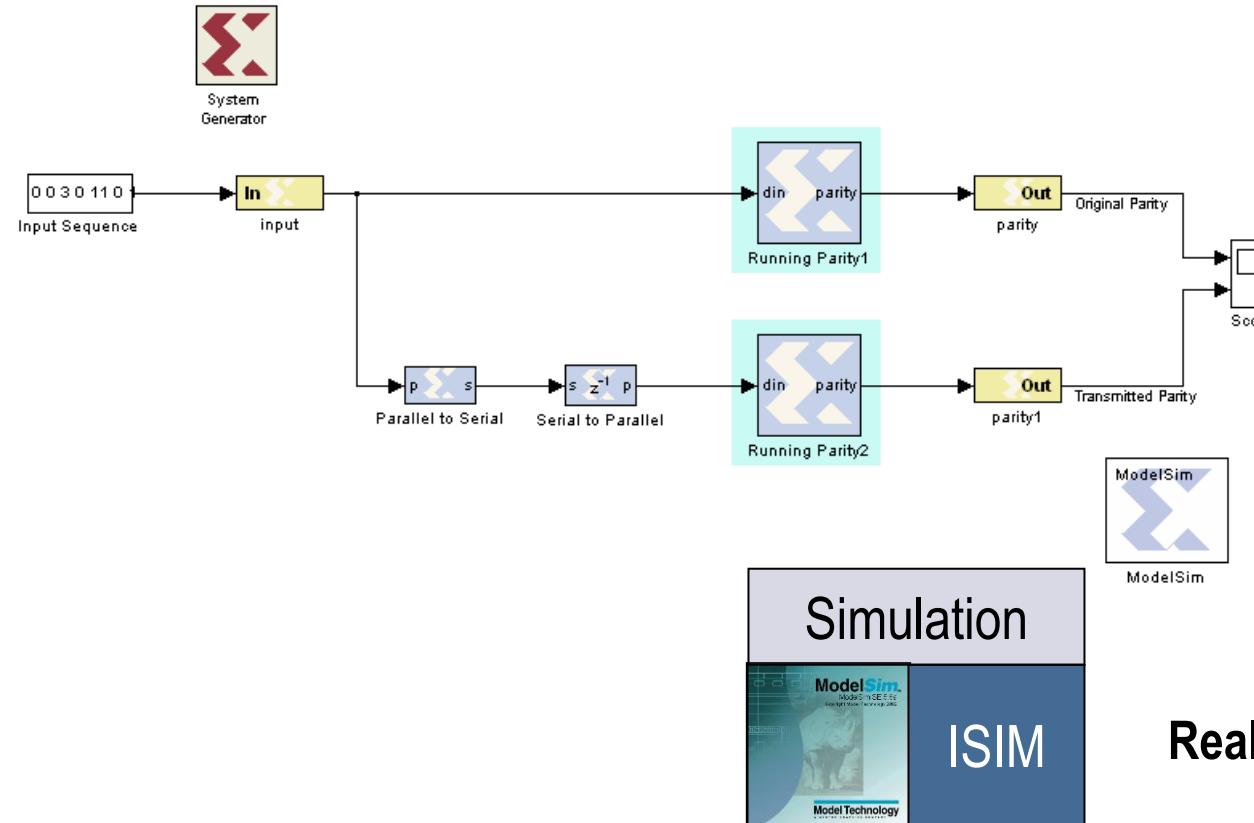
1



MicroBlaze on Spartan-3E XC3S1200E*

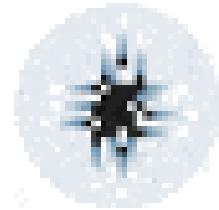
* Approx. 4.5% of Spartan-3E XC3S1200E FPGA, Pricing is for 500K units at end of 2006

Matlab/Simulink XILINX DSP design flow



Real-Time Verification

AccelDSP

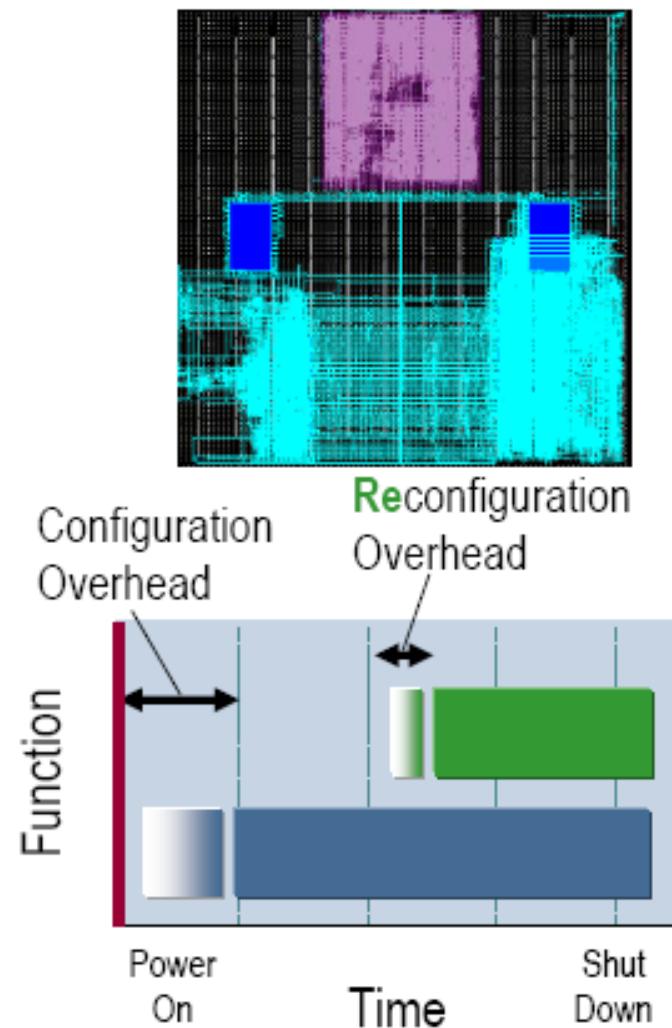


XILINX
AccelDSP™
SYNTHESIS TOOL

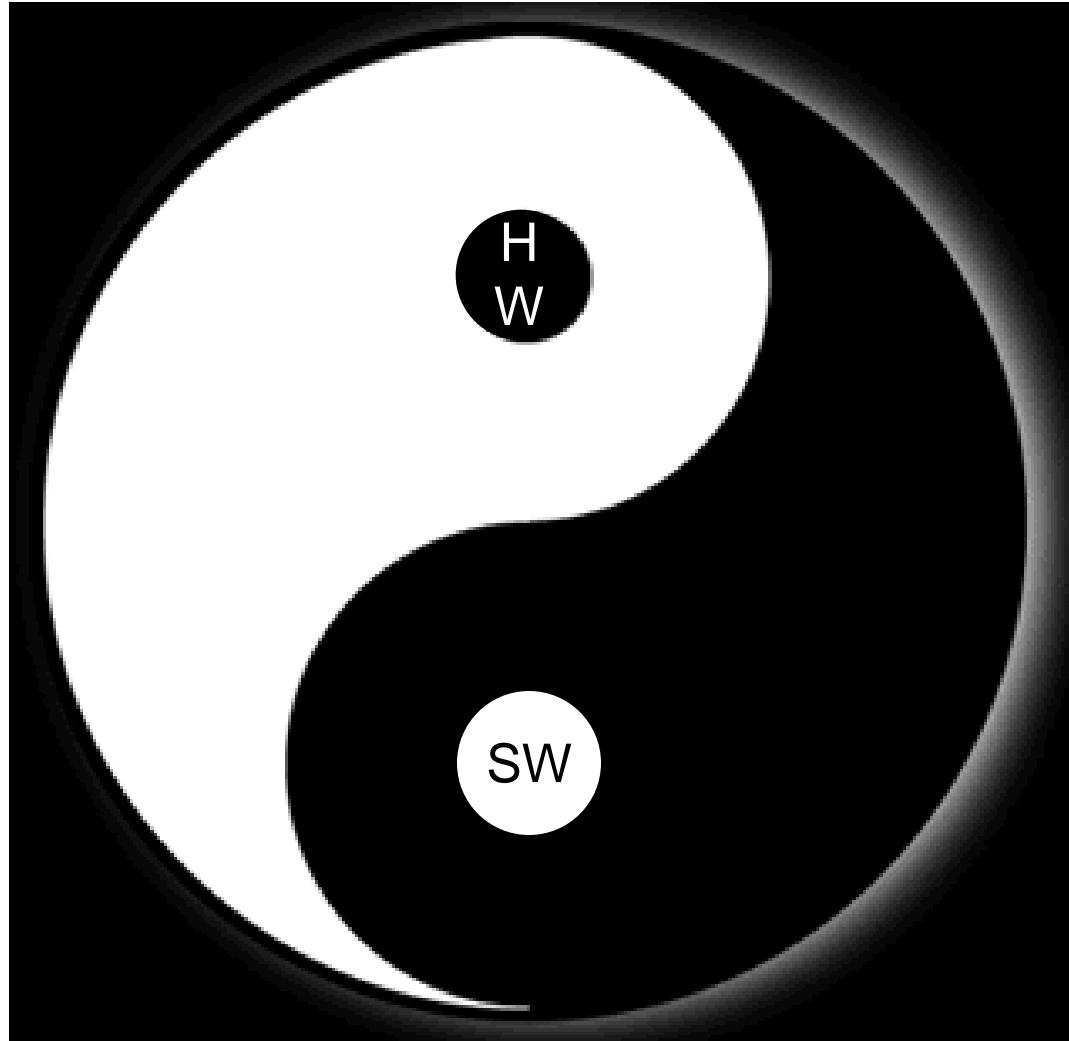
- AccelDSP™ 综合工具是基于高级 MATLAB 语言的工具，用于设计针对 Xilinx FPGA 的 DSP 块。工具可自动地进行浮点-定点转换，生成可综合的 VHDL 或 Verilog，并创建用于验证的测试平台。您还可以生成定点 C++ 模型或由 MATLAB 算法得到 System Generator 块。AccelDSP 综合工具是 Xilinx XtremeDSP™ 解决方案的关键组成，集成了先进的 FPGA、设计工具、IP 核、合作伙伴以及设计与教育培训服务等。

Dynamic Partial Reconfiguration

- A subset of the configuration data changes...
 - But logic layer continues operating while configuration layer is modified...
 - Configuration overhead limited to circuit that is changing...



TAO



OpenHW

- 组建XILINX实践小组：
- 在OpenHW上注册：
 - 西安电子科技大学软件学院-？？？
 - 以3-5人为一组
 - 了解设计流程、工作模式
 - 了解可用资源
 - 提出新的设想
 - 申请资助

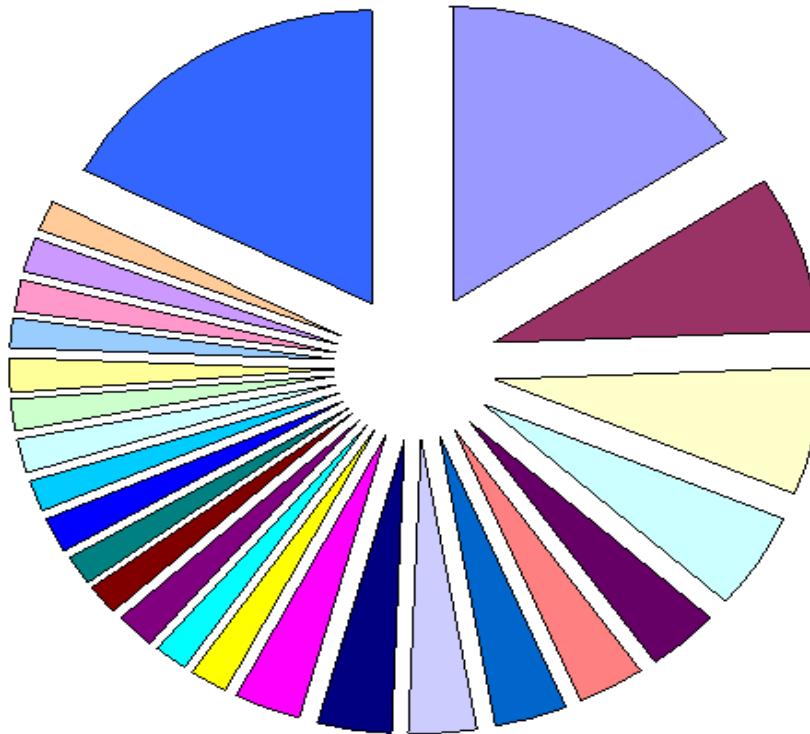


History of Open Source Hardware

- 1998年， Delft University of Technology, Open Design Circuits Group
 - Opencores 和 OpenIPcore.
 - 2000 年 OpenIPcore 合并入Opencores
 - Jamil Khatib是Opencores中教父级人物
-
- 2007 Opencore status:
 - 6 mailing lists
 - 400 projects
 - 7.5M web hits/month
-
- 商业公司SUN, IBM 相继开放源码
 - 各大学的零星开放源码硬件项目

Opencores.org

**80,000 engineers and others visit OpenCores monthly -
Regional breakdown**



- US
- India
- China
- Bahrain
- Iran
- Greece
- Hong Kong
- Germany
- Israel
- Tunisia
- Canada
- Chile
- Kuwait
- Singapore
- Turkey
- Denmark
- Algeria
- France
- Portugal
- Argentina
- Switzerland
- Colombia
- Finland
- United Kingdom
- Other Countries

Vote results

Which HDL you prefer? - opened

Verilog HDL



VHDL



Both are Ok



Different one



Openhard.org

- The first open source hardware website in Chinese
- Created by a student from Xilinx Student Club in XJTU
- Sponsored by Xilinx University Program
- OpenHW.org OpenHW.com OpenHW.net



欢迎您访问OpenHard开源社区！

Eiki电子百科

请输入搜索关键字

搜 索

用户登录

用户名：密 码： 记住我的用户名

登 录

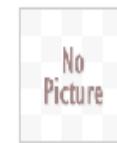
[注册](#) | [忘记密码](#)

赞助商信息

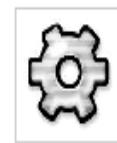


当前位置>>团队

推荐团队

[SuperEDS](#)

该团队致力于嵌入式网络系统的开发与研究,由...

[Thinking Studio](#)

我们来自南京邮电大学,对FPGA有浓厚兴趣,...

[星森 \(天津工业大学Xi...](#)

天津工业大学Xilinx俱乐部成员。

[WUST--Xilinx Team](#)

武汉科技大学嵌入式系统实验室

[Xilinx Stu.Club Of X...](#)

西安赛灵思俱乐部

最新团队

[西电FPGA俱乐部609](#)

本团队精通FPGA的研发,团队成员都是西安电...

[jepq2000的FPGA实现](#)

本团队长期从事FPGA设计于研发。经验丰富。...

推荐团队文章

[开放源码硬件License初探...](#)[IEEE 1588是什么?](#)[以太网的时钟同步](#)[一种基于Xilinx V2Pro的...](#)[用java实现如何删除含有...](#)[8086FPGA核跑吃豆子游戏...](#)[XILINX新MICROBLAZE 软处...](#)[远航的起点](#)[看一下S3C4510内部MAC通...](#)[Spantan-3E的网络应用](#)

more.....

最新团队文章

[IEEE 1588是什么?](#)[8086FPGA核跑吃豆子游戏...](#)

Events will be written in History

- 2006年9月29日， 西安交通大学建立Xilinx学生俱乐部主席王飞成功注册了www.openhard.org 域名。
- 2007年6月， OpenHard改版，以Web2.0方式创建中文开放源码硬件社区，面向广大学生和学术机构，骨干为各地的Xilinx学生俱乐部成员，并在中国发起首届开放源码硬件大赛。
- 2007年6月22日， OpenHard 迎来了首个学生团队，武汉科技大学闵华松教授带队的嵌入式系统实验室，并创建了第一个项目：基于以太网的嵌入式数据采集系统。

XUP introduction

- XILINX University Program
- Start from 1985
- 3000 university registered
- Almost all key U.S. universities using XILINX technology
- In U.S. and European universities, FPGA = XILINX

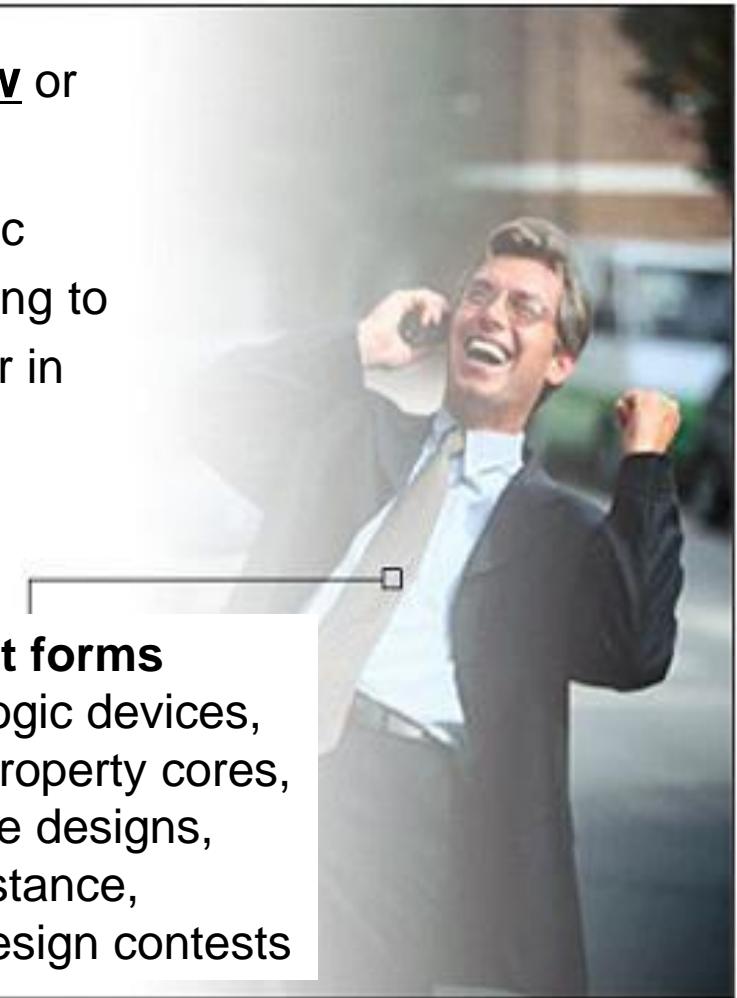


XUP donation policy

Whenever a new project, such as a new or improved course or research program, requires best-in-class programmable logic devices and design software, XUP is willing to consider requests to assist the Professor in establishing the new project

Donations take many different forms

CAD software, programmable logic devices, workshop training, intellectual property cores, development systems, reference designs, training material, technical assistance, conference participation, and design contests



Xilinx technologies in education

- Digital design
- Computer networking
- Digital communications
- Computer Architecture
- Control Systems
- Parallel processing
- Neural networks
- Evolvable systems
- Reconfigurable computing
- System on chip
- Error detection and correction
- Embedded processing
- Real-time systems
- LINUX for embedded systems
- Cryptography
- Compression/decompression
- Industrial control
- Digital signal processing
- Video processing
- Genomics
- Hardware software co-design
- Robotics

Range of XUP boards

Virtex-II Pro
399\$ (China)



For advanced courses : DSP, Embedded projects & research

Spartan-3E
149\$



For Linux/networked processor courses

NEXYS
99\$



For logic/processor courses

BASYS
59\$



For introductory logic courses

BASYS:Empowering personal innovation at the student level

US\$59.99



- Cheaper, smaller, and lighter than the average engineering textbook
- 100,000 gates for US\$59.99
- Combines a 100K-gate Xilinx Spartan3-E with free Xilinx WebPack™ software to give a full digital design environment

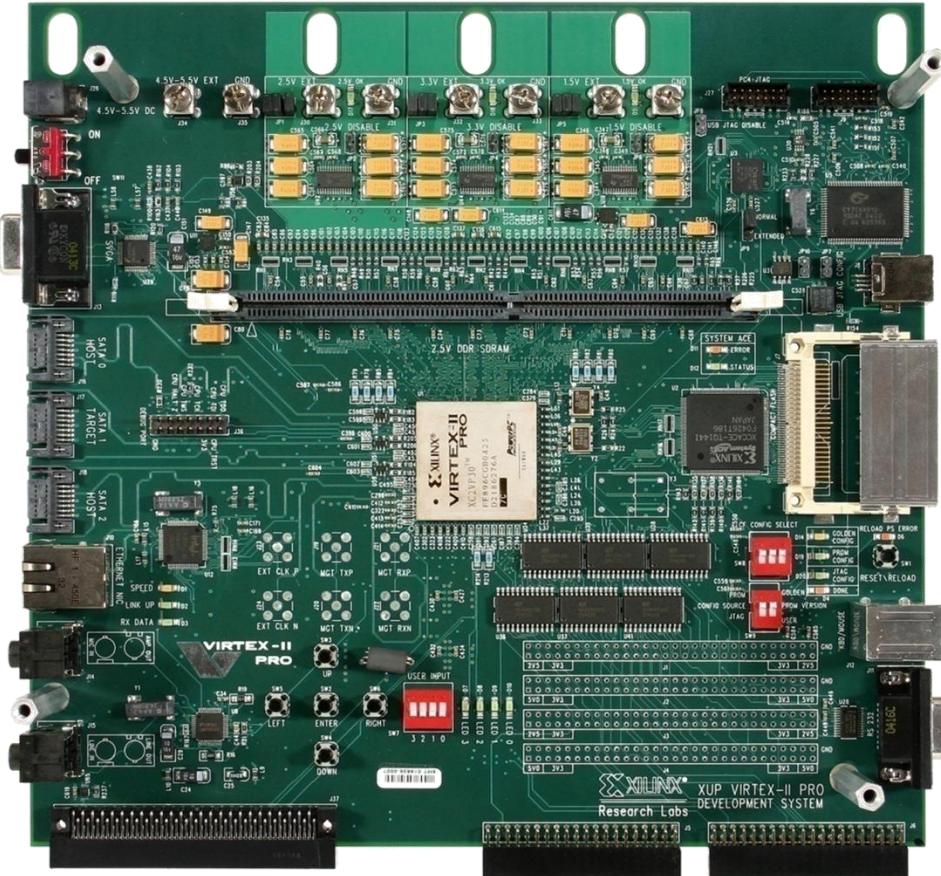
XUP Spartan 3E System: US\$149



- Key Features
- On-board USB
- Built-in self test
- Ethernet PHY
- VDEC board interface
- Reference designs

Virtex-II Pro Development System: Curriculum-on-a-Chip™

University Price \$399(China,to Door)



A powerful, versatile,
low-cost
development system
for education

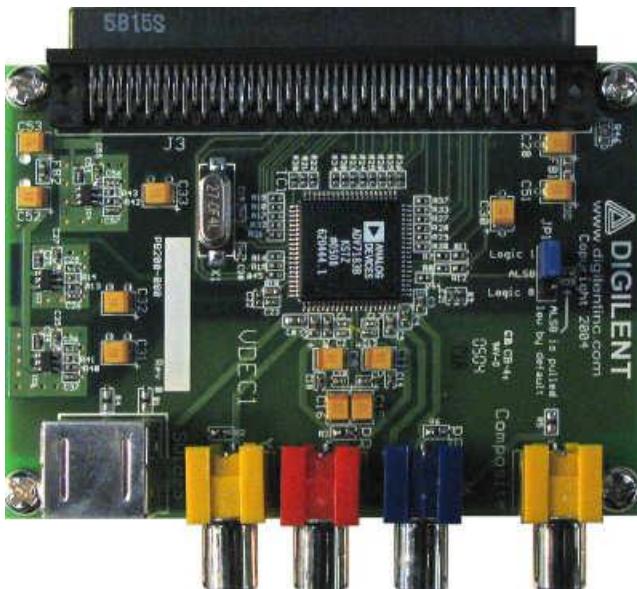
developed with ISE,
EDK and DSP teams
and academic partners

Industrial Price:\$1599

Virtex-II Pro Development System

- Powerful: Virtex-II Pro XC2VP30 FPGA
 - 30,816 Logic Cells , 2 PowerPC 405 processors, 8 multi gigabit transceivers (4 available on board), 2448 Kbits of Block RAM, 136 18x18 multipliers
- Versatile
 - Teaching and research
 - Digital design, computer architecture, operating systems, networking, embedded systems, digital signal processing, image & video processing, digital communications, and more
- Low-cost
 - With donation of 4 on-board Xilinx devices

Auxiliary Video Decoder Board (VDEC1)



- Component, composite, and S-video inputs
- I²C® compatible control bus
- High-speed Hirose FX2 data connector
- Supports NTSC, PAL, and SECAM inputs
- 8-bit or 16-bit YCrCb 4:2:2 outputs
plus HS, VS and Field signals
- Programmable controls include peak white,
hue, brightness, saturation and contrast

Designed in partnership with academia

BYU Brigham Young University

Department of Electrical and Computer Engineering

Computer Systems Senior Project

Winter 2005

Dr. Michael J. Wirthlin

MPEG-2 System on a Chip

Students participating in this senior project created a network-enabled MPEG-2 video and MP3 audio player on a single FPGA device using the Xilinx ML-XUP Pro board and EDK development tools. This multi-disciplinary project involved the design of a complete computer system and integration of the following skills:

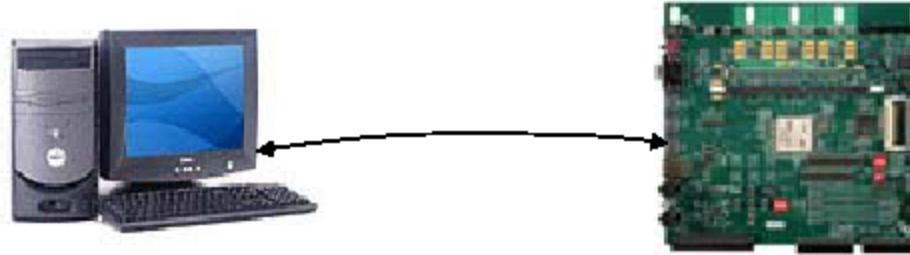
- Computer Architecture
- Network Interfacing
- Real-Time Operating Systems
- Digital Design/VHDL
- Video Decoding
- MP3 Decoding



Xilinx ML-XUP Pro

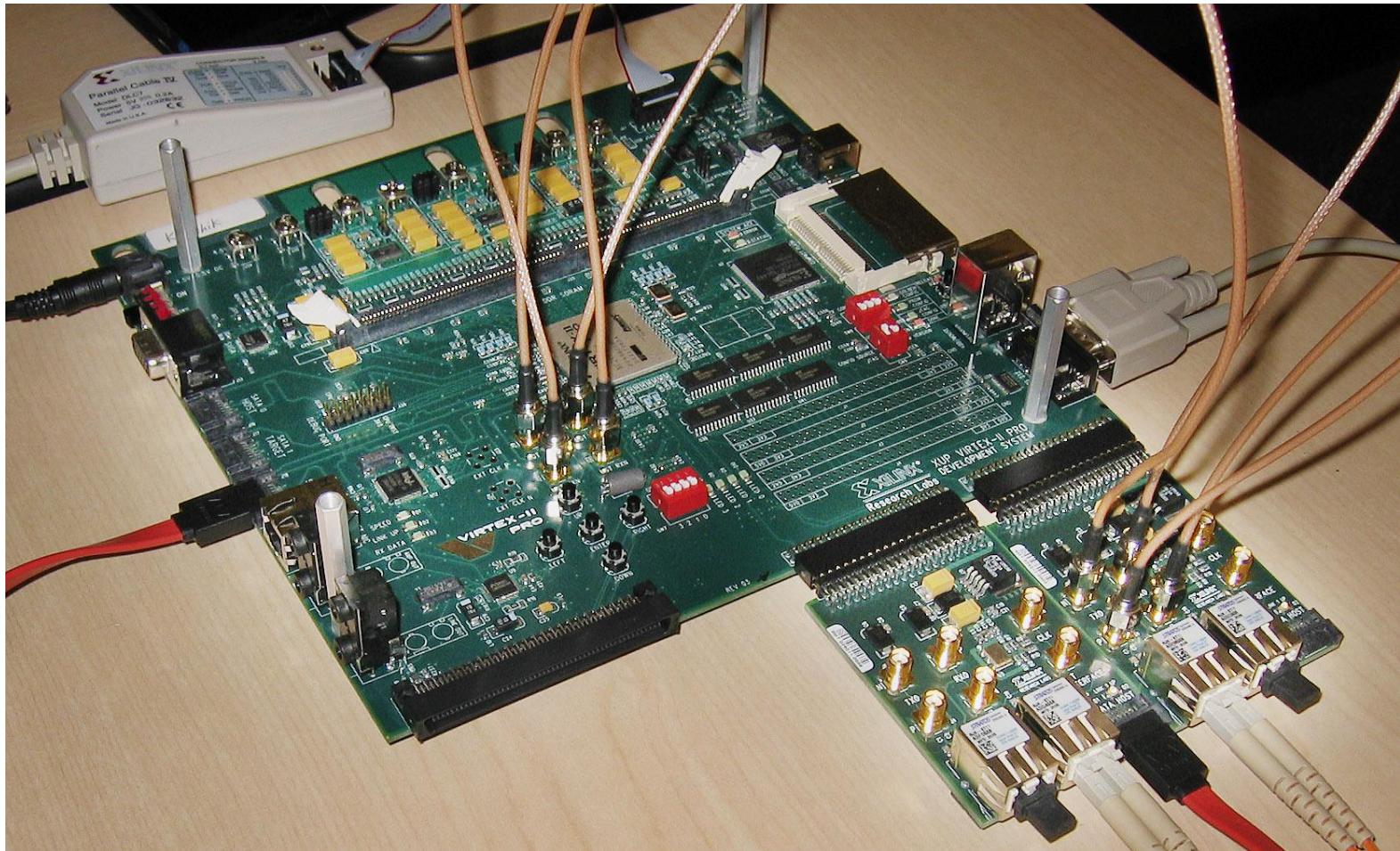
Stanford EE109: networked imaging

Lab 1—Ethernet Loopback



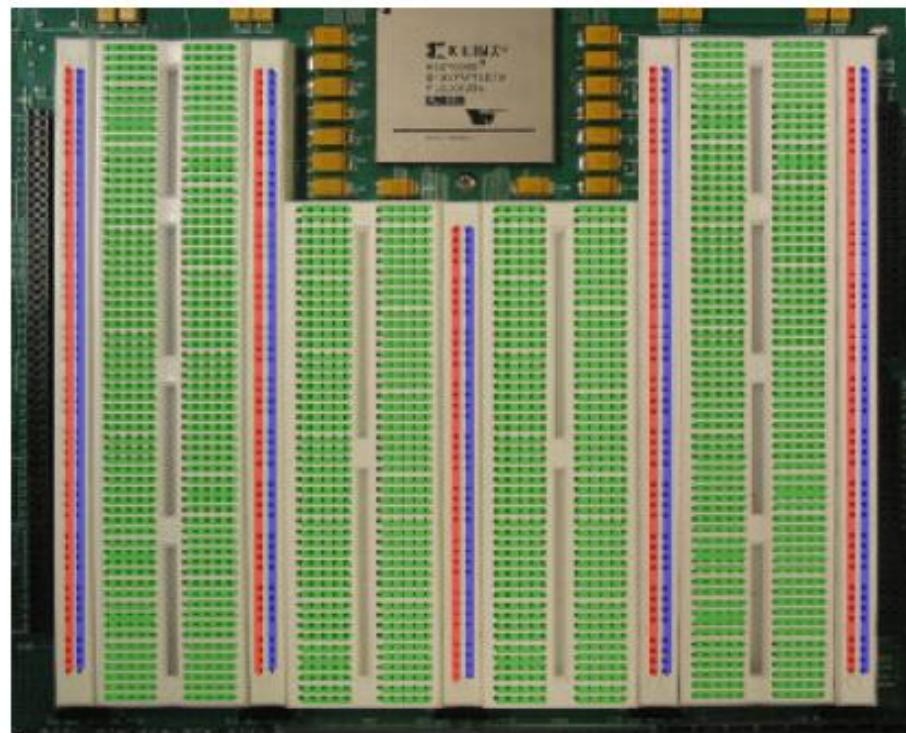
- Implement the Xilinx Tri-Mode Ethernet MAC example loopback device.
 - Receives packets, swaps the source and destination addresses, and transmits them.

Quad gigabit serial optical ports



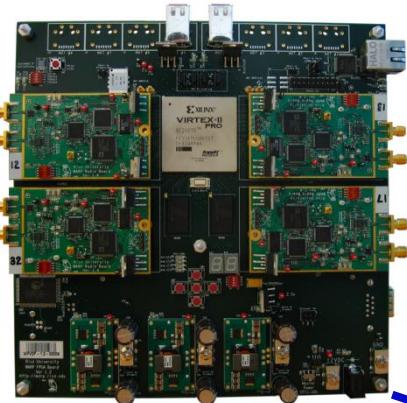
MIT Labkit

- <http://www-mtl.mit.edu/Courses/6.111/labkit/>



Rice University WARP Program

Hardware



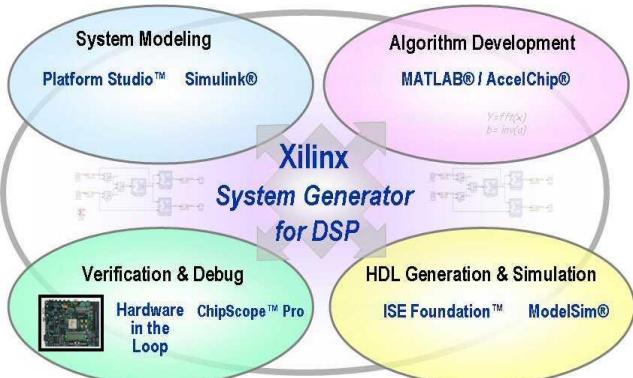
- Next generation of Hardware Kits
- New level of sophistication
 - RF capability
- Fully functional reference designs



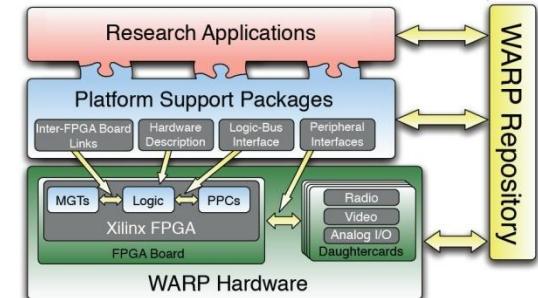
Software



- Top-down derived and completely data derived libraries
- Designed from the ground-up with major considerations for system composition
- Delivered in System Generator

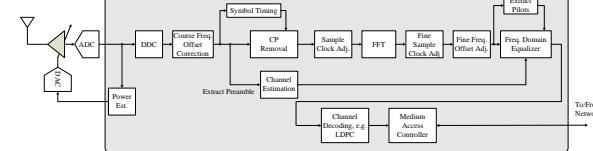


Grow User Community



- Open access repository

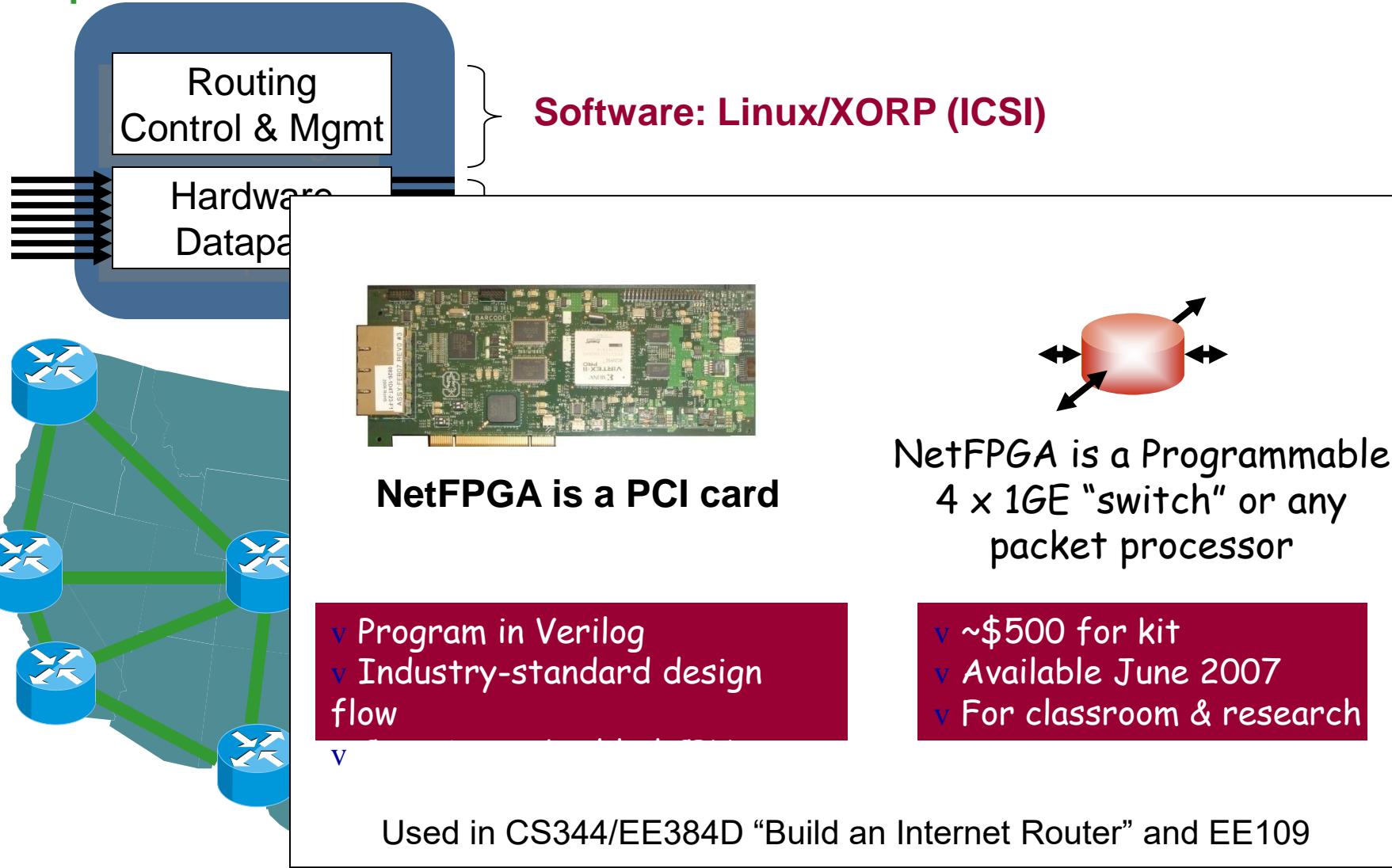
Reference Designs



- System Generator/AccelDSP reference implementations
- In-system validated

Stanford : NetFPGA Program

Open Source “Router Kit”

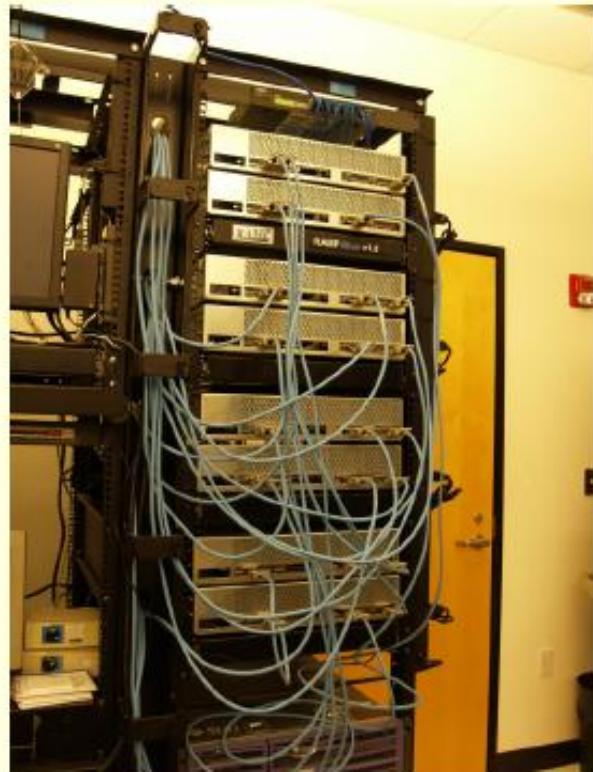


UCBerkeley RAMP program

Large-Scale

- Class 1 M
 - Supercomputer
 - $\sim 10\text{-}10^5$ ips
- Class 2 M
 - Hybrid network
 - FPGA acceleration
 - Programming
- Class 3 M
 - Network
 - Our focus

Next Generation



BEE2 Platform : <http://bee2.eecs.berkeley.edu/>

BEE: Berkeley Emulation Engine

Research Accelerator for Multiple Processors

Feb. 21, 2007

XAF 2007

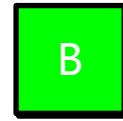
39

可以访问么？

BEE2 Platform : <http://bee2.eecs.berkeley.edu/>



Yes.



No.

提交

XILINX®



< 收藏 手机收藏夹 谷歌 网址大全 360搜索 游戏中心

Images

Videos

MSN

Office

Outlook.com



国内版

国际版



国内版

国际版

http://bee2.eecs.berkeley.edu/



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Any time ▾

BEE2 - casper.ssl.berkeley.edu

<https://casper.ssl.berkeley.edu/wiki/BEE2> ▾

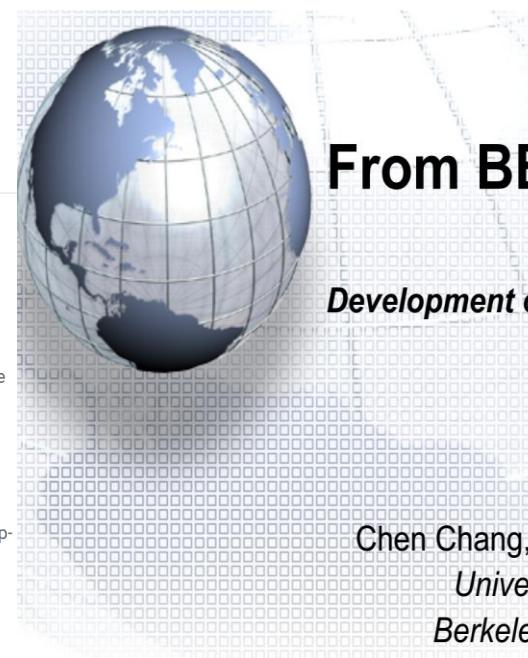
The BEE2 is a general-purpose processing module based on five high-performance Xilinx FPGAs (Virtex-II Pro 2VP70). In addition to the large amount of processing fabric provided by the FPGAs, the BEE2 also provides up to 20GB of high-speed, DDR2 DRAM memory.

EECS at UC Berkeley

<https://eecs.berkeley.edu/> ▾

Welcome to the Department of Electrical Engineering and Computer Sciences at UC Berkeley. Our top-ranked programs attract stellar students and professors from around the world, who pioneer the frontiers of information science and technology with broad impact on society.

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From BEE to BEE2

Development of Supercomputer-in-a-Box

Chen Chang, John Wawrzynek, Bob Brodersen
University of California, Berkeley
Berkeley Wireless Research Center



RAMP

Table 1: List of Industry Supporters

Name	Affiliation	Areas of Expertise
Gordon Bell	Microsoft	computer architecture
Ivo Bolsens	Xilinx, CTO	DSP, EDA
Norm Jouppi	HP Labs	computer architecture
Shih-Lien Lu	Intel	computer architecture
Craig Mundie	Microsoft CTO	software
Greg Papadopoulos	SUN, CTO	parallel processing, computer architecture
Justin Rattner	Intel, CTO	parallel processors, computer architecture
Ivan Sutherland	Sun	graphics, computer design
Chuck Thacker	Microsoft	hardware, computer design
Kees Vissers	Xilinx	embedded Computing

Table 2: List of Academic Supporters

Name	Affiliation	Areas of Expertise
Doug Burger	UT Austin	computer architecture, system implementation, simulation
Bill Dally	Stanford	computer architecture
Carl Ebeling	U Washington	computer architecture
Susan Eggers	U Washington	parallel computers, compilers, architecture
Steve Keckler	UT Austin	computer architecture
Bill Kramer	NERSC/LBL	Head, high-performance Computing
Greg Morrisett	Harvard Univ	programming languages, compilers, security
Scott Shenker	UC Berkeley	networking
Ion Stoica	UC Berkeley	networking
Kathy Yelick	UC Berkeley	parallel languages, compilers, algorithms

Professor workshop

- More than workshops, roadmap makes professor successful
- List increasing
 - Digital Design with FPGAs
 - Digital Communications with FPGAs
 - Digital Signal Processing with FPGAs
 - DSP for FPGA Primer
 - Embedded Design with FPGAs
 - Embedded Linux for the Xilinx Microblaze



IWMS.NET

Joining the Xilinx University Program

- www.xilinx-china.com/univ

The screenshot shows a Microsoft Internet Explorer window displaying the Xilinx University Program website. The address bar shows the URL <http://www.xilinx-china.com/univ/>. The page features the Xilinx logo and navigation links for '主页', '技术解决方案', '产品与服务' (highlighted in red), '市场解决方案', '技术支持', and '采购信息'. A search bar at the top right includes fields for '输入关键字/型号#' and '产品/服务' with a dropdown arrow, and a '高级搜索' button. Below the search bar, there's a banner with images related to engineering and technology. The main content area is titled 'Xilinx大学计划' and includes a circular seal with 'XILINX UNIVERSITY PROGRAM' and a graduation cap icon. It welcomes visitors to the community of over 1,800 universities using Xilinx systems. A '教授' (Professor) section highlights the mission of university faculty to contribute to the future labor force and provides links to donation plans, teaching materials, professor forums, and technical support. A '学生' (Student) section discusses how students can use Xilinx tools in classrooms and research projects. The bottom of the page shows the Windows taskbar with icons for Start, 2006DSP, Microsoft Power..., and the current Internet browser window.

Asia Pacific Technology Fund

- \$75M fund
- Objectives
 - To nurture emerging, complementary products & technologies developed in ASIA Pacific.
 - To promote FPGA innovation in Asia Pacific with local content.
 - To develop new markets or expand existing markets.
 - Technical and market information exchange



The slide features the Xilinx logo at the top left, consisting of a stylized red 'X' followed by the word 'XILINX' in a grey sans-serif font with a registered trademark symbol. Below the logo is a dark red banner containing the text '\$75,000,000 USD Asia Pacific Technology Fund'. The main body of the slide is light blue and contains the following text:

Investing in innovative companies that will expand the PLD business directly or indirectly through development of leading edge, innovative, unique products or technology.

A horizontal collage of images illustrating various applications of technology. From left to right, it shows a person wearing a white lab coat and safety goggles looking at a circuit board; a computer monitor displaying a 3D map or simulation; a complex metal lattice structure, possibly a bridge or antenna; a car driving on a road; and two small portrait photos of smiling individuals.

XUP is more than donation

IEII(inspiration, enabling, innovation, incubation).

Inspiration:

Workshops, books, etc.

Enabling:

Joint lab, books, boards, etch

Innovation:

Open source hardware, contest, Open source IP

Incubation:

Joint project, etc.

Xilinx公司有很多集成的开发软件， 主要包括以下几部分：

ISE	Xilinx公司集成开发环境
Foundation	Xilinx公司早期的开发工具，已经逐步被ISE取代
ISE Webpack	Xilinx提供的免费开发软件，功能比ISE少一些，可以从Xilinx网站下载
EDK	嵌入式开发套件，用于开发集成PowerPC硬核和Microblaze软核CPU的工具
System Generator	配合Matlab，快速在FPGA中实现数字信号处理功能
Xilinx IPCore	Xilinx公司预编译好的可配置功能模块，性能好，可视化用户界面



Quick Start

[Create Project >](#)[Open Project >](#)[Open Example Project >](#)

Tasks

[Manage IP >](#)[Open Hardware Manager >](#)[Xilinx Tcl Store >](#)

Learning Center

[Documentation and Tutorials >](#)[Quick Take Videos >](#)[Release Notes Guide >](#)

New Project

Project Type

Specify the type of project to create.

RTL Project

You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.

Do not specify sources at this time

I/O Planning Project

Do not specify design sources. You will be able to view part/package resources.

Imported Project

Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project

Create a new Vivado project from a predefined template.



Finish

Cancel

< Back

Next >

20:16
2020/2/12

Flow Navigator

PROJECT MANAGER

Settings

Add Sources

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

> Open Elaborated Design

SYNTHESIS

Run Synthesis

> Open Synthesized Design

IMPLEMENTATION

Run Implementation

> Open Implemented Design

PROJECT MANAGER - project_1

Sources



Design Sources

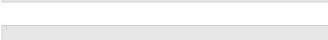
> Constraints

> Simulation Sources

sim_1

> Utility Sources

Properties



Select an object to see properties

Project Summary

Overview | Dashboard

Settings Edit

Project name: project_1

Project location: D:/xilinx-experiments/project_1

Product family: Virtex-7

Project part: xc7vx485tffg1157-1

Top module name: Not defined

Target language: VHDL

Simulator language: VHDL

Synthesis

Implementation

Status: Not started

Status: Not started

Messages: No errors or warnings

Messages: No errors or warnings

Part: xc7vx485tffg1157-1

Part: xc7vx485tffg1157-1

Strategy: Vivado Synthesis Defaults

Strategy: Vivado Implementation Defaults

Report Strategy: Vivado Synthesis Default Reports

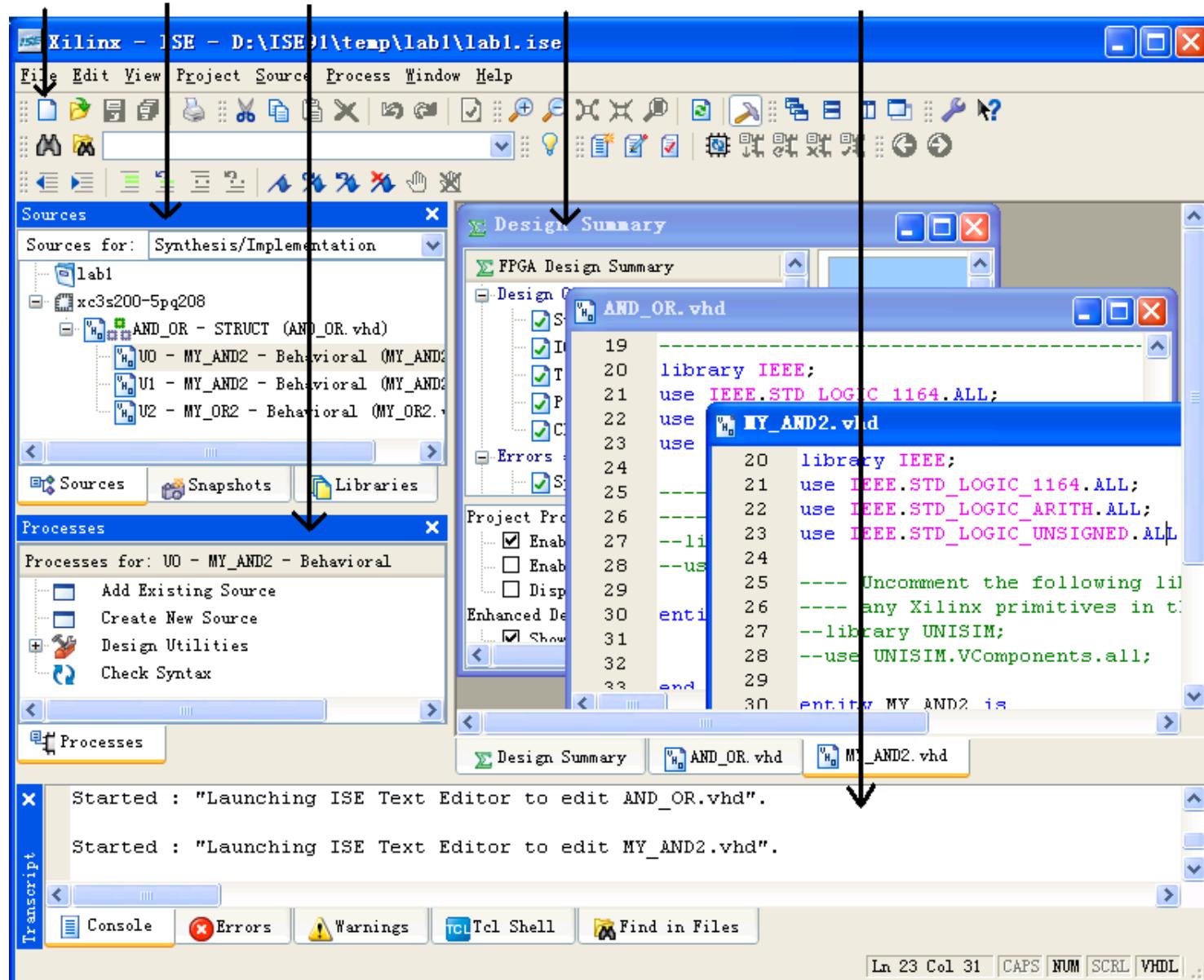
Report Strategy: Vivado Implementation Default Reports

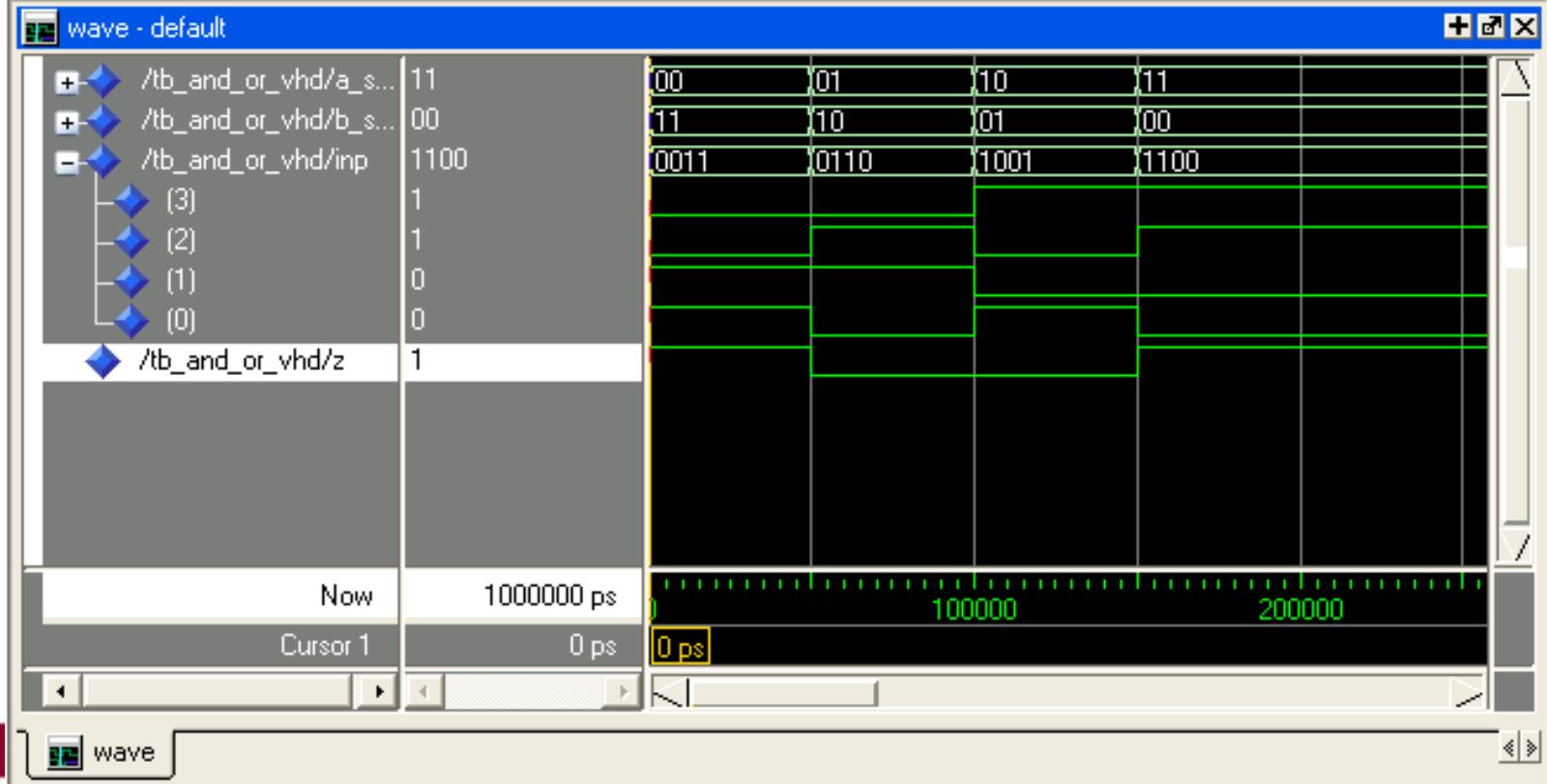
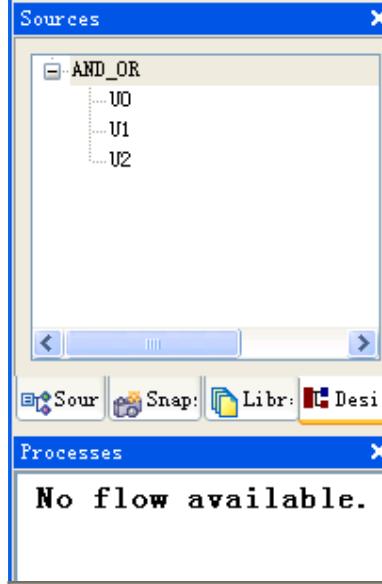
Tcl Console Messages Log Reports Design Runs

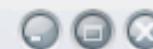


Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	R
synth_1	constrs_1	Not started															V
impl_1	constrs_1	Not started															V









Please select an action from the list below

Configure devices using Boundary-Scan (JTAG)

Automatically connect to a cable and identify Boundary-Scan chain

Prepare a PROM File

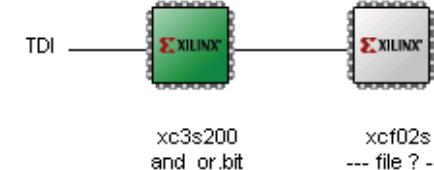
Prepare a System ACE File

Prepare a Boundary-Scan File

SVF

Configure devices

using Slave Serial mode



Configure

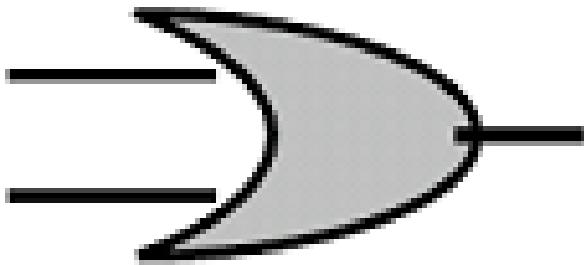
< Back

xs

Design Summary

Boundary Scan

Program Succeeded

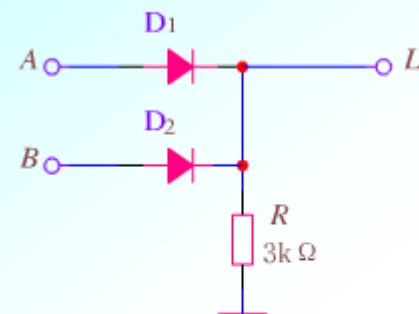


$$A=b+c$$

?

?

或门电路



输入、输出电压之间的关系

输入		输出
V _A (V)	V _B (V)	V _L (V)
0V	0V	0V
0V	5V	5V
5V	0V	5V
5V	5V	5V



或逻辑真值表

输入		输出
A	B	L
0	0	0
0	1	1
1	0	1
1	1	1



XILINX®

Just one statement?

Library ieee

Use ieee.std_logic_1164.all;

Use ieee.std_logic_arith.all;

Use ieee.std_logic_unsigned.all;

Entity device is

port(b: in std_logic; c: in std_logic; a: out std_logic);

End device

Architecture behavioral of device is

A<=b or c;

End behavioral

$$A = b + c$$

You!

- “Two million minutes”

http://v.youku.com/v_show/id_XNjE2NzQ3MDQ=.html

视频: 2 Million Minutes 【纪录片】对比中，美
，印高中教育（无字幕）



欢迎您访问OpenHW, 中国首个 开放源码硬件 社区！当前团队1470个，项目1253个，实名会员53476名。

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FPGA开发全攻略电子书由田耘、苏同麒等人参与编写，他们都是有丰富设计经验的高手。希望这本电子书可以成为对FPGA有兴趣或正在使用FPGA进行开发的工程师的手头设...

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为了避免提到宗教精神被河蟹，现拿一张新闻联播的照片作为镇博之宝吧：照片上那个戴墨镜的哥们，叫 Nicholas McGuire，是兰州大学的客座教授。看到这个照片，和...



预告：NetFPGA10G笔谈(五)Flash ...

忙着写paper连清明3天都木有假期啊。。。这周会写一篇文章专门讲述NetFPGA10G构架中，通过Flash 进行...

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Summary

- Xilinx is No. 1 FPGA Provider in the world
- Platform for embedded and DSP application
- FPGA is the future for next 10 years... **10 years...**
- 1,000,000 Gate will just cost \$2 in the near future
- Open Source Hardware is the future of EE&CS education

Assignments:

- XILINX FPGA 设计基础 第1-2 章
- Lab: 第六章实验一

Thank you

实验、辅导：

- 1、请同学们分组：3-4人/组
- 2、点名、实验、申请实验板、微信群