

A

A

B

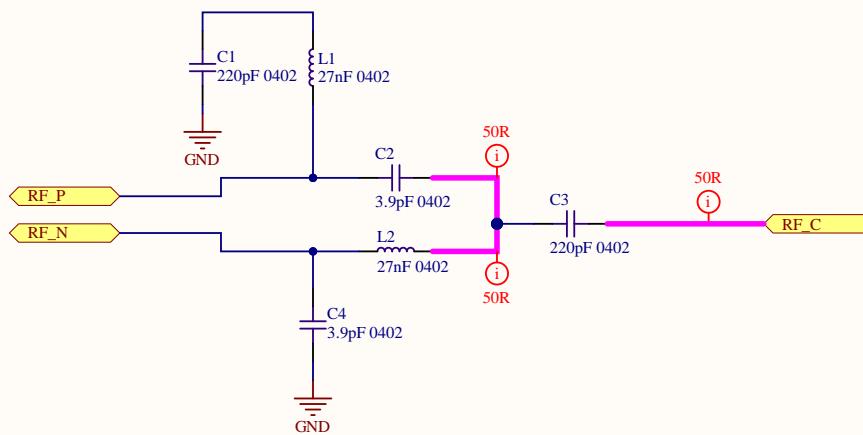
B

C

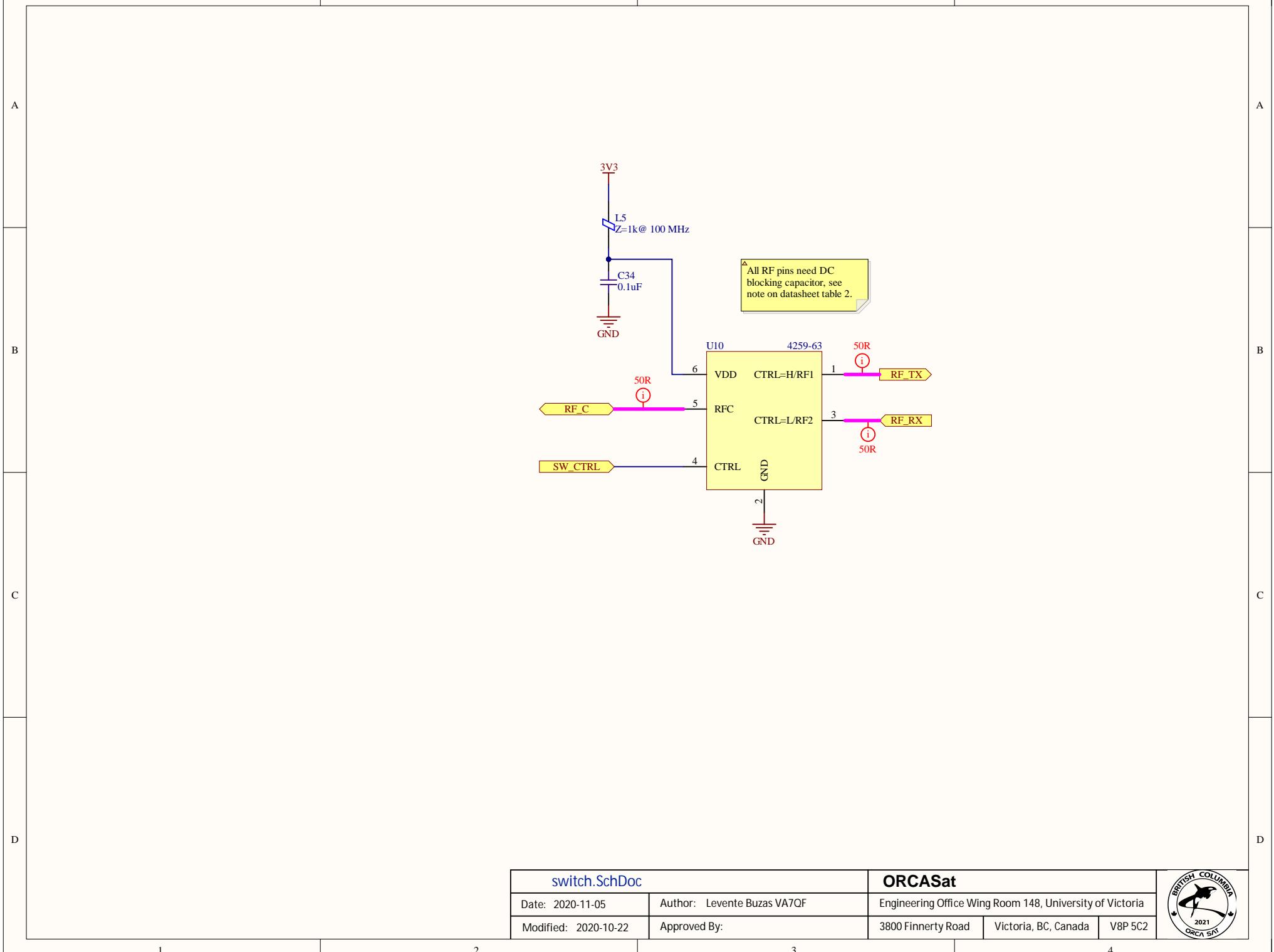
C

D

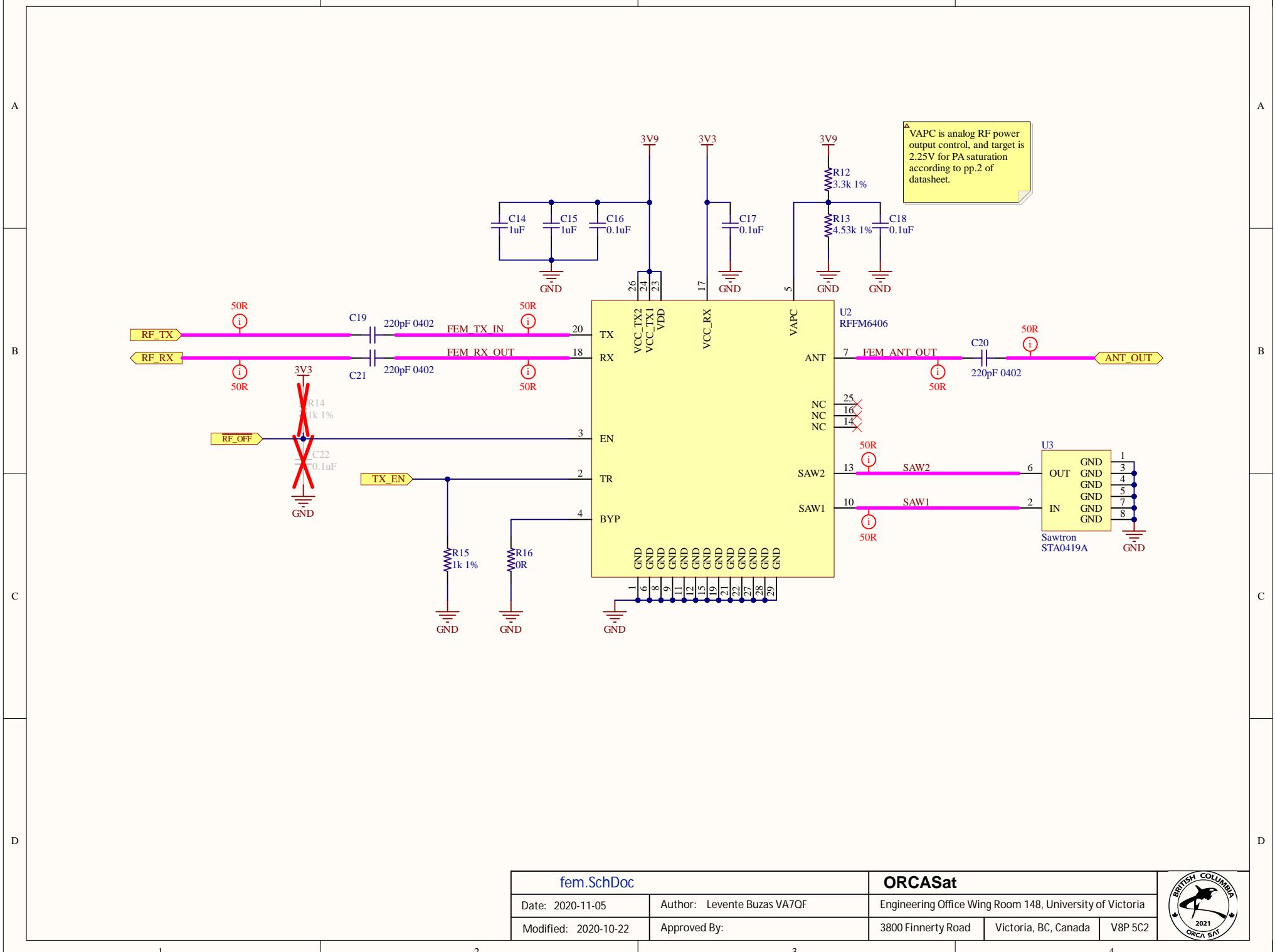
D

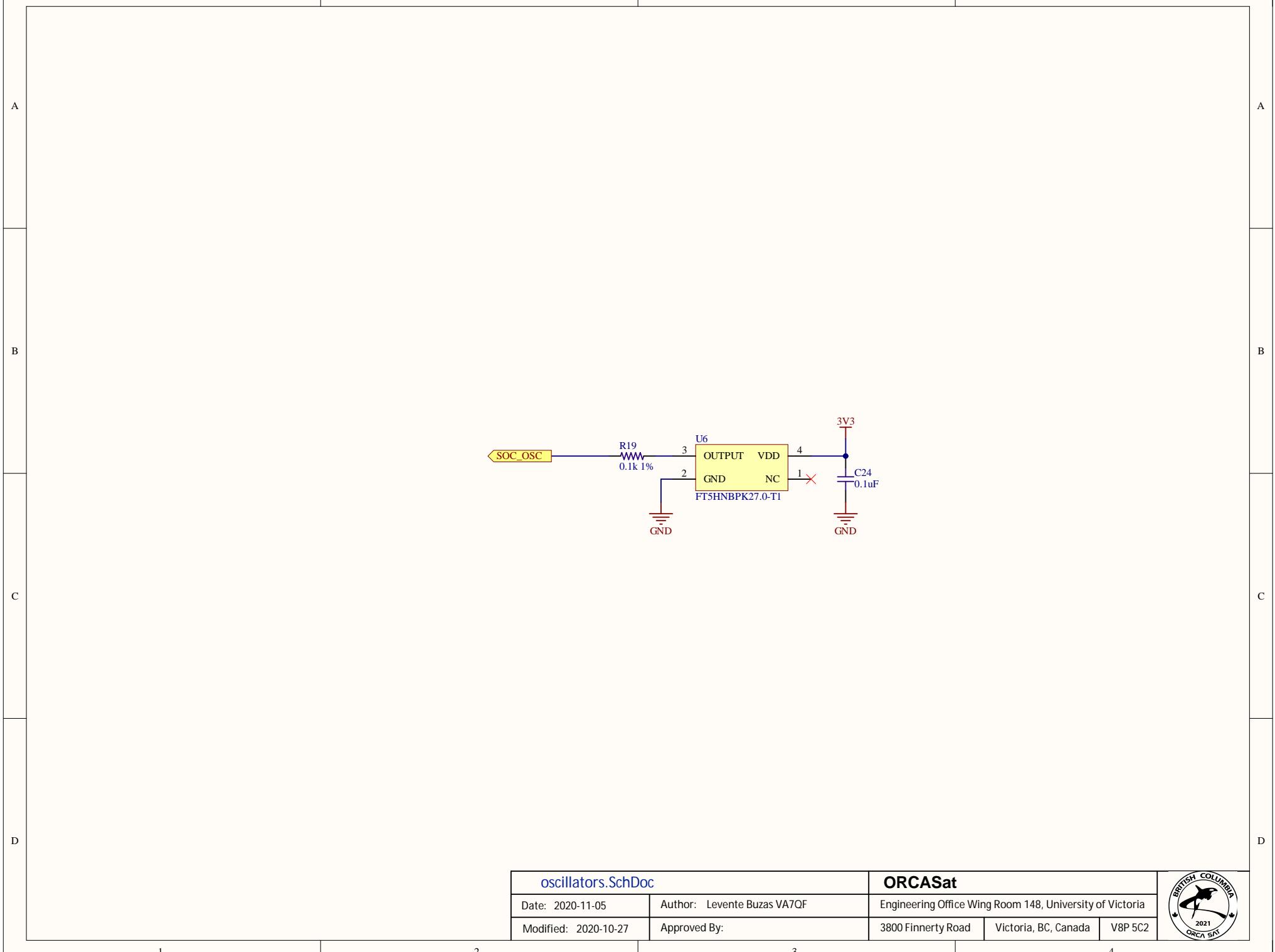


balun.SchDoc		ORCASat			BRITISH COLUMBIA 2021 ORCASAT	
Date: 2020-11-05	Author: Levente Buzas VA7QF	Engineering Office Wing Room 148, University of Victoria				
Modified: 2020-10-27	Approved By:	3800 Finnerty Road	Victoria, BC, Canada	V8P 5C2		



switch.SchDoc		ORCASat			
Date: 2020-11-05	Author: Levente Buzas VA7QF	Engineering Office Wing Room 148, University of Victoria			
Modified: 2020-10-22	Approved By:	3800 Finnerty Road		Victoria, BC, Canada	V8P 5C2





A

A

[▲] See datasheet pp.15-16:

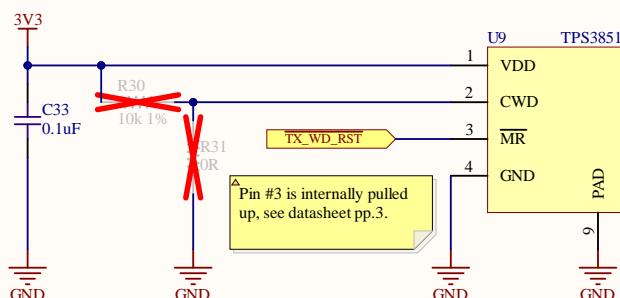
CWD X: (typical tWD) ms
 CWD NC (R to VDD and R to GND DNP): 1600ms
 CWD 10k to VDD (R to GND DNP): 200ms

CWD CAP to GND (R to VDD DNP); tWD (ms) = $3.23 \times \text{CWD} (\text{nF}) + 0.381 (ms)$

CWD CAP in range of 100pF, 1uF, use ceramic capacitor with COG dielectric.

B

B



C

C

[▲] If the watchdog is disabled, WDI cannot be left unconnected and must be driven to either VDD or GND. See datasheet pp. 13.

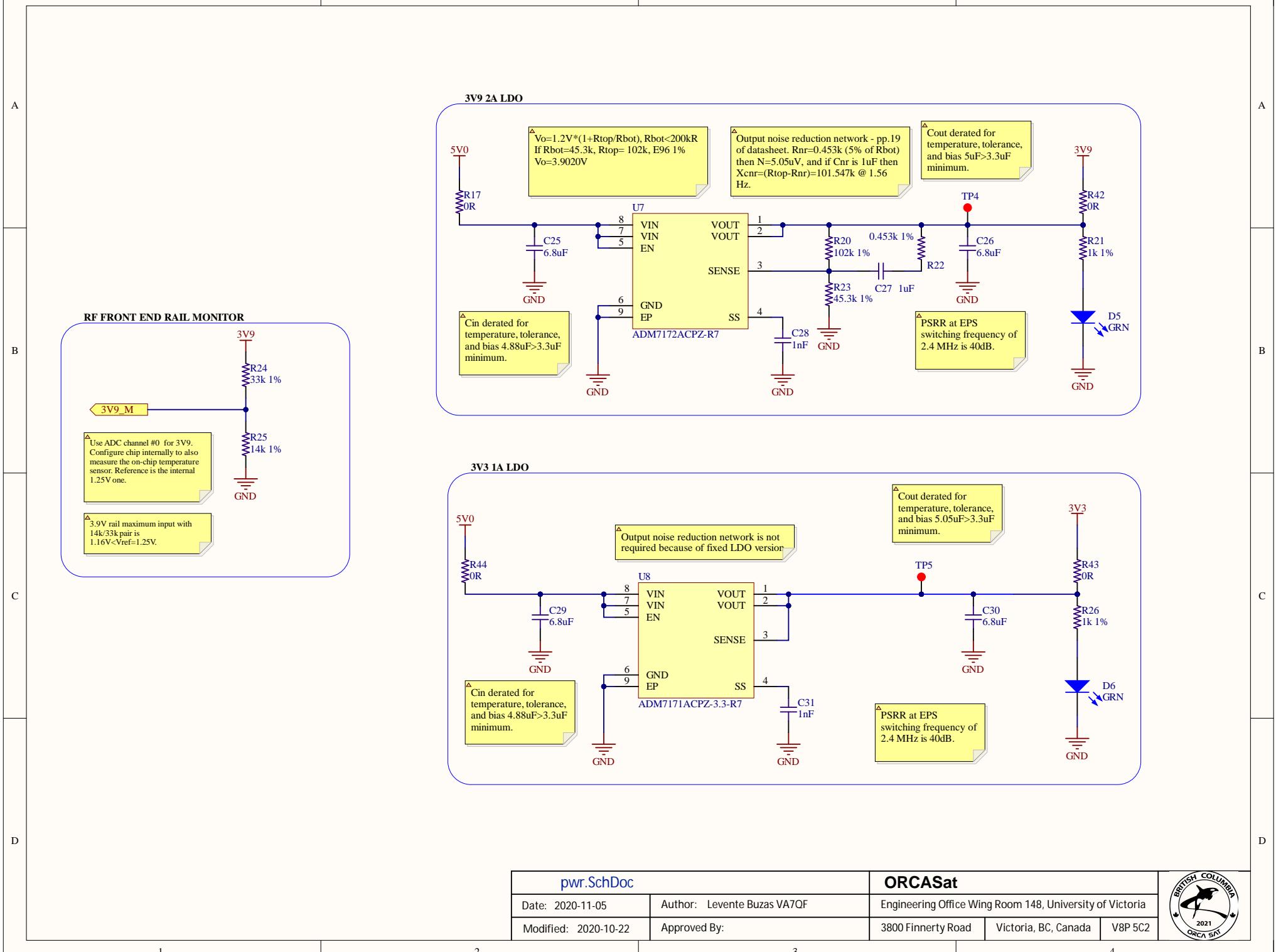


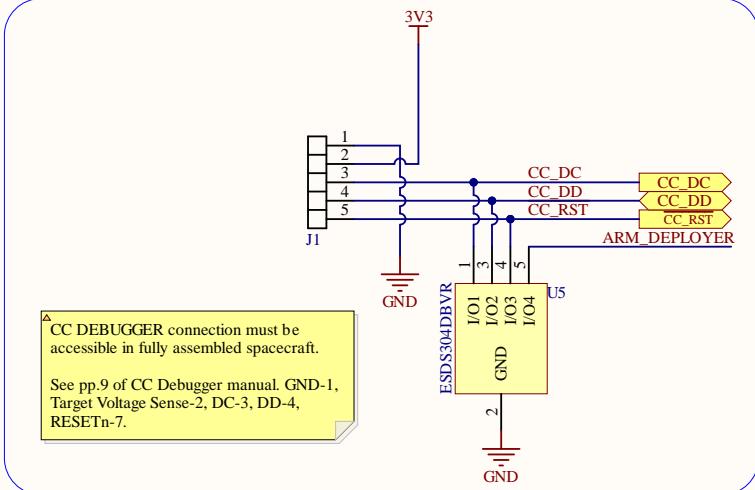
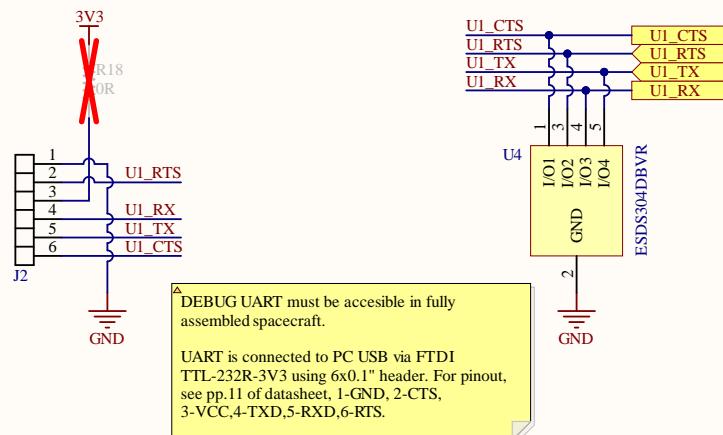
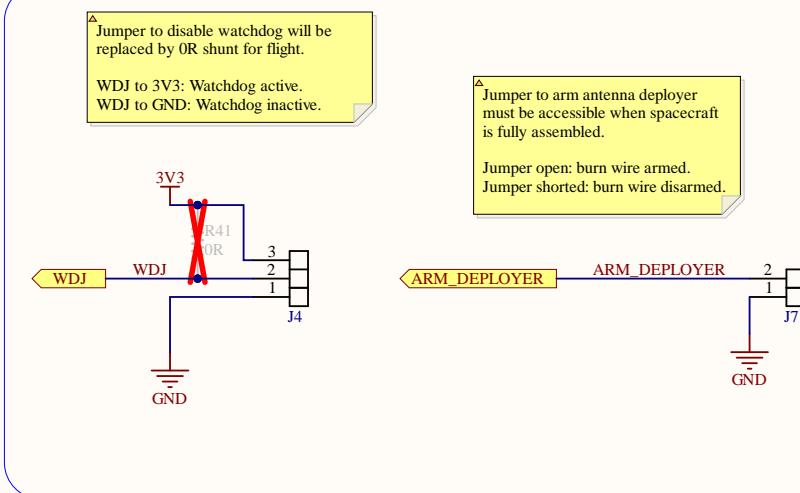
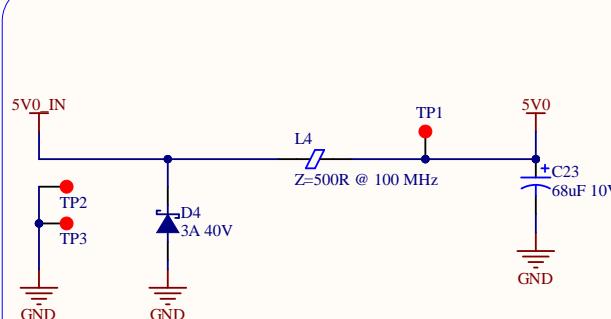
[▲] RESET is active while the 3V3 rail drops to 2.88V and for 200ms after that. During such undervoltage event the watchdog is disabled and WDO is high z.
 WDO is active if there is no pulse on WDI before watchdog expires. It is active for a fixed time of 200ms after which it is inactive.
 RESET and WDO are open drain outputs.

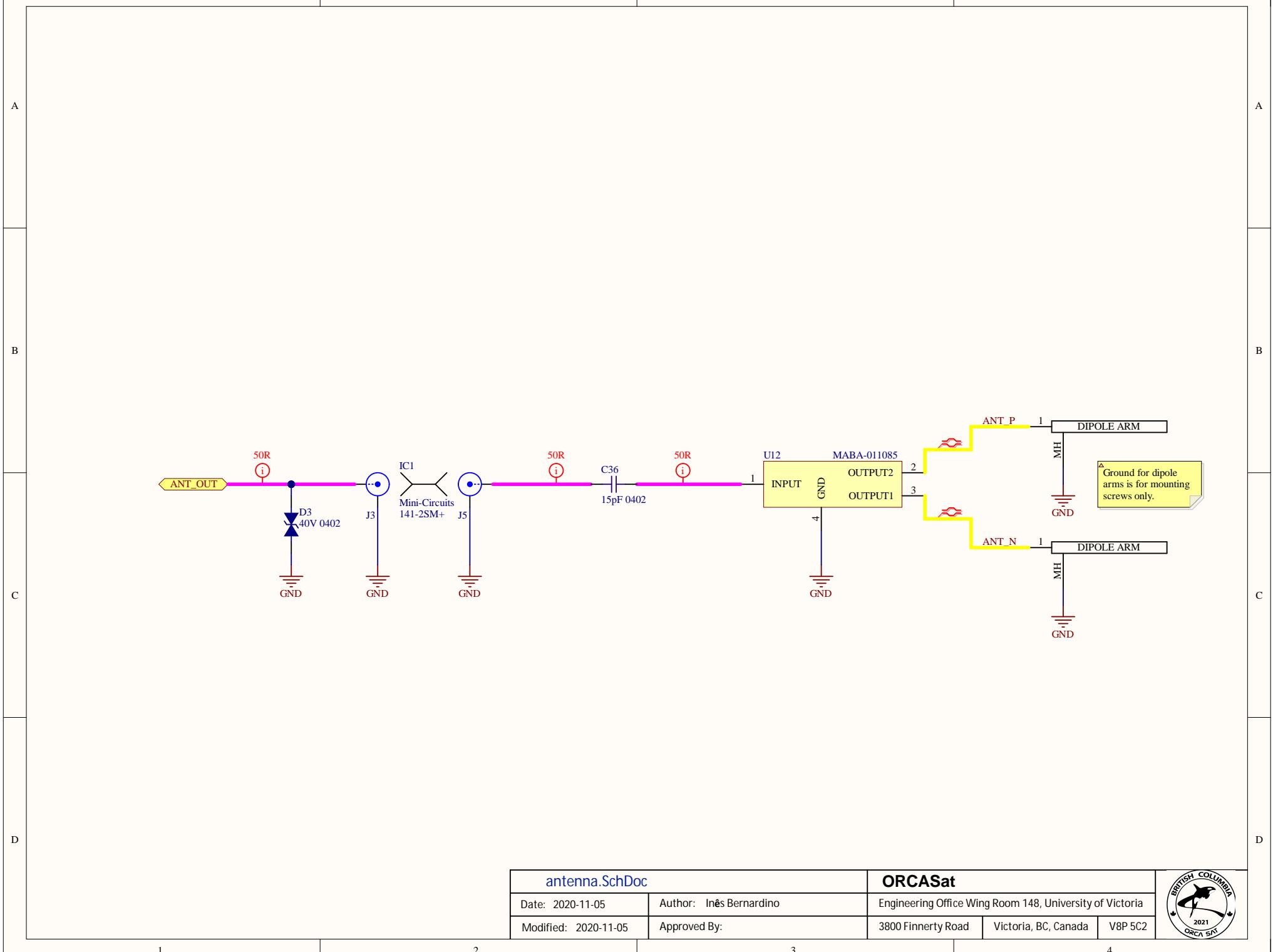
D

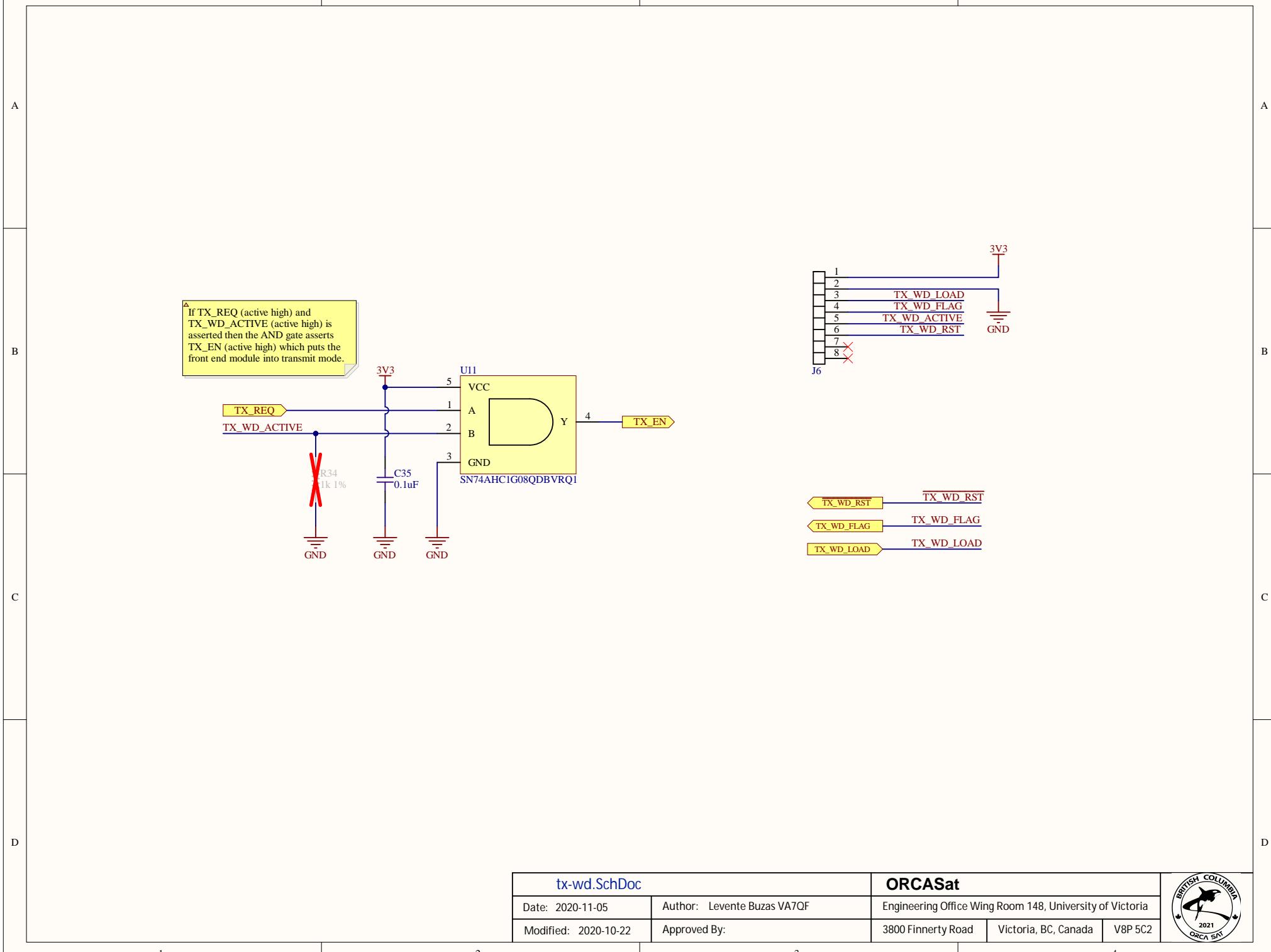
D

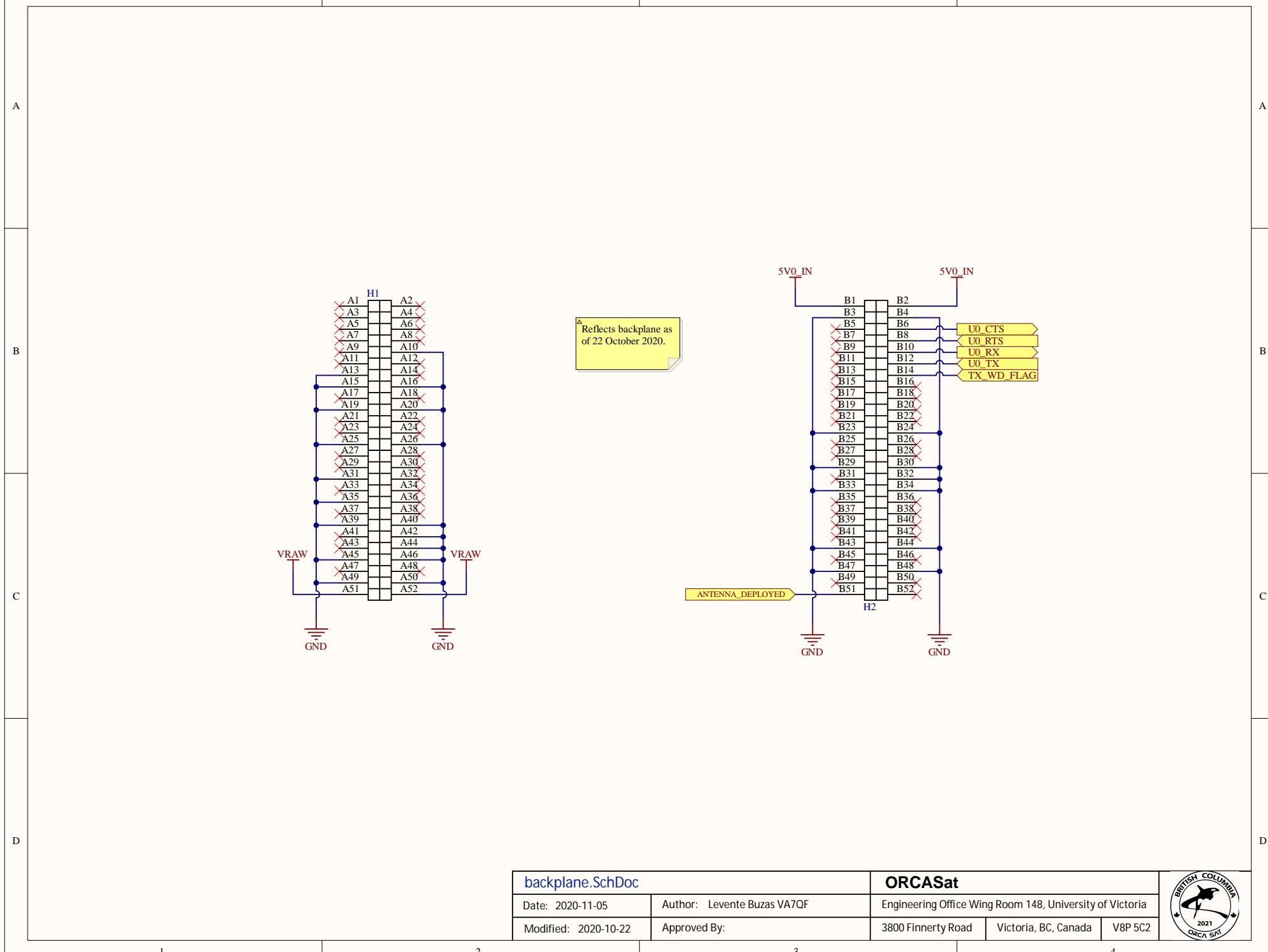
reset.SchDoc		ORCASat			BRITISH COLUMBIA 2021 ORCA SAT	
Date: 2020-11-05	Author: Levente Buzas VA7QF	Engineering Office Wing Room 148, University of Victoria				
Modified: 2020-10-22	Approved By:	3800 Finnerty Road	Victoria, BC, Canada	V8P 5C2		



CC DEBUGGER**DEBUG UART****WATCHDOG DISABLE AND DEPLOYER ARM****POWER INPUT**







1

2

3

4

DEDICATED 3V3 LDO FOR DEPLOYER

