**Directory structure**

**--final**

**--scalar**

**--system.v**

**--vector**

**--vector_all.v**

**--vector_fin.v**

**--config.txt**

**Changes in scalar components**

- No change in **system.v** and ran with yosys flow without any issues

**Changes in vector components**

cd tpu/vtr/
python3 gen_tpu_for_vtr.py -t <path to tpu repo>

- The above command generates vector_all.v

Now the below modifications were made to generate **vpu_fin.v**. This is the file that was used with the yosys flow.

- Changed all the don't care parameters to 0
- Wb_dst, dst, dst_we, dst_mask, vr_src1, vr_src2 to 1D wires and making changes to their references appropriately.
- **Added some missing files to the end of the file - options.v, ram_wrapper.v, components.v, FPAddSub.v, FPMult_16.v, permute.v, reduct_unit.v, transpose.v, trp_unit.v, dma.v, vmem_local.v, dma_axi_mux.v, axi4_slave.v, axi4_master.v.**

The changes have also been provided in the form of a patch (/vector/**diff.patch**) that can be applied to vector_all.v

The vtr task was run with the config file in vector/config.txt