Entity: tx_fsm_axi

- **File**: tx_fsm_axi.vhd

Diagram

Ports

Port name	Direction	Type	Description
clk	in	std_logic	100 MHz Clock
resetn	in	std_logic	Active low reset
packet_ready	in	std_logic	PT is not busy, ready to receive!
packet_valid	out	std_logic	RAM contains valid packet and is ready to transmit
wr_en	out	std_logic	RAM Write Enable
tlast	in	std_logic	AXI4-S End of packet signal
tready	out	std_logic	AXI4-S Ready signal
tvalid	in	std_logic	AXI4-S Valid signal
addr	out	std_logic_vector(10 downto 0)	RAM Data Address

Signals

Name	Type	Description
state	state_t	FSM State Variables
next_state	state_t	FSM State Variables
cnt_addr	unsigned(10 downto 0)	Address Counter

Enums

state_t

TX AXI Bus FSM states

Name	Description
IDLE	AXI Bus receiver is idle as TX is busy
READY	AXI Bus receiver is ready to receive
RECEIVING	AXI Bus receiver is receiving actively
LAST	AXI Bus receiver has received the tlast signal

Processes

- p_seq: (clk, resetn)

  Description
  Sequential Logic Update & State Register Process

- p_cmb: (state, packet_ready, tlast, tvalid)

  Description
  Combinatorial logic for FSM state updates

State machines

- Combinatorial logic for FSM state updates