Entity: rx_fcs_verify

- File: rx_fcs_verify.vhd
- Title: Ethernet FCS (CRC-32) checker

Diagram

Description

This file implements an Ethernet FCS (CRC-32) checker. It wraps a rx_fcs_crc core configured for the standard Ethernet polynomial 0x04C11DB7 (reflected 0xEDB88320), seeded to 0xFFFFFFFF and using a final XOR of 0xFFFFFFFF. Bytes arrive on data[7:0] when enable='1'; the checker updates the running CRC until begin_fcs is asserted, then captures the next four received FCS bytes. It declares the frame valid by raising fcs_valid when the computed CRC (after the final XOR inside the core) matches the received CRC. The interface uses clk and an active-low rst, with simple handshaking via enable/begin_fcs.

Ports

Port name	Direction	Type	Description
clk	in	std_logic	System Clock
rst	in	std_logic	Active Low Reset
data	in	std_logic_vector(7 downto 0)	8-bit data input
enable	in	std_logic	Enable Pin to send data through to CRC generation
begin_fcs	in	std_logic	Enable to end generation and send through comparison CRC Bytes
fcs_valid	out	std_logic	Output bit to Say Valid CRC in Packet

Signals

Name	Type	Description
crc_reg	std_logic_vector(31 downto 0)	CRC Register init 0xFFFFFFFF
crc_next	std_logic_vector(31 downto 0)	Next Generated CRC
crc_existing	std_logic_vector(31 downto 0)	Previous CRC
fcs_reg	std_logic	Valid FCS Register
final	boolean	Register thats set by Begin FCS
finalcount	std_logic	Count of the Final Four Bytes
crc_reset	std_logic	Pin to Reset the CRC Generation

Processes

- p_cmb: (clk, rst, enable)

  Description
  Sequential process for state update

Instantiations

- crc_core: work.rx_fcs_crc

  Description
  Instantiate the CRC-32 core