Entity: tx_phy

- **File**: tx_phy.vhd

Diagram

Description

The TX PHY is responsible for encoding transmitted data into manchester encoding and generating NLP pulses when the link has been active for 1.6ms. It contains a FSM that is used to control the internal logic. Input to output latency is 1 CLK.

Ports

Port name	Direction	Type	Description
clk	in	std_logic	100 MHz Clock
resetn	in	std_logic	Low active reset
tx_active	in	std_logic	Packet transmission is active
bit_valid	in	std_logic	Input bit is valid for this clock cycle
driver_en	out	std_logic	Output driver is enabled
bit_in	in	std_logic	Input bit to encode
tx_out	out	std_logic	Output Manchester / NLP data

Signals

Name	Type	Description
state	state_t	FSM State Variables
next_state	state_t	FSM State Variables
r_mcn_out	std_logic	Internal manchester encoder output
r_mcn_bit_in	std_logic	Internal register for bit_in
r_mcn_phase	std_logic	Phase used to generate manchester encoding
r_nlp_out	std_logic	Internal NLP generator output
r_inactivity_counter	unsigned(20 downto 0)	Idle inactivity counter (for NLP)
r_clk_counter	unsigned(4 downto 0)	Clock Enable Counter for NLP and TP_IDL
r_tp_idl_out	std_logic	

Constants

Name	Type	Value	Description
NLP_TIMEOUT	unsigned(20 downto 0)	to_unsigned(1_600_000, 21)	802.3i specification NLP timeout

Enums

state_t

PHY FSM states

Name	Description
IDLE	Nothing is happening here...
TX	Manchester encoding (TX Data) in progress
NLP	Line is idle and NLP is being sent out
TP_IDL_WAIT	Waiting for end of current bit time before going to TP_IDL
TP_IDL	Sending End of Packet Signal

Processes

- p_seq: (clk, resetn)

  Description
  Sequential Logic Update & State Register Process

- p_cmb: (state, tx_active, r_clk_counter, r_inactivity_counter, r_mcn_out)

  Description
  Combinatorial logic for FSM state updates

State machines

- Combinatorial logic for FSM state updates