Entity: NLP_receiver

- File: nlp_receiver.vhd

Diagram

Ports

Port name	Direction	Type	Description
resetn	in	std_logic	active low reset
clk_in	in	std_logic	100MHz clock
manchester_in	in	std_logic	manchester signal
link_active	out	std_logic	port link is active (active low)

Signals

Name	Type	Description
NLP_count	unsigned(20 downto 0)	Counter
manchester_prev	std_logic	prev mancehster logic

Constants

Name	Type	Value	Description
gap_length	integer	1600000	16ms (1600000 clk cycles)

Processes

- NLP: (clk_in, resetn)