

Entity: axi4s_interconnect

- File: axi4s_interconnect.vhd

Diagram

Ports

Port name	Direction	Type	Description
clk	in	std_logic	
resetn	in	std_logic	
PA_RX_tdata	in	std_logic_vector(7 downto 0)	
PA_RX_tvalid	in	std_logic	
PA_RX_tlast	in	std_logic	
PA_RX_tready	out	std_logic	
PA_TX_tdata	out	std_logic_vector(7 downto 0)	
PA_TX_tvalid	out	std_logic	
PA_TX_tlast	out	std_logic	
PB_RX_tdata	in	std_logic_vector(7 downto 0)	
PB_RX_tvalid	in	std_logic	
PB_RX_tlast	in	std_logic	
PB_RX_tready	out	std_logic	
PB_TX_tdata	out	std_logic_vector(7 downto 0)	
PB_TX_tvalid	out	std_logic	
PB_TX_tlast	out	std_logic	
PC_RX_tdata	in	std_logic_vector(7 downto 0)	
PC_RX_tvalid	in	std_logic	
PC_RX_tlast	in	std_logic	
PC_RX_tready	out	std_logic	
PC_TX_tdata	out	std_logic_vector(7 downto 0)	
PC_TX_tvalid	out	std_logic	
PC_TX_tlast	out	std_logic	
PD_RX_tdata	in	std_logic_vector(7 downto 0)	
PD_RX_tvalid	in	std_logic	
PD_RX_tlast	in	std_logic	
PD_RX_tready	out	std_logic	
PD_TX_tdata	out	std_logic_vector(7 downto 0)	
PD_TX_tvalid	out	std_logic	
PD_TX_tlast	out	std_logic	
PE_RX_tdata	in	std_logic_vector(7 downto 0)	
PE_RX_tvalid	in	std_logic	
PE_RX_tlast	in	std_logic	
PE_RX_tready	out	std_logic	
PE_TX_tdata	out	std_logic_vector(7 downto 0)	
PE_TX_tvalid	out	std_logic	
PE_TX_tlast	out	std_logic	

Signals

Name	Type	Description
last_port	port_t	
active_port	port_t	
PA_TX_tdata_reg	std_logic_vector(7 downto 0)	
PA_TX_tvalid_reg	std_logic	
PA_TX_tlast_reg	std_logic	
PB_TX_tdata_reg	std_logic_vector(7 downto 0)	
PB_TX_tvalid_reg	std_logic	
PB_TX_tlast_reg	std_logic	
PC_TX_tdata_reg	std_logic_vector(7 downto 0)	
PC_TX_tvalid_reg	std_logic	
PC_TX_tlast_reg	std_logic	

Name	Type	Description
PD_TX_tdata_reg	std_logic_vector(7 downto 0)	
PD_TX_tvalid_reg	std_logic	
PD_TX_tlast_reg	std_logic	
PE_TX_tdata_reg	std_logic_vector(7 downto 0)	
PE_TX_tvalid_reg	std_logic	
PE_TX_tlast_reg	std_logic	

Enums

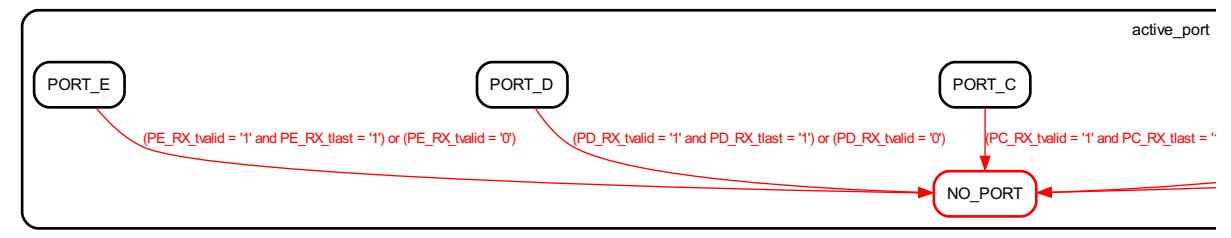
port_t

Name	Description
NO_PORT	
PORT_A	
PORT_B	
PORT_C	
PORT_D	
PORT_E	

Processes

- p_contention_controller: (clk)
- p_output_controller: (clk)

State machines



undefined