Entity: rx_2ff

- File: rx_2ff.vhd

Diagram

Ports

Port name	Direction	Type	Description
clk_in	in	std_logic	100MHz clock
manchester_in	in	std_logic	Manchester input
resetn	in	std_logic	active low reset
manchester_out	out	std_logic	inverted Synchronised manchester output

Signals

Name	Type	Description
sync	std_logic	hold inital signal
sync2	std_logic	synchronsied signal

Processes

- FF2: (clk_in, resetn)