Entity: rx_fsm_AXI

- File: rx_fsm_axi.vhd

Diagram

Ports

Port name	Direction	Type	Description
clk_in	in	std_logic	100MHz clock
resetn	in	std_logic	active low reset
AXI_en	in	std_logic	enable AXI transmitter
tready	in	std_logic	interconnect ready to receive packet
packet_valid	in	std_logic	packet is valid and can be read
size_in	in	std_logic_vector(15 downto 0)	size of packet
fcs_fail	in	std_logic	fcs fail
tvalid	out	std_logic	transmitting data is valid
tlast	out	std_logic	last packet being transmitted
packet_ready	out	std_logic	packet is ready to be received by AXI transmitter
addr_in	in	std_logic_vector(10 downto 0)	Address read by Address reader

Signals

Name	Type	Description
current_state	AXI_state	
next_state	AXI_state	
size_buf	std_logic_vector(10 downto 0)	buffer to hold packet size
counter_en	std_logic	timeout counter enable
counter	unsigned (12 downto 0)	counter for timeout

Enums

AXI_state

Name	Description
AXI_IDLE	awaiting packet
AXI_SIZE	pr packet is valid -> packet size is received
AXI_DATA	Data transmission
AXI_LAST	Last byte of data transmission
AXI_WAIT	wait for tready to be set high

Processes

- sequential: (clk_in, resetn)
- AXI_fsm: (packet_valid, tready, AXI_en, addr_in, current_state, size_buf, fcs_fail)

State machines