Entity: rx_fsm_pr

- File: rx_fsm_pr.vhd

Diagram

Ports

Port name	Direction	Type	Description
clk_in	in	std_logic	100MHz clock
resetn	in	std_logic	active low
byte_valid	in	std_logic	byte valid from sipo
packet_ready	in	std_logic	packet ready to receive
RX_timeout	in	std_logic	end of packet
wr_en	out	std_logic	writing enabled for RAM
packet_valid	out	std_logic	packet is valid and can be read from RAM
data_in	in	std_logic_vector(7 downto 0)	data input
addr_out	out	std_logic_vector(10 downto 0)	address output
data_out	out	std_logic_vector(7 downto 0)	data output
size_out	out	std_logic_vector(15 downto 0)	Packet size

Signals

Name	Type	Description
current_state	RX_state	
next_state	RX_state	
preamble_detect	std_logic	signal for preamble detection
SFD_detect	std_logic	signal for SFD detection
SIZE_lower	std_logic	Append lower size byte
SIZE_upper	std_logic	Append upper size byte
packet_hand	std_logic	packet valid/ready handshake signal
data_buf	std_logic_vector(7 downto 0)	data buffer for direct state output
cnt_addr	unsigned(10 downto 0)	counter for RAM address
cnt_size	unsigned(15 downto 0)	counter for paylaod size (NO. of bytes)

Constants

Name	Type	Value	Description
preamble	std_logic_vector(55 downto 0)	x"55555555555555"	preamble constant
SFD	std_logic_vector(7 downto 0)	x"D5"	SFD constant

Enums

RX_state

Packet receiving FSM states

Name	Description
RX_PREAMBLE	detecting preamble of data stream
RX_SFD	detecting SFD of data stream
RX_DATA	Packet data being read
RX_SIZE	reading packet data
RX_END	detect end of data stream

Processes

- unnamed: (clk_in, resetn)
- main_fsm: (current_state, preamble_detect, SFD_detect, RX_timeout, packet_hand, SIZE_lower)

State machines