Entity: rx_fcs_crc

- File: rx_fcs_crc.vhd
- Title: CRC Generation through Polynomial

Diagram

Description

This file defines the CRC-32 generation core used for Ethernet Frame Check Sequence (FCS) computation. It implements the standard polynomial x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1 (corresponding to 0x04C11DB7) in a right-shifting, little-endian configuration. The entity rx_fcs_crc accepts 8-bit input data words and updates the 32-bit CRC value on each clock cycle when crc_en is asserted. The CRC register is initialised to 0xFFFFFFFF on reset and updates synchronously with clk, while the output crcOut presents the current CRC value after applying the final XOR with 0xFFFFFFFF. The architecture explicitly defines each XOR tap in the polynomial, providing full combinational logic for bit-wise CRC computation suitable for hardware implementation.

Ports

Port name	Direction	Type	Description
clk	in	std_logic	System clock
rst	in	std_logic	Active low reset
crc_en	in	std_logic	Generation enable signal: update CRC when '1'
data	in	std_logic_vector(7 downto 0)	8-bit data input
crcOut	out	std_logic_vector(31 downto 0)	Current CRC value

Signals

Name	Type	Description
crc_in_signal	std_logic_vector(31 downto 0)	Current CRC state (Updated on Clock Cycle)
crc_out_signal	std_logic_vector(31 downto 0)	

Processes

- p_seq: (clk, rst)

  Description
  Sequential process for state update