Entity: sr_piso

- **File**: sr_piso.vhd

Diagram

Description

Parallel-In, Serial Output Shift Register with configurable delay for bit output. Byte valid to first bit latency is 2 CLKs. Bit to Bit latency is BIT_DELAY CLKs. If sending multiple bytes in close contact, the next byte may be sent anytime after byte_ready goes high and 2 CLKs before the first bit out (otherwise a gap in output may be observed). Bit order within octet is LSB first.

Generics

Generic name	Type	Value	Description
WIDTH	positive	8	Width of input byte
BIT_DELAY	positive	1	Number of clocks between each bit output

Ports

Port name	Direction	Type	Description
clk	in	std_logic	Input clock
resetn	in	std_logic	Active-low synchronous reset
byte_in	in	std_logic_vector(WIDTH - 1 downto 0)	Input byte data
byte_valid	in	std_logic	Pulse high when byte_in is valid
byte_ready	out	std_logic	High when this PISO can accept a new byte
bit_out	out	std_logic	Serial bit output
bit_valid	out	std_logic	1-clk strobe: bit_out is valid this cycle

Signals

Name	Type	Description
r_byte	std_logic_vector(WIDTH - 1 downto 0)	Input byte register
cnt_bit_rem	unsigned(LEN_BIT_REM - 1 downto 0)	Remaining bit counter
cnt_bit_delay	unsigned(LEN_BIT_DELAY - 1 downto 0)	Bit Delay Counter
state	state_t	FSM State Variables
next_state	state_t	FSM State Variables

Constants

Name	Type	Value	Description
LEN_BIT_REM	positive	integer(ceil(log2(real(WIDTH + 1))))	Constant that counts how many bits is required to represent values from 0 to WIDTH-1
LEN_BIT_DELAY	positive	integer(ceil(log2(real(BIT_DELAY))))	Constant that counts how many bits is required to present values from 0 to BIT_DELAY

Enums

state_t

PISO SR FSM states

Name	Description
IDLE	Awaiting new data to shift
TX	Actively shifting data & unable to accept new data
TX_BYTE_READY	Actively shifting data & able to accept new data

Processes

- p_seq: (clk, resetn)

  Description
  Sequential Logic Update & State Register Process

- p_cmb: (state, byte_valid, cnt_bit_rem, cnt_bit_delay)

  Description
  Combinatorial logic for FSM state updates

State machines

- Combinatorial logic for FSM state updates