Entity: rx_decoder

- File: rx_decoder.vhd

Diagram

Ports

Port name	Direction	Type	Description
clk_in	in	std_logic	100 MHz Clock
manchester_in	in	std_logic	Manchester Input
resetn	in	std_logic	Active low reset
data_out	out	std_logic	Decoded bitsream
RX_timeout	out	std_logic	Timeout for end of packet
bit_valid	out	std_logic	Bit is valid and can be read by SIPO

Signals

Name	Type	Description
data_buf	std_logic_vector(55 downto 0)	Register to hold incoming edges for clock recovery
manchester_prev	std_logic	Prev input to detect edge.
timeout	std_logic	timeout to reset logic

Processes

- decode: (clk_in, resetn)
- rxtimeout: (clk_in, resetn)