Entity: rx_fsm_adr

- File: rx_fsm_adr.vhd

Diagram

Ports

Port name	Direction	Type	Description
clock	in	std_logic	100MHz clock
reset	in	std_logic	Active low reset
valid	in	std_logic	byte strobe
tlast	in	std_logic	Transmit Final Flag
fcs_valid	in	std_logic	Valid FCS Check
size	in	std_logic_vector(15 downto 0)	payload length (bytes)
axi_en	out	std_logic	axi4 bus enable flag
crc_en	out	std_logic	CRC enable generation variable
begin_fcs	out	std_logic	Flag to begin generation of the comparison FCS CRC
fcs_fail	out	std_logic	fcs fail
addr	out	std_logic_vector(10 downto 0)	address output

Signals

Name	Type	Description
state	state_t	
next_state	state_t	
addr_reg	unsigned(10 downto 0)	address register
size_lat	unsigned(15 downto 0)	packet size
cnt	unsigned(1 downto 0)	counter for CRC failure detection
val_reg	std_logic	register to hold valid

Constants

Name	Type	Value	Description
ADDR_BASE	unsigned(10 downto 0)	to_unsigned(10, 11)	Starting base for address

Enums

state_t

Name	Description
IDLE	IDLE and awaiting packet
CRC	Reading addresses for CRC
AXI	reading addresses for AXI Transmitter

Processes

- sequential: (clock, reset)
- FSM: (state, valid, tlast, fcs_valid, cnt, val_reg)

State machines