Entity: eth_tx

- **File**: eth_tx.vhd

Diagram

Description

This entity puts together all other TX pieces into a cohesive entity that takes in an AXI4-Stream data stream and transmits it out in 10Base-T ethernet format. For a full explanation of how this works, see the theory of operation section of the TX section of the documentation.

Ports

Port name	Direction	Type	Description
clk	in	std_logic	100 MHz Clock
resetn	in	std_logic	Active low reset
tx	out	std_logic	Manchester Encoded Output Signal
tx_en	out	std_logic	Driver Enable
tvalid	in	std_logic	AXI4-Stream valid signal
tready	out	std_logic	AXI4-Stream ready signal
tlast	in	std_logic	AXI4-Stream end of packet signal
tdata	in	std_logic_vector(7 downto 0)	AXI4-Stream Data Line

Signals

Name	Type	Description
r_bs	std_logic	PISO to PHY. Ethernet bitstream
r_rd_data	std_logic_vector(7 downto 0)	RAM to PISO. Ethernet bytestream
r_wr_en	std_logic	FSM AXI to RAM. RAM write enable
r_wr_addr	std_logic_vector(10 downto 0)	FSM AXI to RAM. RAM write address
r_rd_addr	std_logic_vector(10 downto 0)	FSM PT to RAM. RAM read address
r_byte_valid	std_logic	FSM PT to SR PISO. High when a valid byte is on r_rd_data
r_byte_ready	std_logic	SR PISO to FSM PT. High when the shift register is ready to accept a new byte
r_bit_valid	std_logic	SR PISO to FSM PHY. High when a valid bit is on r_bs
r_tx_active	std_logic	FSM PT to FSM PHY. High when a transmit operation is in process

Name	Type	Description
r_packet_ready	std_logic	FSM PT to FSM AXI. High when the system is ready to transmit a new packet
r_packet_valid	std_logic	FSM AXI to FSM PT. High when a valid packet has been received over AXI4-Stream and is in the RAM

Instantiations

- c_phy: work.tx_phy(arch)

  Description
  Physical layer finite state machine. For more details see module documentation.

- c_ram: work.ram_eth_packet(SYN)

  Description
  Altera RAM. 2 M9Ks providing dual port access with an 8 bit bus to 2048 bytes

- c_piso_sr: work.sr_piso(rtl)

  Description
  Parallel-In, Serial-Out Shift Register. For more details see module documentation.

- c_fsm_pt: work.tx_fsm_pt(arch)

  Description
  Finite State Machine Packet Transmission. For more details see module documentation.

- c_fsm_axi: work.tx_fsm_axi(arch)

  Description
  Finite State Machine Advanced eXtensible Interface v4 Stream. For more details see module documentation.