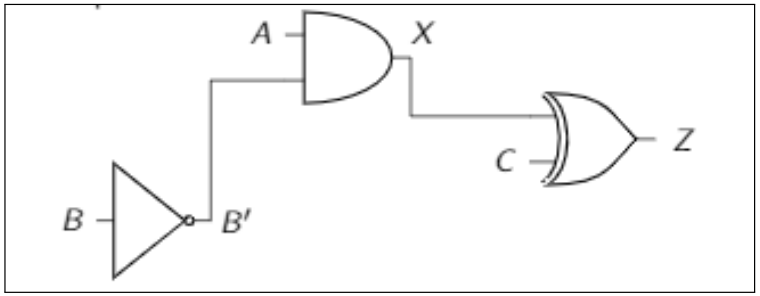
Assignment 11

UTTAKARSHIKA
CS20B1023
IIIT RAICHUR

6TH JANUARY, 2021

Problem Statement

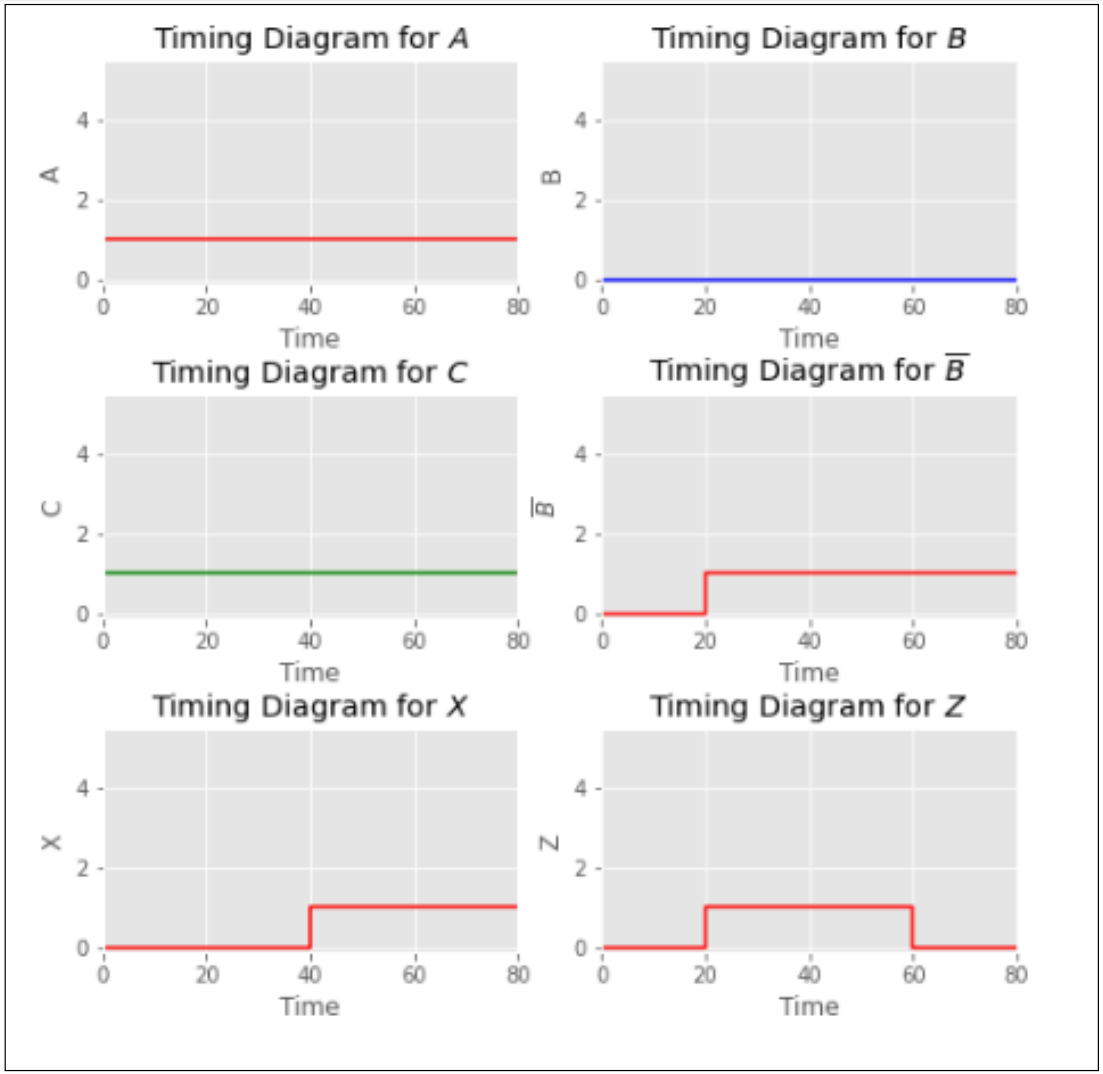
EC GATE 2015, 37-
All the logic gates shown in the figure have a propagation delay of 20ns. Let A=C=0 and B=1 until time t=0. At t=0, all the inputs flip (i.e., A=C=1 and B=0) and remain in that state. For t >0, output Z=1 for a duration of-



Propagation Delay

Propagation delay refers to the time taken by a signal to reach its destination.

Solution / Timing Diagrams



Solution / Truth Table

time(t)	A	B	C	B'	X	Z
<0	0	1	0	0	0	0
0	1	0	1	0	0	0
20	1	0	1	1	0	1
40	1	0	1	1	1	1
60	1	0	1	1	1	0
80	1	0	1	1	1	0

Conclusion

According to the given timing diagram, Z=1 for a duration of 20-60ns.