ASSIGNMENT 9

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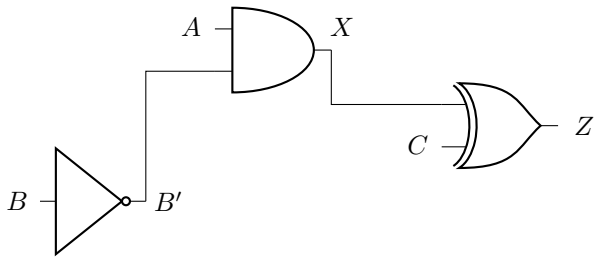
1 All logic gates shown in the figure have a propagation delay for 20ns. Let A=C=0 and B=1 until time t=0. At t=0, all inputs flip(i.e., A=C=1 and B=0) and remain in that state. for t greater than 0, output Z=1 for a duration of(in ns)-

SOLUTION-

Using the graphs and table provided, we come to the conclusion that-

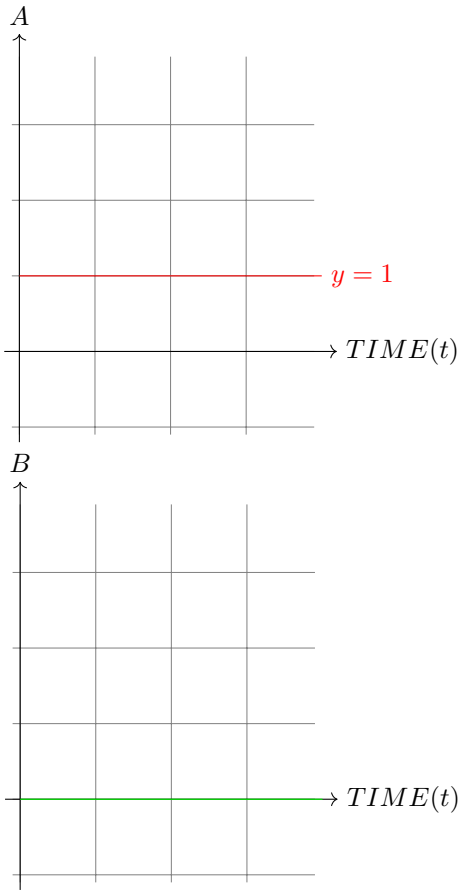
Z=1 FOR t=20ns-60ns

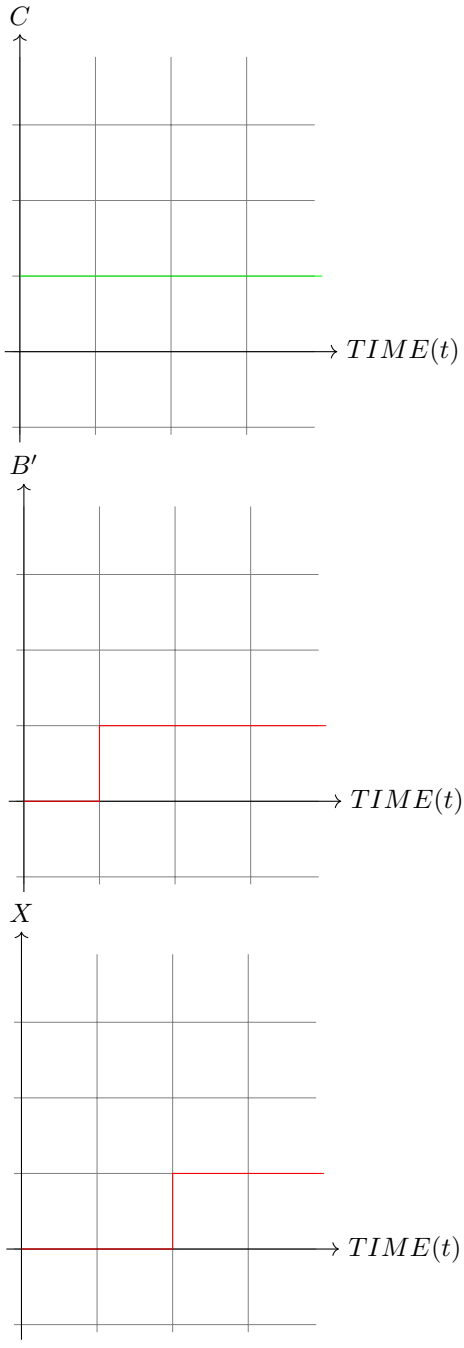
BOOLEAN EXPRESSION $\overline{A\bar{B}} + A\bar{B}\bar{C}$

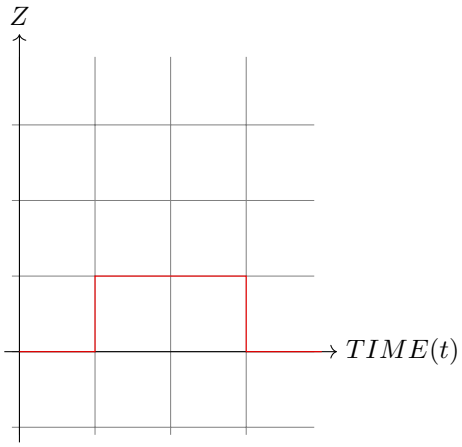


time(t)	A	B	C	B'	X	Z
less than 0	0	1	0	0	0	0
0	1	0	1	0	0	0
20	1	0	1	1	0	1
40	1	0	1	1	1	1
60	1	0	1	1	1	0
80	1	0	1	1	1	0

KEY FOR GRAPHS-
ALONG X-AXIS- 1 UNIT=20ns
Y-AXIS- 1 UNIT=1




C
TIME(t)
B′
TIME(t)
X
TIME(t)


Z
TIME(t)