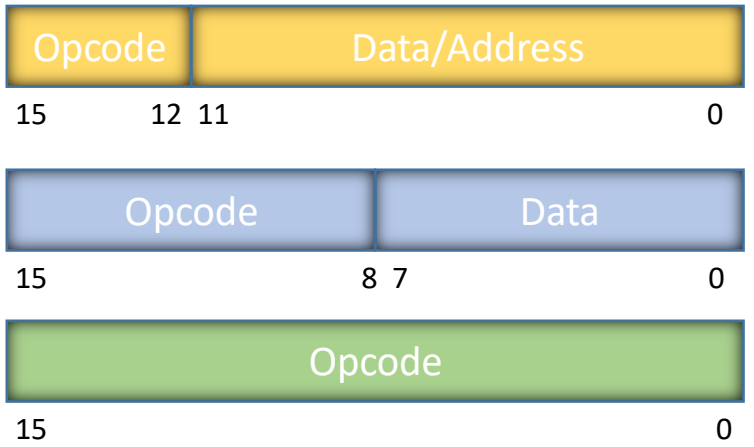
Processor that is Useful and New for Education of Hardware

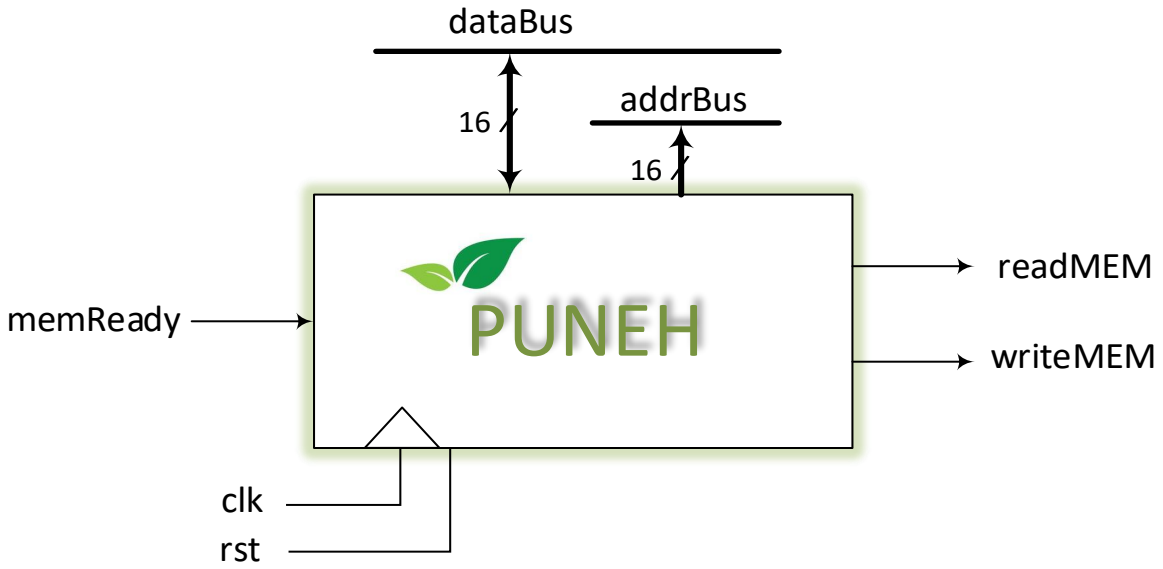
Instruction Set Architecture



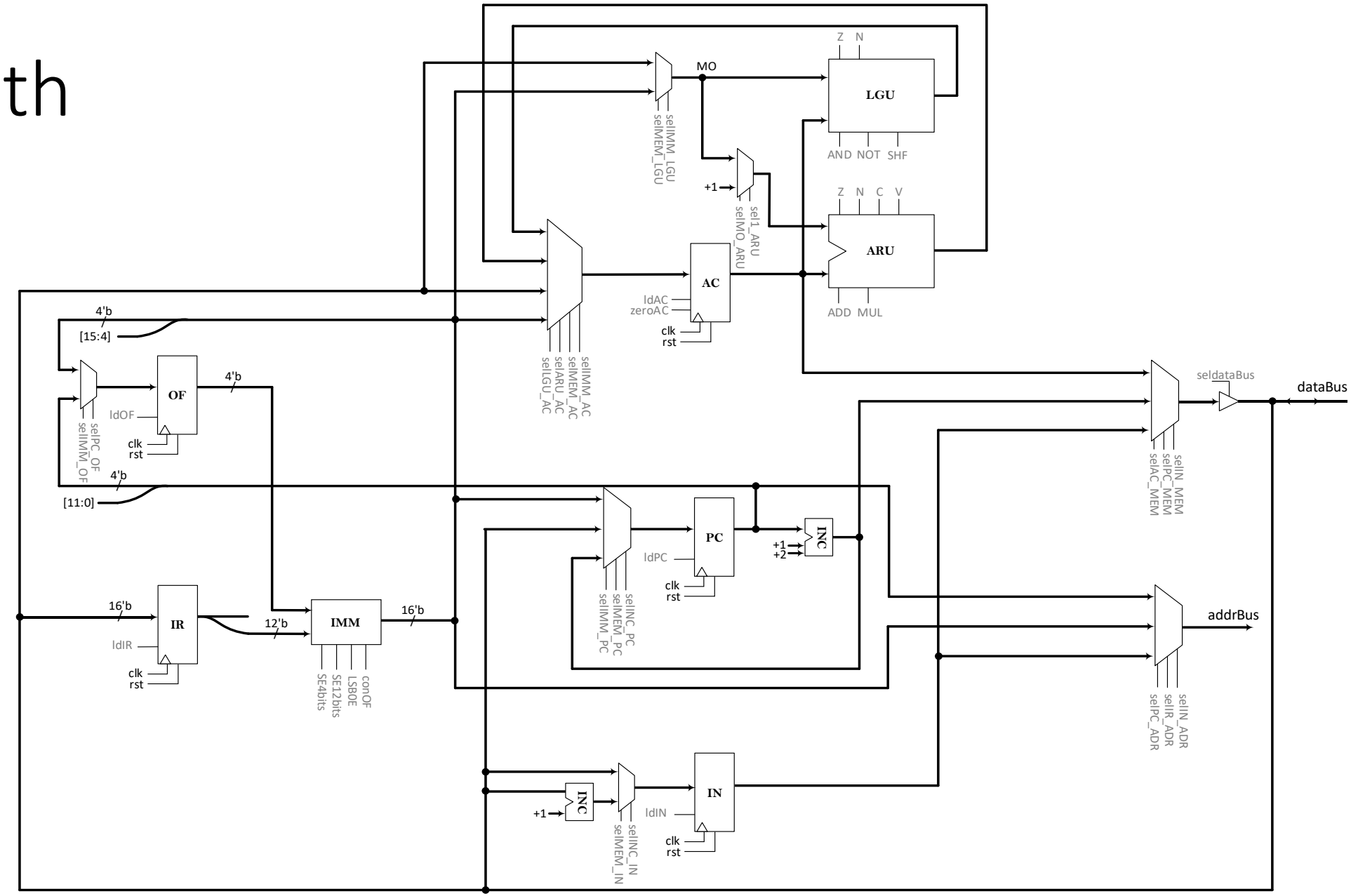
Instruction Type	Opcode	Instruction	Description
Full Address Instr.	0000	LDm	Load Accumulator Immediate
	0001	LDa	Load Accumulator Addressed
	0010	LDn	Load Accumulator Indirect
	0011	STa	Store Accumulator Addressed
	0100	STn	Store Accumulator Indirect
	0101	INa	Increment memory Address
	0110	ANm	AND Accumulator Immediate
	0111	ANa	AND Accumulator Addressed
	1000	ADm	Add Accumulator Immediate
	1001	ADa	Add Accumulator Addressed
	1010	ADn	Add Accumulator Indirect
	1011	MLa	Multiply Accumulator Addressed
	1100	JMa	Jump Addressed (unconditional)
	1101	JMn	Jump Indirect
	1110	JSR	Jump Sub-routine

Instruction Type	Opcode		Instruction	Description
No Address Instr.	1111	0000	00000000	LPO	Load PC to Offset register
			00000001	LOP	Load Offset register to PC
			00000010	ACZ	Accumulator Zero
			00000011	ACN	Accumulator NOT
			00000100	ACI	Accumulator Increment
		0001		LOm	Load Offset register Immediate
		0010		SRA	Shift Right Arithmetic
		0011		SRL	Shift Right Logical
		0100		SLL	Shift Left Logical
		0101		$SKP_{Z,N,C,V}$	Skip Zero, Negative, Carry, Overflow (obs, exp)
		0110		$SET_{Z,N,C,V}$	Set Zero, Negative, Carry, Overflow (enb, val)

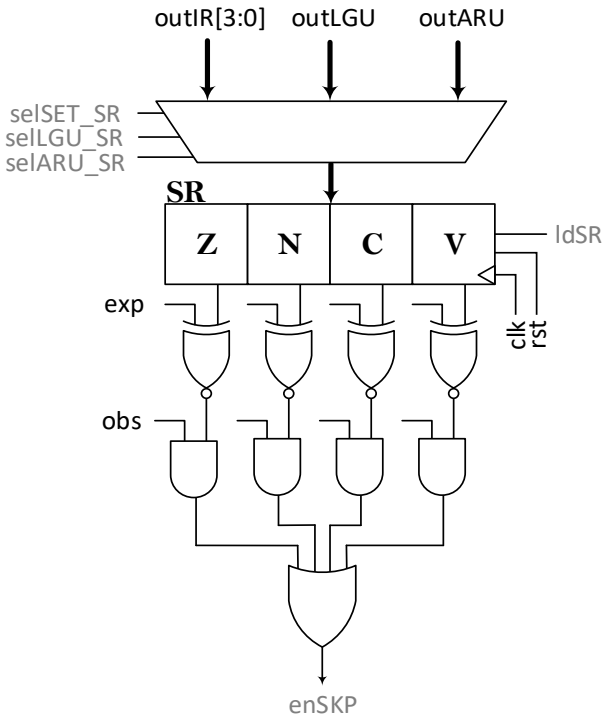
Top level


dataBus
16
addrBus
16
PUNEH
memReady
readMEM
writeMEM
clk
rst

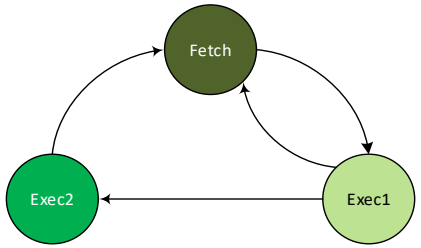
Datapath

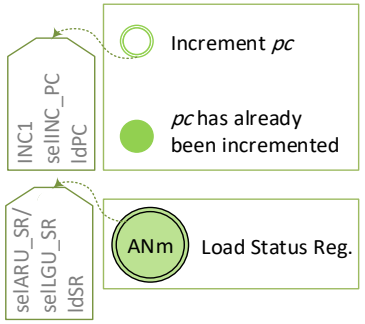

Z
N
MO
LGU
AND NOT SHF
selIMM_LGU
selMEM_LGU
+1
sel1_ARU
selMO_ARU
Z N C V
ARU
ADD MUL
AC
ldAC
zeroAC
clk
rst
selLGU_AC
selARU_AC
selMEM_AC
selIMM_AC
4'b
[15:4]
OF
ldOF
clk
rst
4'b
selIMM_OF
selPC_OF
4'b
[11:0]
seldataBus
dataBus
selIN_MEM
selPC_MEM
selAC_MEM
PC
ldPC
clk
rst
INC
+1
+2
selINC_PC
selMEM_PC
selIMM_PC
16'b
IR
ldIR
clk
rst
12'b
IMM
16'b
SE4bits
SE12bits
LSB0E
conOF
addrBus
selIN_ADR
selIR_ADR
selPC_ADR
INC
+1
IN
ldIN
clk
rst
selINC_IN
selMEM_IN

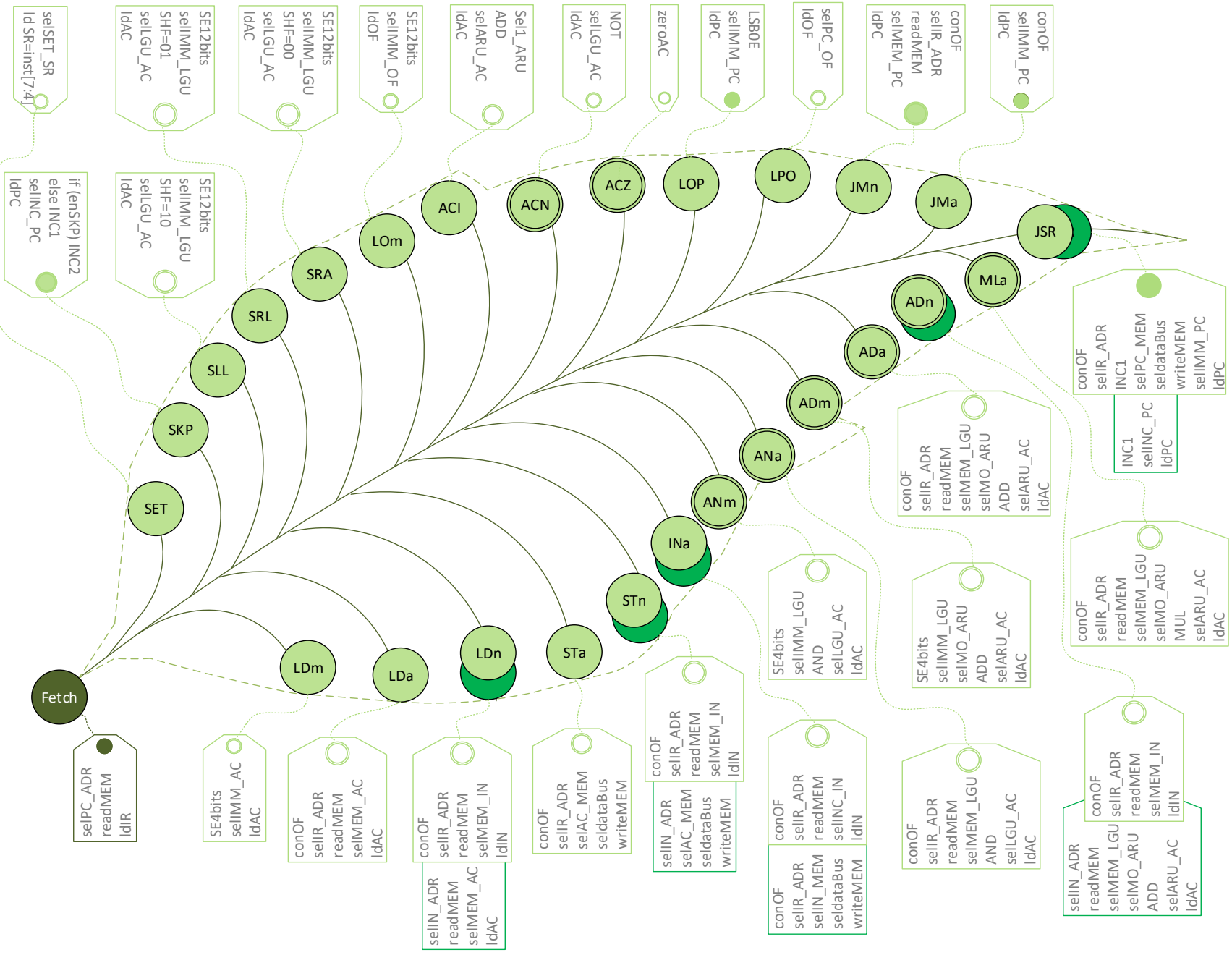
Flags


outIR[3:0]
outLGU
outARU
selSET_SR
selLGU_SR
selARU_SR
SR
Z
N
C
V
ldSR
exp
clk
rst
obs
enSKP

Controller


Fetch
Exec2
Exec1


INC1
selINC_PC
ldPC
Increment *pc*
pc has already been incremented
selARU_SR/
selLGU_SR
ldSR
ANm
Load Status Reg.


Fetch
SET
SKP
SLL
SRL
SRA
LOm
ACI
ACN
ACZ
LOP
LPO
JMn
JMa
JSR
MLa
ADn
ADa
ADm
ANa
ANm
INa
STn
STa
LDn
LDa
LDm
selSET_SR
ld SR=inst[7:4]
SE12bits
selIMM_LGU
SHF=01
selLGU_AC
ldAC
SE12bits
selIMM_LGU
SHF=00
selLGU_AC
ldAC
SE12bits
selIMM_OF
ldOF
Sel1_ARU
ADD
selARU_AC
ldAC
NOT
selLGU_AC
ldAC
zeroAC
LSBOE
selIMM_PC
ldPC
selPC_OF
ldOF
conOF
selIR_ADR
readMEM
selMEM_PC
ldPC
conOF
selIMM_PC
ldPC
if (enSKP) INC2
else INC1
selINC_PC
ldPC
SE12bits
selIMM_LGU
SHF=10
selLGU_AC
ldAC
selPC_ADR
readMEM
ldIR
SE4bits
selIMM_AC
ldAC
conOF
selIR_ADR
readMEM
selMEM_AC
ldAC
conOF
selIR_ADR
readMEM
selMEM_IN
ldIN
selIN_ADR
readMEM
selMEM_AC
ldAC
conOF
selIR_ADR
selAC_MEM
seldataBus
writeMEM
conOF
selIR_ADR
readMEM
selMEM_IN
ldIN
selIN_ADR
selAC_MEM
seldataBus
writeMEM
SE4bits
selIMM_LGU
AND
selLGU_AC
ldAC
conOF
selIR_ADR
readMEM
selINC_IN
ldIN
conOF
selIR_ADR
selIN_MEM
seldataBus
writeMEM
SE4bits
selIMM_LGU
selMO_ARU
ADD
selARU_AC
ldAC
conOF
selIR_ADR
readMEM
selMEM_LGU
AND
selLGU_AC
ldAC
conOF
selIR_ADR
readMEM
selMEM_LGU
selMO_ARU
ADD
selARU_AC
ldAC
conOF
selIR_ADR
readMEM
selMEM_LGU
selMO_ARU
selMO_ARU
ADD
selARU_AC
ldAC
conOF
selIR_ADR
INC1
selIPC_MEM
seldataBus
writeMEM
selIMM_PC
ldPC
INC1
selINC_PC
ldPC
conOF
selIR_ADR
readMEM
selMEM_LGU
selMO_ARU
MUL
selARU_AC
ldAC
conOF
selIR_ADR
readMEM
selMEM_IN
ldIN
selIN_ADR
readMEM
selMEM_LGU
selMO_ARU
ADD
selARU_AC
ldAC

Simulation Results