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C1L1-05 Software Design Guide

MD Electronic System Design Department 2005/12/26





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Rev. no	Date	page	Description
0.1	2005/10/24	all	New Release
0.2	2005/11/24	7	Remove Table 1.3
		11	Remove Table 1.6
		27	Remove Rigister
		36	Figure 2.7
0.3	2005/12/21		Add Section 3 3-Wire SPI Interface
		44	Modify VCOMH VOCML Value
0.4	2005/12/26	43	hex Start_X_Select
		44	hex Start_Y_Select
		46	hex Start_X_Select
			hex Start_Y_Select
		47	hex Partial_VCO_Select
		48	hex Start_X_Select





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1. CPU Interface Timing

1.1 Intel 8080-Series Interface Timing

1.1.1 Intel 8080-Series Interface Timing Characteristic

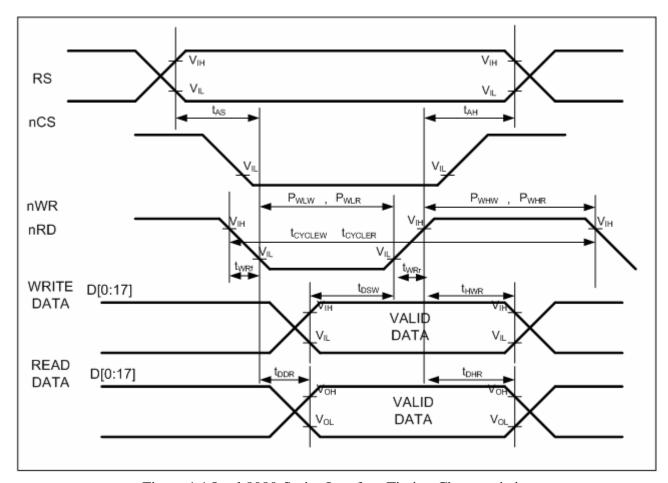


Figure 1.1 Intel 8080-Series Interface Timing Characteristic





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Table 1.1 18/16-Bit Intel 8080-Series Interface Timing Characteristic

18/16-Bit Interface: VDDIO=1.6 to 3.3 V

Item	Symbol	Min	Тур	Max	unit
Due avala tima	t _{CYCLEW}	150	_	_	ns
Bus cycle time	t _{CYCLER}	500	_	_	ns
nWD nDD nulse width low	P_{WLW}	40	_	_	ns
nWR_nRD pulse width low	P_{WLR}	250	_	_	ns
nWD nDD nulse width high	P_{WHW}	70	_	_	ns
nWR_nRD pulse width high	P _{WHR}	200			
Pulse rise/fall time	t _{WRr} , t _{WRf}	_	_	25	ns
Setup time(RS,nCS,nWR,nRD)	t _{AS}	10	_	_	ns
Hold time(RS,nCS,nWR,nRD)	t_{AH}	2	_	_	ns
Data setup time	$t_{ m DSW}$	25	_	_	ns
Data hold time	t _{HWR}	5	_	_	ns
Data output setup time	t _{DDR}	_	_	200	ns
Data output hold time	t _{DHR}	5	_	_	ns

Table 1.2 9/8-Bit Intel 8080-Series Interface Timing Characteristic-1

9/8-Bit Interface: VDDIO=1.6 to 3.3 V

Item	Symbol	Min	Тур	Max	unit
Due evele time	t _{CYCLEW}	100	_	_	ns
Bus cycle time	t _{CYCLER}	500	_	_	ns
nWD nDD nulsa width law	P_{WLW}	40	_	_	ns
nWR_nRD pulse width low	P _{WLR}	250	_	_	ns
nWD nDD nulso width high	P_{WHW}	50	_	_	ns
nWR_nRD pulse width high	P _{WHR}	200			
Pulse rise/fall time	t _{WRr} , t _{WRf}	_	_	25	ns
Setup time(RS,nCS,nWR,nRD)	t _{AS}	10	_	_	ns
Hold time(RS,nCS,nWR,nRD)	t _{AH}	2	_	_	ns
Data setup time	$t_{ m DSW}$	25	_	_	ns
Data hold time	t _{HWR}	5	_	_	ns
Data output setup time	t _{DDR}	-	_	100	ns
Data output hold time	t _{DHR}	5	_	_	ns





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1.1.2 The Type of Intel 8080-Series Interface Timing

The C1L1-05 can operate as host sends the different type of interface timing per the below figure.

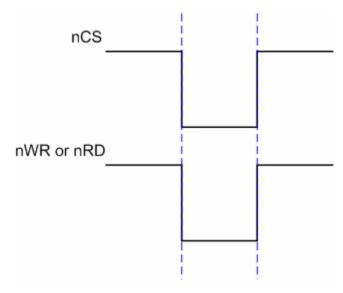


Figure 1.2 Type 1 of Intel 8080-Series Interface Timing

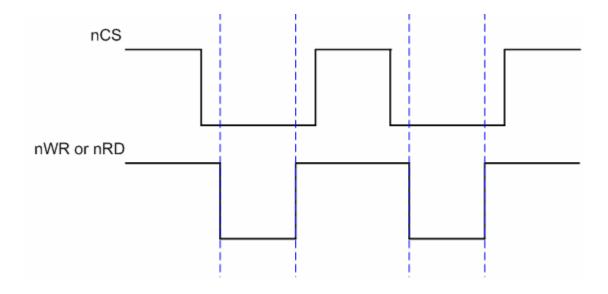


Figure 1.3-1 Type 2 of Intel 8080-Series Interface Timing





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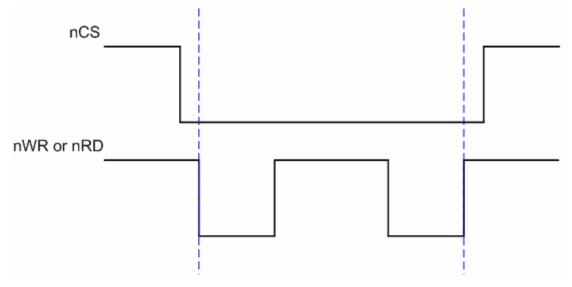


Figure 1.3-2 Type 2 of Intel 8080-Series Interface Timing

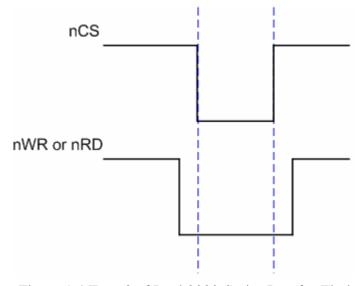


Figure 1.4 Type 3 of Intel 8080-Series Interfac Timing





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1.2 Motorola 6800-Series Interface Timing

1.2.1 Motorola 6800-Series Interface Timing Characteristic

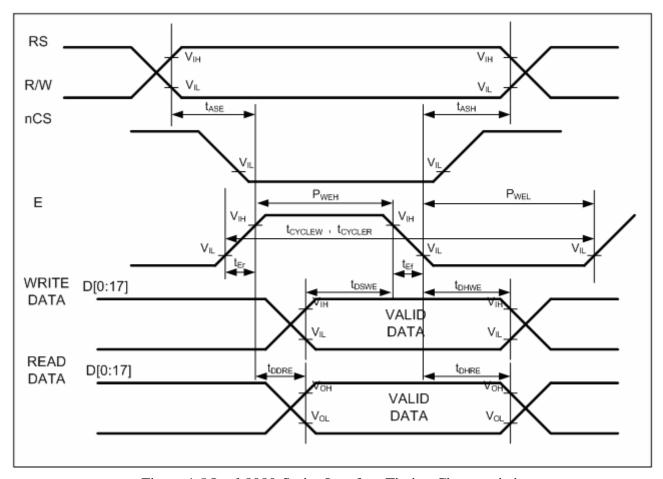


Figure 1.5 Intel 8080-Series Interface Timing Characteristic





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Table 1.3 18/16-Bit Motorola 6800-Series Interface Timing Characteristic

18/16-Bit Interface: VDDIO=1.6 to 3.3 V

Item		Symbol	Min	Typ	Max	unit
D1- 4'	write	t _{CYCLEW}	150	_	_	ns
Bus cycle time	read	t _{CYCLER}	500	_	_	ns
E mulas mildth land	write	-	40	_	_	ns
E pulse width low	read	$P_{ m WEL}$	250	_	_	ns
E pulse width high	write	D	70	_	_	ns
	read	P_{WEH}	200			
E Pulse rise/fall time		t_{Er}, t_{Ef}	_	_	25	ns
Setup time(RS,nCS,E,R/W)		t _{ASE}	10	_	_	ns
Hold time(RS,nCS,E,R/W)		t _{ASH}	2	_	_	ns
Data setup time		t _{DSWE}	25	_	_	ns
Data hold time		t _{DHWE}	5	_	_	ns
Data output setup time		t _{DDR}	_	_	200	ns
Data output hold time		t _{DHR}	5	_	_	ns

Table 1.4 9/8-Bit Motorola 6800-Series Interface Timing Characteristic-1

9/8-Bit Interface: VDDIO=1.6 to 3.3 V

Item		Symbol	Min	Тур	Max	unit
Due avale time	write	t _{CYCLEW}	100	_	_	ns
Bus cycle time	read	t _{CYCLER}	500	_	_	ns
E mula a suidth lass	write	D	40	_	_	ns
E pulse width low	read	$P_{ m WEL}$	250	_	_	ns
E mula a width high	write	D	50	_	_	ns
E pulse width high	read	P_{WEH}	200			
E Pulse rise/fall time		t_{Er}, t_{Ef}	_	_	25	ns
Setup time(RS,nCS,E,R/W)		t _{ASE}	10	_	_	ns
Hold time(RS,nCS,E,R/W)		t _{ASH}	2	_	_	ns
Data setup time		t _{DSWE}	25	_	_	ns
Data hold time		t _{DHWE}	5	_	_	ns
Data output setup time		t _{DDR}	_	_	200	ns
Data output hold time		t _{DHR}	5	_	_	ns

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1.2.2 The Type of Motorola 6800-Series Interface Timing

The C1L1-05 can operate as host sends the different type of interface timing per the below figure.

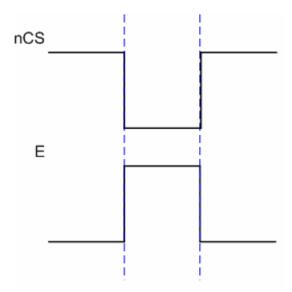


Figure 1.6 Type 1 of Motorola 6800-Series Interface Timing

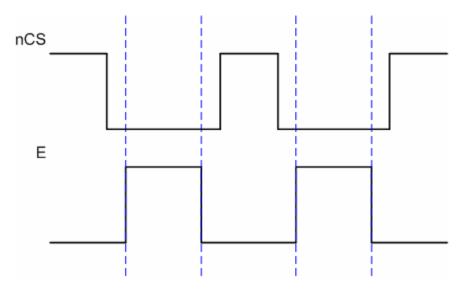


Figure 1.7-1 Type 2 of Motorola 6800-Series Interface Timing





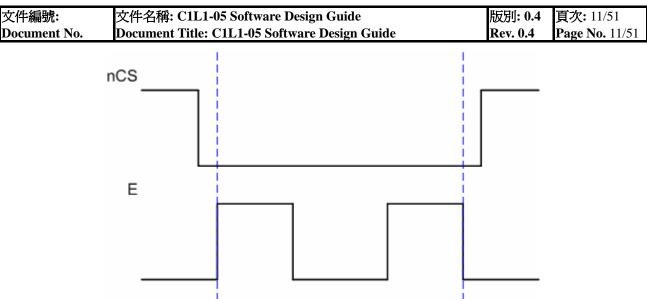


Figure 1.7-2 Type 2 of Motorola 6800-Series Interface Timing

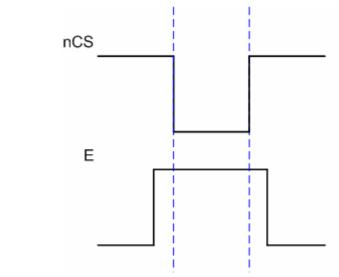


Figure 1.8 Type 3 of Motorola 6800-Series Interface Timing





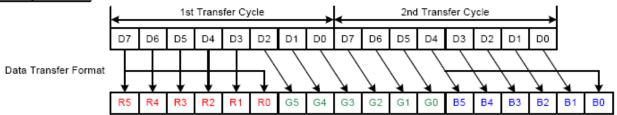
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1.3 Input DATA Mapping

1.3.1 8-Bit Mode

8-Bit Bus Width CPU interface

Memory Access:



Register Access:

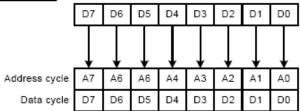
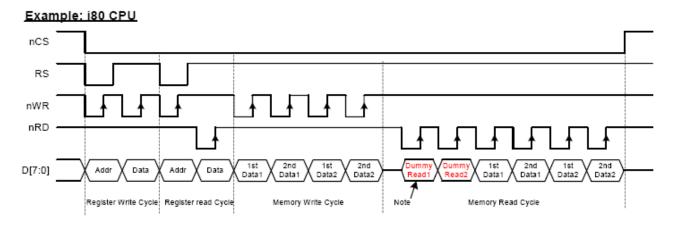


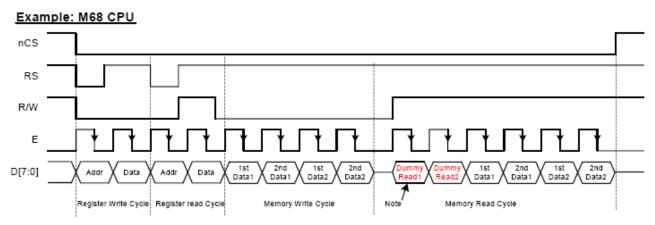
Figure 1.9 DATA Mapping of 8-Bit Mode





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Note:

- Since the content of memory is latch into output buffer first, the dummy read operation is necessary to let the latch data send to the output bus when the write cycle is changed to read cycle.
- 2, The content of address counter increases automatically based on the interface configuration.

Figure 1.10 Transfer Timing of 8-Bit Mode



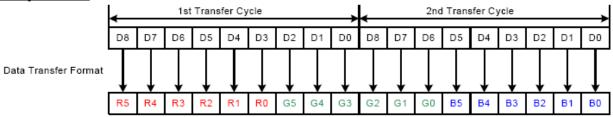


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1.3.2 9-Bit Mode

9-Bit Bus Width CPU interface

Memory Access:



Register Access:

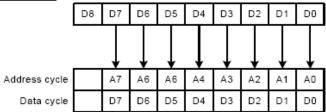
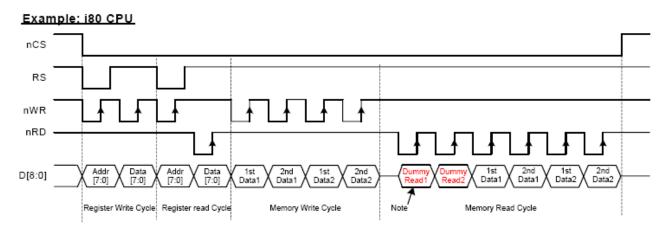


Figure 1.11 DATA Mapping of 9-Bit Mode





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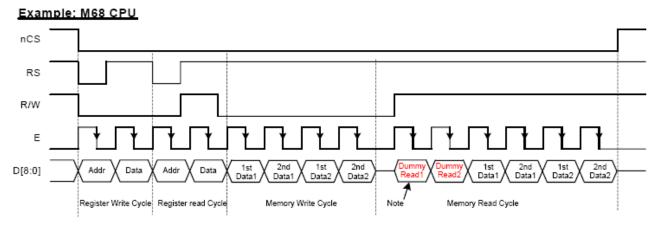


Figure 1.12 Transfer Timing of 9-Bit Mod





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1.3.3 16-Bit Mode

16-Bit Bus Width CPU interface

Memory Access:

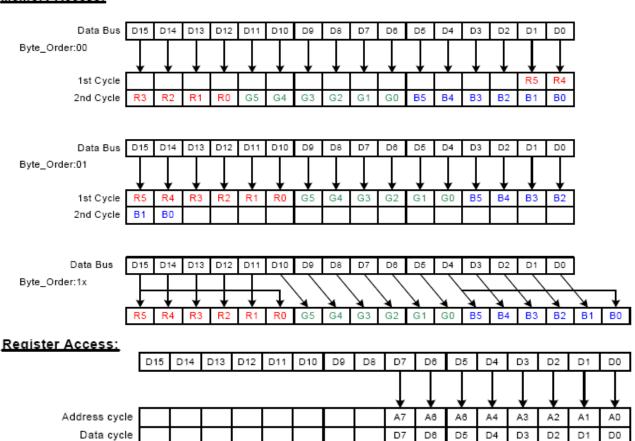


Figure 1.13 DATA Mapping of 16-Bit Mode







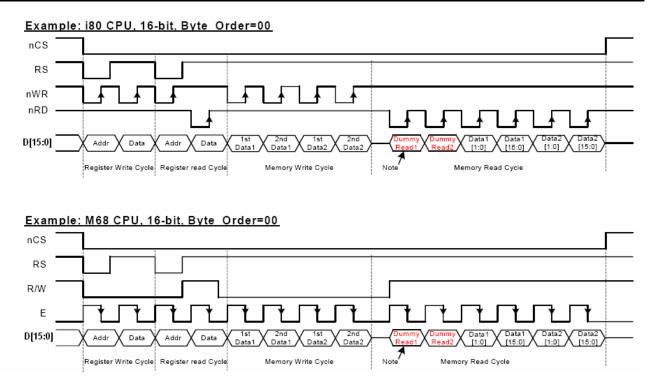


Figure 1.14 Transfer Timing of 16-Bit Mode BODR00

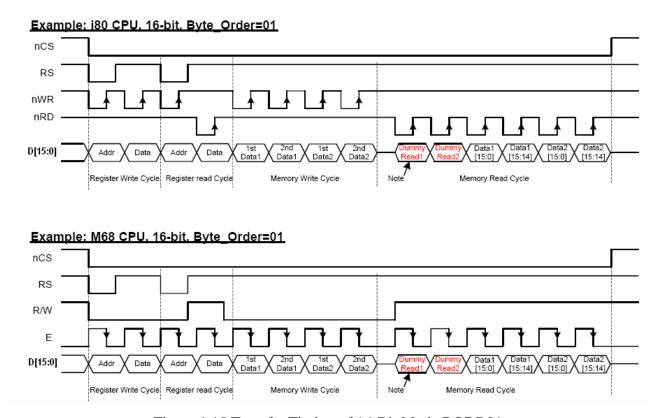


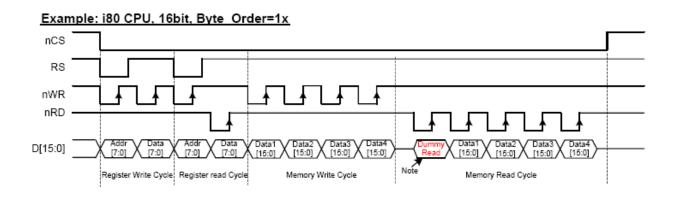
Figure 1.15 Transfer Timing of 16-Bit Mode BODR01

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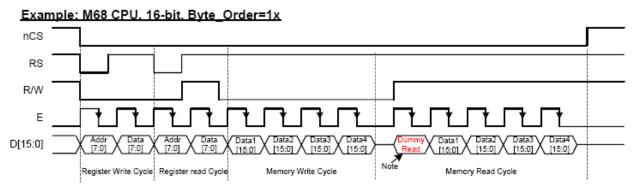


Figure 1.16 Transfer Timing of 16-Bit Mode BODR1x

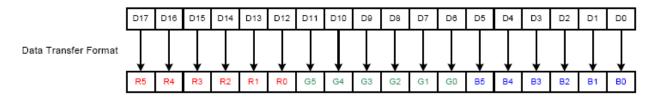




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1.3.4 18-Bit Mode

Memory Access:



Register Access:

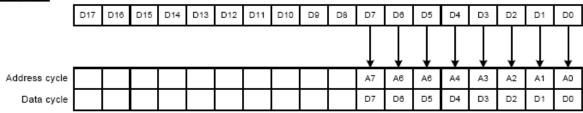
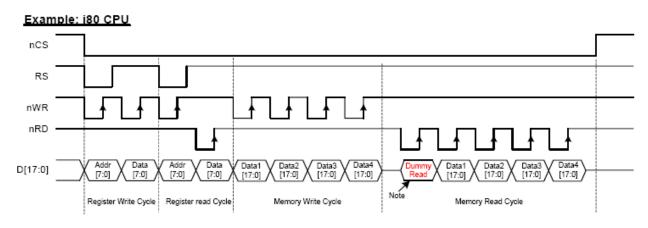


Figure 1.17 DATA Mapping of 18-Bit Mode





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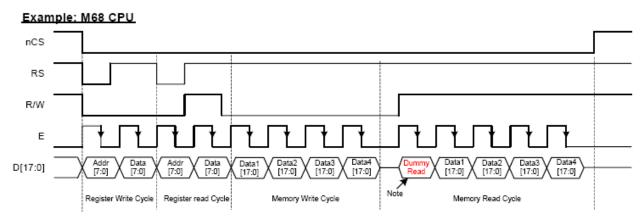


Figure 1.18 Transfer Timing of 18-Bit Mode





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2. Register Table

Table 2.1 C1L1-05 Register Table

Address	Register/	Reset	2.1 C1L1-05 Register Table	Comment
Auuress	Bit Name	Value	Meaning	Comment
	CHIPID		[7:3]: REVID (read only)	
		0000 1001	[2:0]: CHIPID (read only)	
0x00			000:TP078	
UAUU			001:TP077	
			010:TP079	
	MODE_SEL1	0000 0010	[7:6]: Panel resolution select	
	MODE_SEL1	0000-0010	00: 128 x 160 (Default)	
			01: 128 x 128	
			10 : 96 x 96	
			11 : 132 x 160	
			[5]: Vcom output mask on non-partial area in partial	
			mode	
			0: Normal (unmask) (Default)	
			1: Vcom output mask	
			[4:2]: display mode	
0x01			000: 16/18 bit color	
UAUI			001: 16/18 bit color + partial	
			010: 8 color	
			011: 8 color + partial	
			100: 8color + dithering 101: 8 color + dithering + partial	
			[1]: SLP: sleep mode	
			0: sleep	
			1: normal(Default)	
			[0]: Out of range data control:	
			0: White (Default)	
			1 : Black	
	MODE_SEL2	0001-0010	[7:6]: Scan direction	
	WIODE_SEE2	0001 0010	[7] 0 : CSV=1(V normal scan) (Default)	
			1 : CSV=0 (V reverse scan)	
			` '	
			[6] 0 : CSH=1(H normal scan) (Default)	
			1 : CSH=0(H reverse scan) [5]: Line or frame inversion driving select	
			0: Line inversion (Default);	
			1 : Frame inversion	
0x02			[4]: STV2 signal output	
UAUZ			0: STV2 output	
			1 : STV2 NO output(Default)	
			[3]: STV1 signal output	
			0: STV1 output (Default)	
			1 : STV1 NO output	
			[2:1]: Non-partial area data output control	
			00 : GND output	
			01 : Vcom output(Default)	
			or . Voin output(Delault)	





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			1x : Hi-Z	
			[0]: Non-partial area CKH1/2/3 output control	
			0: CKH1/2/3 output = "Low" (Default)	
			1 : CKH1/2/3 output = "High"	
	MODE_SEL3	0000-xxxx	[7:6]: Input data selection	Note1
	117022_0220		00 : 8 bit mode (Default)	1,000
			01 : 16 bit mode	
			10 : 9 bit mode	
			11 : 18 bit mode	
0x03			[5:4]: BODR : 16 bit data access control	
UXUS				
			00: 1 st cycle transfer only 2 bit data and 2nd	
			cycle transfer 16 bit data (Default)	
			01 : 1 st cycle transfer 16 bit data and 2nd	
			cycle transfer only 2 bit data	
			1x : Transfer 16 bit data (R:G:B = 5:6:5)	
	MODE_SEL4	0000-xxxx	[7]: RGB interface mode selection	Only for
			0 : DE(Default)	Parallel
			1: VS + HS	RGB
			[6]: SYNC polarity 0: Negative(Default)	Mode
			1 : Positive	
0x04			[5]: Input data mapping selection	Bit 5 for
			0: 18 bits(Default) (R : G : B = 6:6:6)	SPI Mode
			1:16 bits (R:G: $B = 5:6:5$)	
			[4]: Input mode selection	
			0 : moving mode(Default)	
			1 : still mode	
	VCO_Mode	x000-1000	[4:3]: VCO bias mode select	
			00:-5%	
			01 : typical (Default) 10 : +5%	
			11:+10%	
			[5], [2:0]: VCO frequency	
			0,000:1.82 MHz (Default)	
0x05			$1,000:1.82 \times 3/4$ MHz	
			0,001:1.82/2 MHz	
			0,010:1.5 MHz	
			1,010:1.5 \times 3/4 MHz	
			0,011:1.5/2 MHz	
			0,100:0.9 MHz	
			1,100:0.9 × 3/4 MHz	
	DAC OD CTD	1000 0101	0 , 101 : 0.9 / 2 MHz [[7]: DC/DC Vpower on signal select	
	DAC_OP_CTR	1000-0101	0: Input pin PWDN	
	L2		1 : Internal register ([6]) (Default)	
0.00			[6]: int_PWDN : DC/DC power on signal	
0x06			0 : AVDD1 AVDD2 power off(Default)	
			1 : AVDD1 AVDD2power on	
			[5:4]: DAC bias select	
			00:100% (Default)	
	J	<u> </u>	UU. 10070 (Detault)	





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	•		<u> </u>	ge 1 (01 23/31
			01:80%	
			10:60%	
			11:50%	
			[3:2]: Vcom bias select	
			00 : -20% × normal	
			01 : normal (Default)	
			10 : 20% × normal	
			11:40% × normal	
			[1:0]: RGB loading select	
			00 : 5p 01 : 10.5p (Default)	
			10:15p	
			11:20p	
	VCOMH CTRL	x111-0100	[6:0]: VCOM_H output Voltage control	Note 2
0x07	V COMIT_CTRE	XIII 0100	step = $2.1 \text{V}/128 = 0.0164 \text{V}$ (Default =	11010 2
02407			4.0V)	
			(VCOM_H=2.1V in settting x000-0001)	
	VCOMI, CTRI	x000-1100	[6:0]: VCOM_L output Voltage control	Note 2
	VCOME_CTRE	X000 1100	step = $2.1 \text{V}/128 = 0.0164 \text{V}$ (Default =	11010 2
0x08			0.197V)	
			(VCOM_L=0V in setting x000-0000)	
SRAM c	ontrol		(VCOM_L=0 V in setting x000 0000)	
0x09	PWS-X	0000-0000	[7:0]: Write SRAM window start X point	Note3
0x10	PWS-Y		[7:0]: Write SRAM window start Y point	Note3
0x10 0x11	PWE-X		[7:0]: Write SRAM window start 1 point	Note3
$0x11 \\ 0x12$	PWE-Y		[7:0]: Write SRAM window end Y point	Note3
$0x12 \\ 0x14$	PDS-Y		[7:0]: Partial Display start Y point	Note4
0x14 0x16	PDE-Y		[7:0]: Partial Display start 1 point	Note4
UXIU	SRAM _Control			Note 4
	SIXAW _CONTO	XXXX-0000	[3]: If X or Y position is set over range,	
			0 : Ineffective writing. X or Y position are not changed. (Default)	
			[2]: ACX (SRAM X Address Counter)	
			0: SRAM X position + 1 (Default)	
017			1: SRAM X position – 1	NI a 4 a F
0x17			[1]: ACY (SRAM Y Address Counter)	Note5
			0: SRAM Y position + 1 (Default)	
			1: SRAM Y position –1	
			[0]: ACXY (SRAM access control)	
			0 : add X position first then add Y position	
			(Default)	
	CDAM D ''	0000 0000	1 : add Y position first then add X position	
0x18	SRAM_Position	0000-0000	[7:0]: SRAM X position $0 \le X \le 0x83$	Note6
	_X	0000 0000		
0x19	SRAM_Position	0000-0000	[7:0]: SRAM Y position $0 \le Y \le 0x9F$	Note6
	_Y			





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0x1A	Th	0001-0010	[7:0]: t _{Hds} (min to max) : 1clk / step [0 ~ 255]	Only for Parallel RGB Mode
0x1B	Tv	xxx0-0110	[4:0]: t _{Vds} (min to max) : 1t _H / step [0~31]	Only for Parallel RGB Mode
			Gamma voltage adjustable level	
0x21	Gamma adjust 1	1000-1000	[7:4]: PV0 [3:0]: NV0	
0x22	Gamma adjust 2	0011-0011	[7:4]: PV1 [3:0]: NV1	
0x23	Gamma adjust 3	0111-0111		
0x24	Gamma adjust 4	0111-0111		
0x25	Gamma adjust 5	0110-0110		
0x26	Gamma adjust 6	0110-0110		
0x27	Gamma adjust 7	0100-0100		
0x28	Gamma adjust 8	0011-0011		
0x29	Gamma adjust 9	0010-0010		
0x3f	EB		[3]: Engineering table register control enable bit 0: disable access register address 0x40 – 0xFF 1: enable access register address 0x40 – 0xFF	
		I	Engineering Timing setup table	
0x40	Reserve	xxxx-xxxx		
0x41	CK_P	xx10-0000	[5:0]: CKH3/CKH2/CKH1 pulse width, 1 clk / step	
0x42	CK3_CK2	xx00-1010	[5:0] CKH3_CKH2/ CKH2_CKH1, 1 clk / step	
0x43	EC		[5:0] : ENBV_CKH3, 1 clk / step	
0x44	EL		[5:0]: ENBV_L, 1 clk /step.	
0x45	PC	xx00-1000	[5:0]: PCG_CKH3, 1 clk / step	
0x46	PH	xx00-0101	[5:0] : PCG_H, 1 clk /step.	
0x47	FC		[5:0]: VCOM_CKH3, 1 clk / step	
0x48	SC	xx01-0011	[5:0] : STV_CKH3, 1 clk / step	





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0x49	CV_CH	xx00-1110	[5:0] : CKV_CKH3, 1 clk / step	
	Cd	xxx0-1000	[4]: CKV1/CKV2 inversion	
			0 : normal	
			1: inversion	
0x4A			[3:1] : CKV_d, 1H/step	
			[0]: mask bit (Blanking mask)	
			0 : ON(mask display) 1 : OFF (normal	
			display)	
0x4B	Sd	xx01-0011	[5:3] : STV_disp, 1 H / step.	
UX4D			[2:0]: RGB data adjustment	





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Note 1: Please refer to section 1.3.

Note 2: The below table is showed the VCOMH and VCOML voltage mapping to register step setting.

Table 2.2 VCOMH VCOML step setting

(Decimal) (Decimal) 127 4.184 127 2.084 126 4.167 126 2.067 125 4.151 125 2.051 124 4.134 124 2.034 123 4.118 123 2.018 122 4.102 122 2.002 121 4.085 121 1.985 120 4.069 120 1.969 119 4.052 119 1.952 118 4.036 118 1.936 117 4.020 117 1.920 116 4.003 116 1.903 115 3.987 115 1.887 114 3.970 114 1.870 24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 21 2.428	Digital Input	VCOMH Output (V)	Digital Input	VCOML Output (V)
127	(Decimal)	VCOMII Output (V)		VCOME Output (V)
126		A 18A		2 084
125 4.151 125 2.051 124 4.134 124 2.034 123 4.118 123 2.018 122 4.102 122 2.002 121 4.085 121 1.985 120 4.069 120 1.969 119 4.052 119 1.952 118 4.036 118 1.936 117 4.020 117 1.920 116 4.003 116 1.903 115 3.987 115 1.887 114 3.970 114 1.870 24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 20 2.428 20 0.328 19 2.412 19 0.312 18 2.395 18 0.295 17 </td <td></td> <td></td> <td></td> <td></td>				
124 4.134 124 2.034 123 4.118 123 2.018 122 4.102 122 2.002 121 4.085 121 1.985 120 4.069 120 1.969 119 4.052 119 1.952 118 4.036 118 1.936 117 4.020 117 1.920 116 4.003 116 1.903 115 3.987 115 1.887 114 3.970 114 1.870 24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 20 2.428 20 0.328 19 2.412 19 0.312 18 2.395 18 0.295 17 2.379 17 0.279 16 <td></td> <td></td> <td></td> <td></td>				
123 4.118 123 2.018 122 4.102 122 2.002 121 4.085 121 1.985 120 4.069 120 1.969 119 4.052 119 1.952 118 4.036 118 1.936 117 4.020 117 1.920 116 4.003 116 1.903 115 3.987 115 1.887 114 3.970 114 1.870 24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 20 2.428 20 0.328 19 2.412 19 0.312 18 2.395 18 0.295 17 2.379 17 0.279 16 2.363 16 0.263 15				
122 4.102 122 2.002 121 4.085 121 1.985 120 4.069 120 1.969 119 4.052 119 1.952 118 4.036 118 1.936 117 4.020 117 1.920 116 4.003 116 1.903 115 3.987 115 1.887 114 3.970 114 1.870 24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 20 2.428 20 0.328 19 2.412 19 0.312 18 2.395 18 0.295 17 2.379 17 0.279 16 2.363 16 0.263 15 2.346 15 0.246 14				
121 4.085 121 1.985 120 4.069 120 1.969 119 4.052 119 1.952 118 4.036 118 1.936 117 4.020 117 1.920 116 4.003 116 1.903 115 3.987 115 1.887 114 3.970 114 1.870 24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 20 2.428 20 0.328 19 2.412 19 0.312 18 2.395 18 0.295 17 2.379 17 0.279 16 2.363 16 0.263 15 2.346 15 0.246 14 2.330 14 0.230 13				
120 4.069 120 1.969 119 4.052 119 1.952 118 4.036 118 1.936 117 4.020 117 1.920 116 4.003 116 1.903 115 3.987 115 1.887 114 3.970 114 1.870 24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 20 2.428 20 0.328 19 2.412 19 0.312 18 2.395 18 0.295 17 2.379 17 0.279 16 2.363 16 0.263 15 2.346 15 0.246 14 2.330 14 0.230 13 2.313 13 0.213 12				
119 4.052 119 1.952 118 4.036 118 1.936 117 4.020 117 1.920 116 4.003 116 1.903 115 3.987 115 1.887 114 3.970 114 1.870 24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 20 2.428 20 0.328 19 2.412 19 0.312 18 2.395 18 0.295 17 2.379 17 0.279 16 2.363 16 0.263 15 2.346 15 0.246 14 2.330 14 0.230 13 2.313 13 0.213 12 2.297 12 0.197 11				
118 4.036 118 1.936 117 4.020 117 1.920 116 4.003 116 1.903 115 3.987 115 1.887 114 3.970 114 1.870 24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 20 2.428 20 0.328 19 2.412 19 0.312 18 2.395 18 0.295 17 2.379 17 0.279 16 2.363 16 0.263 15 2.346 15 0.246 14 2.330 14 0.230 13 2.313 13 0.213 12 2.297 12 0.197 11 2.280 11 0.180 10 <t< td=""><td></td><td></td><td></td><td></td></t<>				
117 4.020 117 1.920 116 4.003 116 1.903 115 3.987 115 1.887 114 3.970 114 1.870 24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 20 2.428 20 0.328 19 2.412 19 0.312 18 2.395 18 0.295 17 2.379 17 0.279 16 2.363 16 0.263 15 2.346 15 0.246 14 2.330 14 0.230 13 2.313 13 0.213 12 2.297 12 0.197 11 2.280 11 0.180 10 2.248 9 0.148 8 2.				
116 4.003 116 1.903 115 3.987 115 1.887 114 3.970 114 1.870 24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 20 2.428 20 0.328 19 2.412 19 0.312 18 2.395 18 0.295 17 2.379 17 0.279 16 2.363 16 0.263 15 2.346 15 0.246 14 2.330 14 0.230 13 2.313 13 0.213 12 2.297 12 0.197 11 2.280 11 0.180 10 2.264 10 0.164 9 2.248 9 0.148 8 2.231				
115 3.987 115 1.887 114 3.970 114 1.870 24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 20 2.428 20 0.328 19 2.412 19 0.312 18 2.395 18 0.295 17 2.379 17 0.279 16 2.363 16 0.263 15 2.346 15 0.246 14 2.330 14 0.230 13 2.313 13 0.213 12 2.297 12 0.197 11 2.280 11 0.180 10 2.264 10 0.164 9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 <td></td> <td></td> <td></td> <td></td>				
114 3.970 114 1.870 24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 20 2.428 20 0.328 19 2.412 19 0.312 18 2.395 18 0.295 17 2.379 17 0.279 16 2.363 16 0.263 15 2.346 15 0.246 14 2.330 14 0.230 13 2.313 13 0.213 12 2.297 12 0.197 11 2.280 11 0.180 10 2.264 10 0.164 9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 7 0.115 6 2.198				
24 2.494 24 0.394 23 2.477 23 0.377 22 2.461 22 0.361 21 2.445 21 0.345 20 2.428 20 0.328 19 2.412 19 0.312 18 2.395 18 0.295 17 2.379 17 0.279 16 2.363 16 0.263 15 2.346 15 0.246 14 2.330 14 0.230 13 2.313 13 0.213 12 2.297 12 0.197 11 2.280 11 0.180 10 2.264 10 0.164 9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 7 0.115 6 2.198 6 0.098 5 2.182				
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18 2.395 18 0.295 17 2.379 17 0.279 16 2.363 16 0.263 15 2.346 15 0.246 14 2.330 14 0.230 13 2.313 13 0.213 12 2.297 12 0.197 11 2.280 11 0.180 10 2.264 10 0.164 9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 7 0.115 6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066				
17 2.379 17 0.279 16 2.363 16 0.263 15 2.346 15 0.246 14 2.330 14 0.230 13 2.313 13 0.213 12 2.297 12 0.197 11 2.280 11 0.180 10 2.264 10 0.164 9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 7 0.115 6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066				
16 2.363 16 0.263 15 2.346 15 0.246 14 2.330 14 0.230 13 2.313 13 0.213 12 2.297 12 0.197 11 2.280 11 0.180 10 2.264 10 0.164 9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 7 0.115 6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066				
15 2.346 15 0.246 14 2.330 14 0.230 13 2.313 13 0.213 12 2.297 12 0.197 11 2.280 11 0.180 10 2.264 10 0.164 9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 7 0.115 6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066	17		17	
14 2.330 14 0.230 13 2.313 13 0.213 12 2.297 12 0.197 11 2.280 11 0.180 10 2.264 10 0.164 9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 7 0.115 6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066	16	2.363	16	0.263
13 2.313 13 0.213 12 2.297 12 0.197 11 2.280 11 0.180 10 2.264 10 0.164 9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 7 0.115 6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066	15	2.346	15	0.246
13 2.313 13 0.213 12 2.297 12 0.197 11 2.280 11 0.180 10 2.264 10 0.164 9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 7 0.115 6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066	14	2.330	14	0.230
11 2.280 11 0.180 10 2.264 10 0.164 9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 7 0.115 6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066	13		13	0.213
10 2.264 10 0.164 9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 7 0.115 6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066	12	2.297	12	0.197
10 2.264 10 0.164 9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 7 0.115 6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066	11	2.280	11	0.180
9 2.248 9 0.148 8 2.231 8 0.131 7 2.215 7 0.115 6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066				
8 2.231 8 0.131 7 2.215 7 0.115 6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066		2.248		
7 2.215 7 0.115 6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066				
6 2.198 6 0.098 5 2.182 5 0.082 4 2.166 4 0.066				
5 2.182 5 0.082 4 2.166 4 0.066				
4 2.166 4 0.066				
1 3 2.149 3 0.049	3	2.149	3	0.049
2 2.133 2 0.033	2			
1 2.100 1 0.016				





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Note3: The window size of SRAM setting is due to different resolution. The below list of register value is aimed at different panel resolution.

a. Register 0x01[7:6]=00, Resolution 128x160Register PWS-X(0x09h)=0x00hRegister PWS-Y(0x10h)=0x00hRegister PWE-X(0x11h)=0x7Fh

Register PWE-Y(0x12h)=0x9Fh

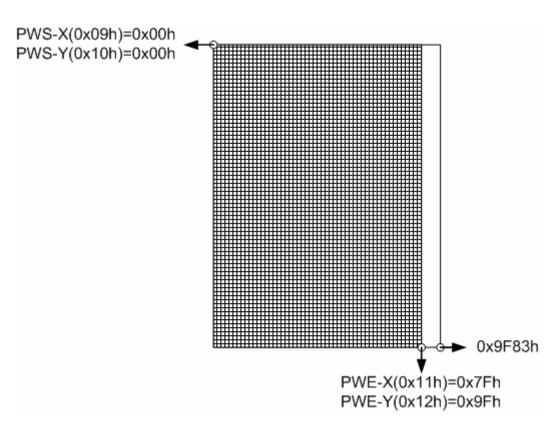


Figure 2.1 128x160 Window Size





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b. Register 0x01[7:6]=01 , Resolution 128x128

Register PWS-X(0x09h)=0x00h

Register PWS-Y(0x10h)=0x00h

Register PWE-X(0x11h)=0x7Fh

Register PWE-Y(0x12h)=0x7Fh

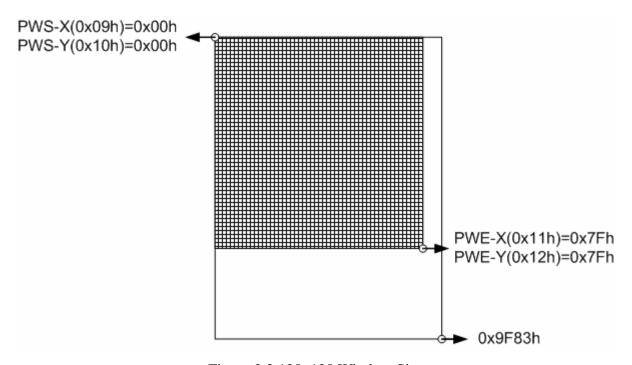


Figure 2.2 128x128 Window Size





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c. Register 0x01[7:6]=10 , Resolution 96x96

Register PWS-X(0x09h)=0x00h

Register PWS-Y(0x10h)=0x00h

Register PWE-X(0x11h)=0x5Fh

Register PWE-Y(0x12h)=0x5Fh

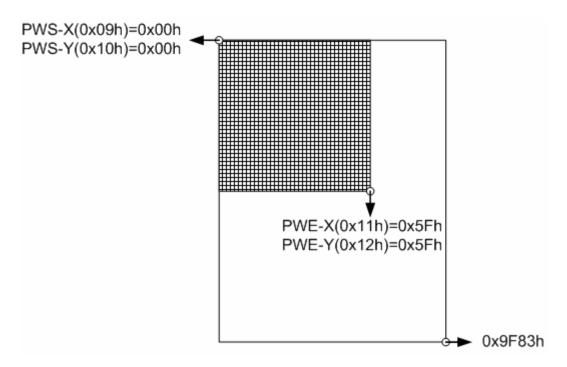


Figure 2.3 96x96 Window Size





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c. Register 0x01[7:6]=11 , Resolution 132x160

Register PWS-X(0x09h)=0x00h

Register PWS-Y(0x10h)=0x00h

Register PWE-X(0x11h)=0x83h

Register PWE-Y(0x12h)=0x9Fh

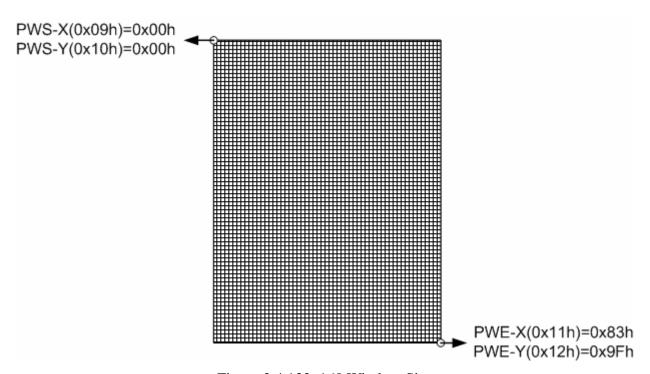


Figure 2.4 132x160 Window Size





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Note4: The register defines the partial mode's display area. PDS-Y(0x14h) set the start line of display area and PDE-Y(0x16h) set the end line of display area.

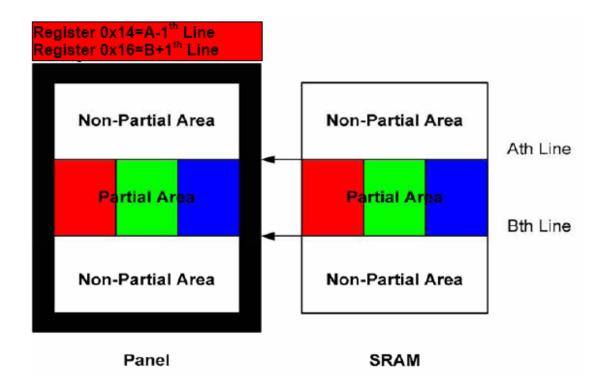


Figure 2.5 Partial Display Area





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Note5: The register defines read and write scanning direction of memory. The scanning direction refer to below figure.

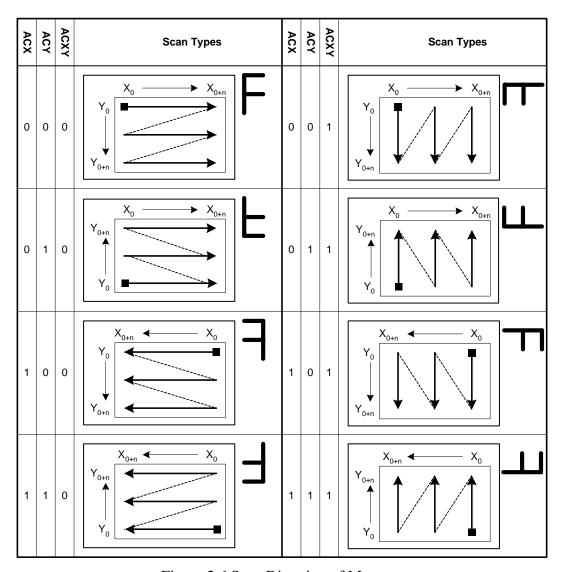


Figure 2.6 Scan Direction of Memory





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Note6:

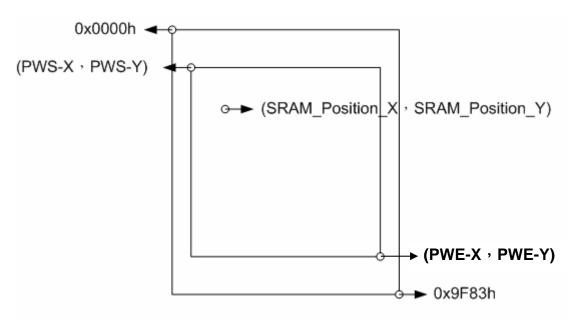


Figure 2.7 Start Point of SRAM





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3. 3-Wire SPI Interface

3.1 3-Wire SPI Interface Timing

C1L1-05 provides SPI interface to read/write registers and write the display memory. When writing the registers, the input data of SDI is latched on the rising edge of SCK; reading the register data, the system can latch output data on the rising edge of SCK. The transfer method is showed as below figure.

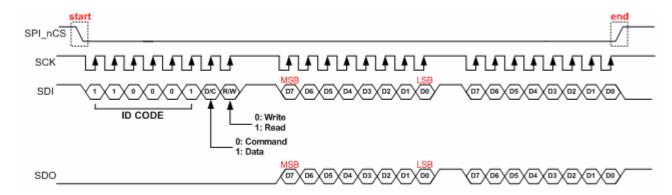


Figure 3.1 SPI transfer method from hosts to C1L1-05

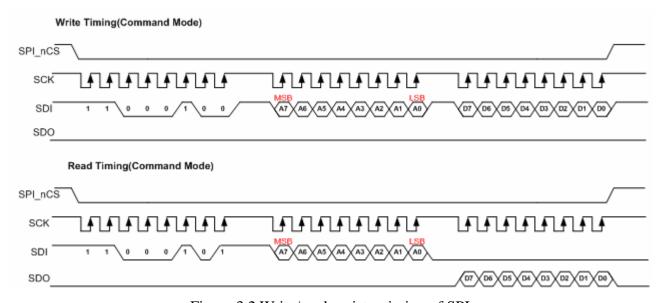


Figure 3.2 Write/read register timing of SPI





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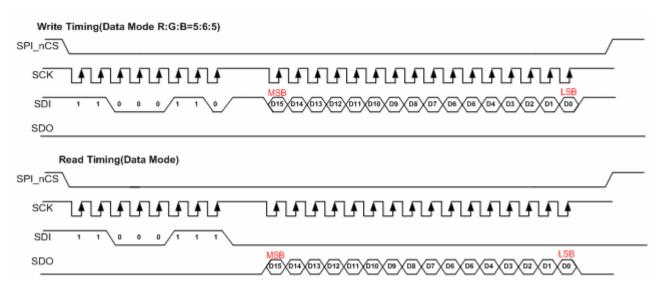


Figure 3.3 Write/read SRAM timing of SPI -1

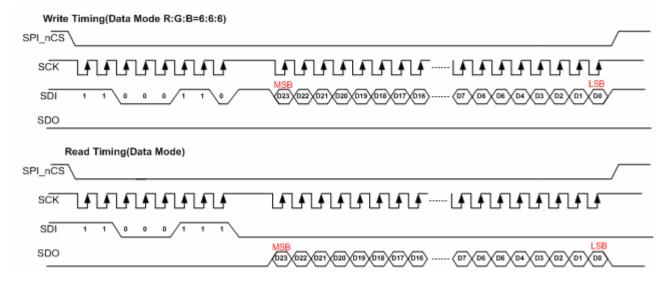


Figure 3.4 Write/read SRAM timing of SPI -2

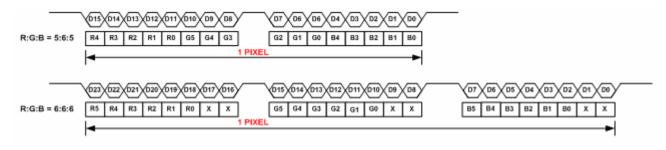


Figure 3.5 Data transfer format

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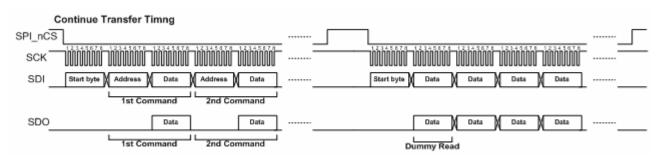


Figure 3.6 Continue transfer timing





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3.2 3-Wire SPI Interface Characteristic

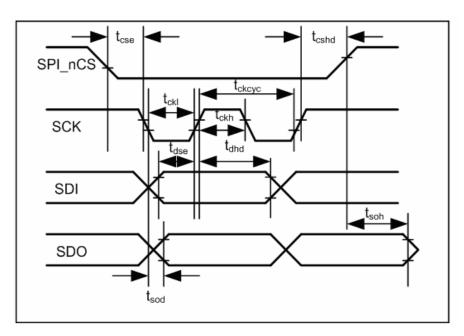


Figure 3.7 SPI interface timing characteristic

Table 3.1 SPI interface timing characteristic

Normal Write Mode(18/16-Bit Interface): VDDIO=1.6 to 3.3 V

Item		Symbol	Min	Тур	Max	unit
Carrial apleak avalatima	write	4	0.1		20	us
Serial colock cycle time	read	$t_{ m ckcyc}$	0.35		20	us
Comial coloals mules width low	write	4	40		_	ns
Serial colock pulse width low	read	$t_{ m ckl}$	150		_	ns
Carriel apleate pulse width high	write	t _{ckh}	40	_	_	ns
Serial colock pulse width high	read		150			ns
Serial clock rise/fall time			_	_	20	ns
SPI_nCS Setup time		t_{cse}	20	_	_	ns
SPI_nCS hold time	SPI_nCS hold time			_	_	ns
Data setup time	$t_{ m dse}$	30	_	_	ns	
Data hold time	$t_{ m dhd}$	30	_	_	ns	
Data output setup time	t _{sod}	_		130	ns	
Data output hold time		$t_{\rm soh}$	5	_	_	ns





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4. Power On/Off Sequence

4.1 Power On Sequence

The power on sequence of C1L1-05 is showed as below figures. nREST can't toggle while power rose up to 90%. The minimum time system can start to do reset is 40ms. C1L1-05 can be reset as nRESET keep low state in 1ms at least. Host can send commands and data to C1L1-05 as C1L1-05 finish resetting after nREST goes high 100us.

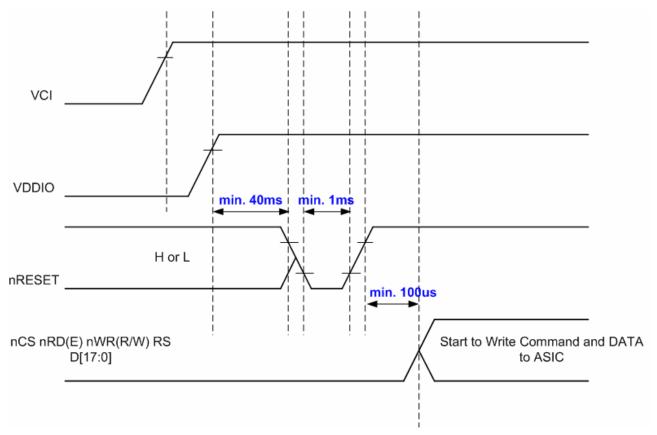


Figure 4.1 Power On Sequence - VCI Lead VDDIO

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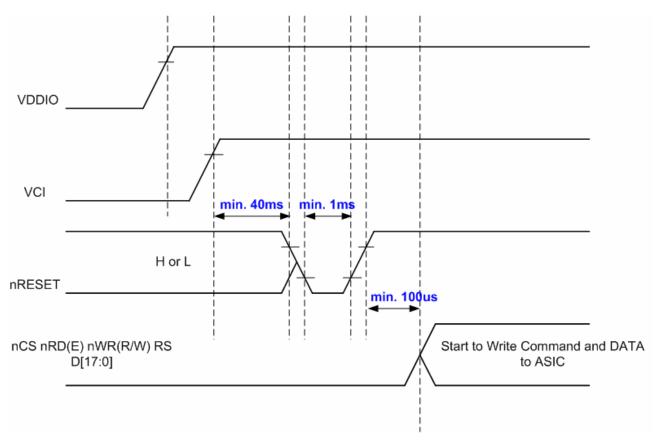


Figure 4.2 Power On Sequence - VCI Lag VDDIO





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4.2 Power Off Sequence

The power off sequence of C1L1-05 is showed as below figure. VCI VDDIO and nRESTE need to keep at least 20 frames time as host sends power off commands to C1L1-05.

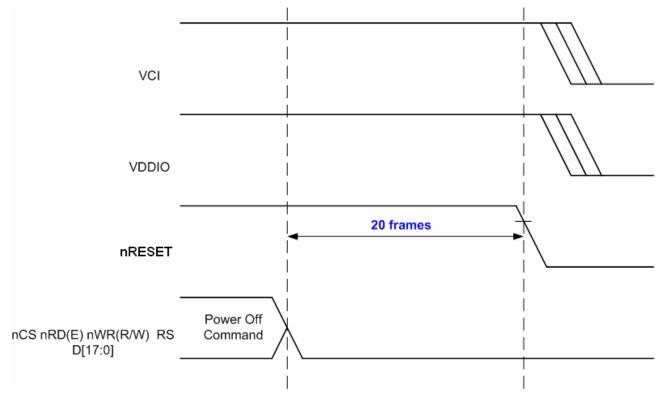


Figure 4.3 Power Off Sequence





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5. Software Application Guide5.1 LCD Module Application Type

While display modules are placed on boards, there are two types can be located. The one of this is LCD driver on bottom in observation and the other one is LCD driver on top. The difference to software is scanning direction and start point.



Figure 5.1 Type 1- IC on Bottom

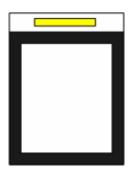


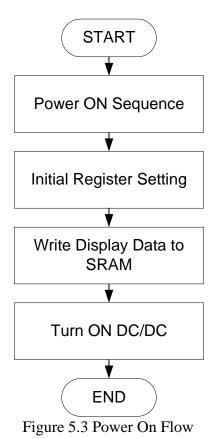
Figure 5.2 Type 2- IC on Top





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5.2 Power On Initial Setting







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hex Resolution_Select

Resolution_Select					
0x02h 0x42h 0x82h 0xC2h					
128x160					

hex DATA Input Select

DATA_Input_Select1							
0x00h	0x80h	0x40h	0x50h	0x60h	0xC0h		
8 bit	9 bit	16 bit BODR 00	16 bit BODR 01	16 bit BODR 1X	18 bit		

DATA_Input_Select2				
0x00h 0x20h				
18 bit (6:6:6) 16 bit (5:6:5)				

hex VCO Select

VCO_Select					
0x08h 0x0Ah 0x0Ch 0x08h					
128x160	128x128	96x96	132x160		

hex PWE_X_Select

PWE_X_Select					
0x7Fh	0x7Fh	0x5Fh	0x83h		
128x160	128x128	96x96	132x160		

hex PWE Y Select

	PWE Y Select					
0x9Fh 0x7Fh 0x5Fh 0x9Fh						
	128x160	128x128	96x96	132x160		

hex Start_X_Select

Start_X_Select(IC on Bottom)					
0x00h 0x00h 0x00h 0x00h					
128x160	128x128	96x96	132x160		

Start_X_Select(IC on Top)				
0x7Fh 0x7Fh 0x5Fh 0x83h				
128x160	128x128	96x96	132x160	

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hex Start_Y_Select

Start_Y_Select(IC on Bottom)				
0x00h 0x00h 0x00h 0x00h				
128x160	128x128	96x96	132x160	

Start_Y_Select(IC on Top)				
0x9Fh 0x7Fh 0x5Fh 0x9Fh				
128x160	128x128	96x96	132x160	

hex Scan Direction Select

Scan_Direction_Select		
0x00h	0x06h	
IC on Bottom	IC on TOP	

Write register MODE_SEL1(0x01h)=Resolution_Select

Write register MODE_SEL2(0x02h)=0x12h

Write register MODE_SEL3(0x03h)=DATA_Input_Select1 /*for CPU I/F*/

Write register MODE_SEL4(0x04h)=DATA_Input_Select2 /*for SPI I/F*/

Write register VCO_Mode(0x05h)=VCO_Select

Write register VCOMH_CTRL(0x07h)=0x7Fh

Write register VCOML_CTRL(0x08h)=0x17h

Write register PWS_X(0x09h)=0x00h

Write register PWS_Y(0x10h)=0x00h

Write register PWE_X(0x11h)=PWE_X_Select

Write register PWE_Y(0x12h)=PWE_Y_Select

Write register SRAM_POSITION_X(0x18h)= Start_X_Select

Write register SRAM_POSITION_Y(0x19h)= Start_Y_Select

Write register SRAM_Control(0x17h)= Scan_Direction_Select

integer x,y

for y = 0 to PWE_Y_Select

for x = 0 to PWE_X_Select

Write display data to SRAM

Write register DAC_OP_CTRL(0x06h)=0xC7h

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5.3 8 Color Partial Mode

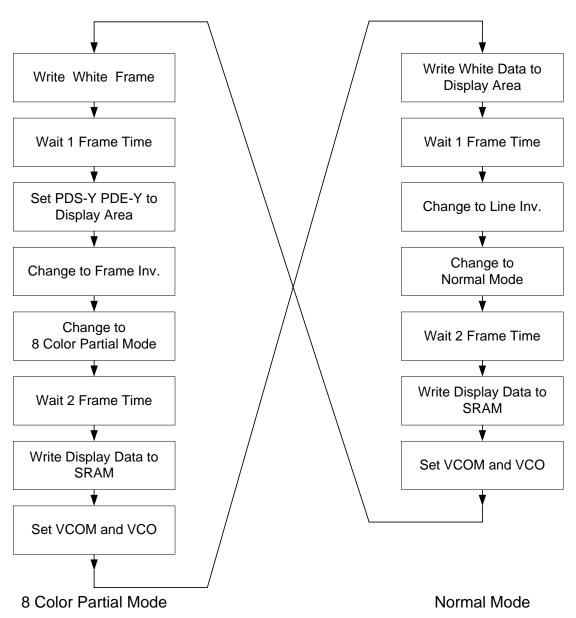


Figure 5.4 8 Color+Partial and Normal Exchange Flow





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5.3.1 To 8 Color+Partial Mode

hex Start_X_Select

Start_X_Select(IC on Bottom)				
0x00h 0x00h 0x00h 0x00h				
128x160	128x128	96x96	132x160	

Start_X_Select(IC on Top)				
0x7Fh 0x7Fh 0x5Fh 0x83h				
128x160	128x128	96x96	132x160	

hex Start_Y_Select

Start_Y_Select(IC on Bottom)				
0x00h 0x00h 0x00h 0x00h				
128x160	128x128	96x96	132x160	

Start_Y_Select(IC on TOP)				
0x9Fh 0x7Fh 0x5Fh 0x9Fh				
128x160	128x128	96x96	132x160	

hex Scan Direction Select

Scan_Direction_Select			
0x00h 0x06h			
IC on Bottom	IC on TOP		

hex Mode_Select

Mode_Select			
0x0Eh	0x4Eh	0x8Eh	0xCEh
128x160	128x128	96x96	132x160

hex Partial_Start_Y_Select

Partial_Start_Y_Select		
(Start_Partial_Line+1) (End_Partial_Line-1)		
IC on Bottom	IC on Bottom IC on TOP	





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hex Partial_VCO_Select

Partial_VCO_Select			
0x28h 0x2Ah 0x2Ch 0x28h			
128x160	128x128	96x96	132x160

Write register SRAM_POSITION_X(0x18h)= Start_X_Select Write register SRAM_POSITION_Y(0x19h)= Start_Y_Select Write register SRAM_Control(0x17h)= Scan_Direction_Select

integer x,y
for y = 0 to PWE_Y_Select
 for x = 0 to PWE_X_Select
 Write WHITE(R:G:B=0x3Fh:0x3Fh:0x3Fh) data to SRAM

Delay 1 Frame Time

Write register PDE_Y(0x16h)=End_Partial_Line(Set By Customer)
Write register PDS_Y(0x14h)=Start_Partial_Line(Set By Customer)
Write register MODE_SEL2(0x02h)=0x32h
Write register MODE_SEL1(0x01h)=Mode_Select

Delay 2 Frame Time

Write register SRAM_POSITION_X(0x18h)=Start_X_Select
Write register SRAM_POSITION_Y(0x19h)=Partial_Start_Y_Select
Write register SRAM_Control(0x17h)=Scan_Direction_Select

integer x,y
for y = 0 to (End_Partial_Line - Start_Partial_Line)
for x = 0 to PWE_X
 Write display data to SRAM

Write register VCO_Mode(0x05h)=Partial_VCO_Select





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5.3.2 Return Normal Mode

hex Start_X_Select

Start_X_Select(IC on Bottom)			
0x00h 0x00h 0x00h 0x00h			
128x160	128x128	96x96	132x160

Start_X_Select(IC on Top)				
0x7Fh 0x7Fh 0x5Fh 0x83h				
128x160	128x128	96x96	132x160	

hex Partial Start Y Select

· · · · · · · · · · · · · · · · · · ·			
Partial_Start_Y_Select			
(Start_Partial_Line+1) (End_Partial_Line-1)			
IC on Bottom	IC on TOP		

hex Scan_Direction_Select

Scan_Direction_Select		
0x00h 0x06h		
IC on Bottom	IC on TOP	

hex Resolution_Select

Resolution_Select			
0x02h 0x42h 0x82h 0xC2h			
128x160	128x128	96x96	132x160

hex Start_Y_Select

Start_Y_Select(IC on TOP)			
0x00h 0x00h 0x00h 0x00h			
128x160	128x128	96x96	132x160

Start_Y_Select(IC on Bottom)			
0x9Fh 0x7Fh 0x5Fh 0x9Fh			
128x160	128x128	96x96	132x160





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hex PWE_X_Select

PWE_X_Select						
0x7Fh	0x7Fh	0x5Fh	0x83h			
128x160	128x128	96x96	132x160			

hex PWE_Y_Select

PWE_Y_Select					
0x9Fh	0x7Fh	0x5Fh	0x9Fh		
128x160	128x128	96x96	132x160		

hex VCO_Select

VCO_Select					
0x08h	0x0Ah	0x0Ch	0x08h		
128x160	128x128	96x96	132x160		





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Write register SRAM_POSITION_X(0x18h)=Start_X_Select
Write register SRAM_POSITION_Y(0x19h)=Partial_Start_Y_Select
Write register SRAM_Control(0x17h)=Scan_Direction_Select

integer x,y
for y = 0 to (End_Partial_Line - Start_Partial_Line)
for x = 0 to PWE_X
 Write WHITE(R:G:B=0x3Fh:0x3Fh:0x3Fh) data to SRAM

Delay 1 Frame Time

Write register MODE_SEL2(0x02h)=0x12h
Write register MODE_SEL1(0x01h)=Resolution_Select

Delay 2 Frame Time

Write register SRAM_POSITION_X(0x18h)=Start_X_Select Write register SRAM_POSITION_Y(0x19h)=Start_Y_Select Write register SRAM_Control(0x17h)=Scan_Direction_Select

integer x,y
for y = 0 to PWE_Y_Select
 for x = 0 to PWE_X_Select
 Write display data to SRAM

Write register VCO_Mode(0x05h)=VCO_Select



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5.4 Sleep Mode Mode

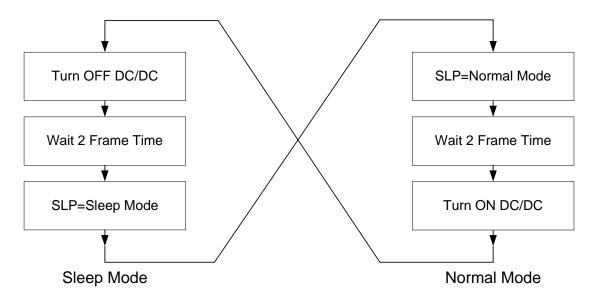


Figure 5.5 Sleep and Normal Exchange Flow

5.4.1 To Sleep Mode

Write register DAC_OP_CTRL(0x06h)=0x87h

Delay 2 Frame Time

Write register MODE_SEL1(0x01h)=0x00h

5.4.1 To Normal Mode

Write register MODE_SEL1(0x01h)=Resolution_Select

Delay 2 Frame Time

Write register DAC_OP_CTRL(0x06h)=0xC7h