TFT LCD MODULE

1.77" 262K 128RGB*160 DOTS

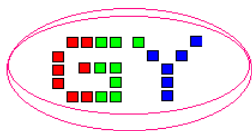## MODULE NO.: GYTF018M1B0M

REVISION: A00

Customer Approval:

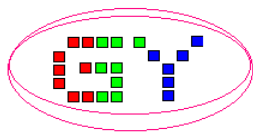|	SIGNATURE
PREPARED BY	ANDY YI
CHECKED BY	
APPROVED BY	

Table of Contents

Record of Revision

| Rev	Issued Date	Description
0.0	Mar. 20, 2006	New Create for GYTF018M1B0M

1. FEATURES

The 1.77"(4.487cm) LCD module is an active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used. Vertical drivers are built on the panel.

2. GENERAL SPECIFICATIONS

Item	Description	Unit
Display Size (Diagonal)	1.77 (4.487)	Inch (cm)
Display Type	Transmissive	
Active Area (HxV)	28.032 x 35.04	mm
Number of Dots (HxV)	128 x RGB x 160	dot
Dot Pitch (HxV)	0.073 x 0.219	mm
Color Arrangement	RGB Stripe	
Color Numbers	65K Driver IC support 262K	
Outline Dimension (HxVxT) *	34.0 x 45.78 x 2.90	mm
Weight	TBD	g

* Exclude protrusions.
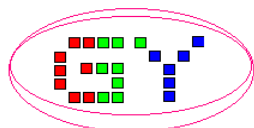
3. INPUT/OUTPUT TERMINALS

Interface: CPU mode 8080(Parallel)		
NO.	Name	Description
1	BL_K	LED1 Cathode
2	BL_A	LED Supply Voltage (LED1 Anode)
3	GND	System ground
4	VDD	Supply Voltage (2.5V~3.3V)
5	NC	Not connect
6	NC	Not connect
7	/CS	Chip Select(Low: Chip select; High: Chip de-select)
8	/RESET	Reset
9	RS	Command/DATA select (Low: command; High: data)
10	/WR	Write enable(Low: Write; High: Read)
11	/RD	Read enable
12	D7	Data 7
13	D6	Data 6
14	D5	Data 5
15	D4	Data 4
16	D3	Data 3
17	D2	Data 2
18	D1	Data 1
19	D0	Data 0
20	GND	System ground
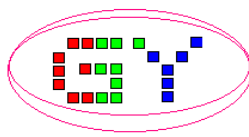
4. ABSOLUTE MAXIMUM RATINGS

VSS=0V

Item	Symbol	Min	MAX	Unit	Remark
Supply Voltage	VDD	--	+4.6	V	
I/O Supply Voltage	VDDIO	-0.3	VDD+0.3	V	
Input voltage	VI	-0.3	VDD+0.3	V	Note 4-1
Back Light Forward Current	I_F	-	+25	mA	
Operating temperature	Topr	-20	+70		
Storage temperature	Tstg	-40	+80		

Note 4-1 : VI   D0~D7, /CS, RS, /WR, /RD, /RESET.

## 5. ELECTRICAL CHARACTERISTICS

5.1 Driving TFT LCD Panel

VSS=0V, Ta=25

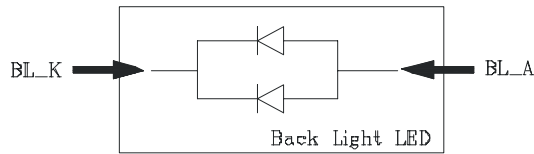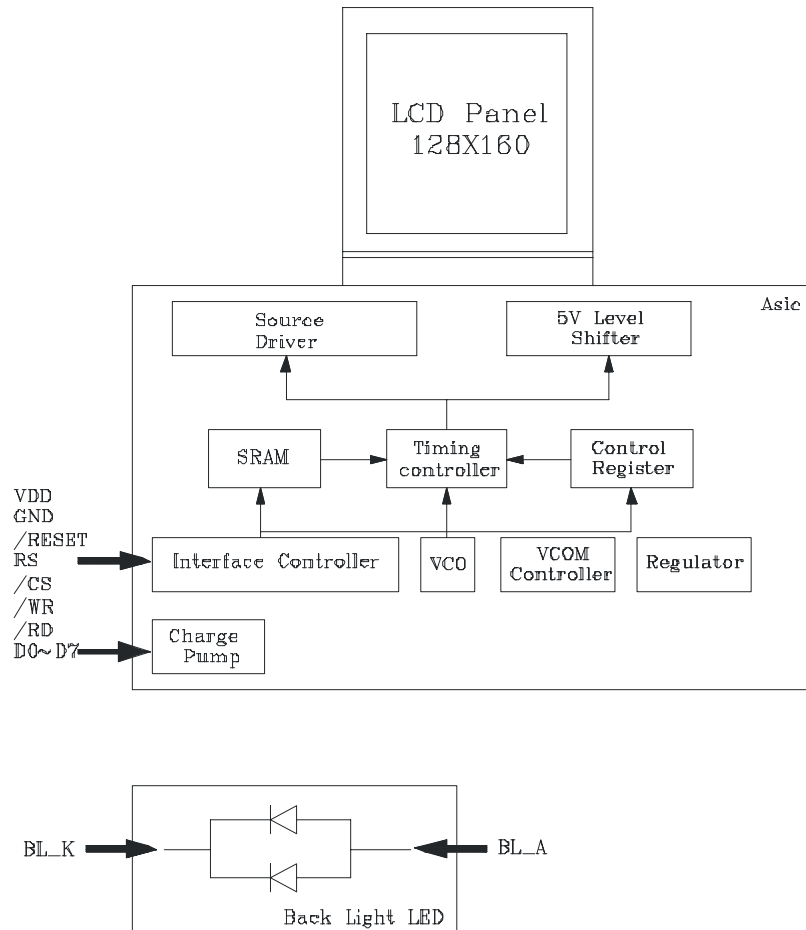| Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage	VDD	2.5	2.8	3.3	V	
Logic Input High Level	V_{IH}	0.8VDD	--	VDD	V	
Logic Input Low Level	V_{IL}	GND	--	0.2 VDD	V	
Power consumption in Normal Still mode (Line inversion , 70 Hz)	P_{Normal}	--	5.1	5.9	mW	
VDD Current consumption in Normal Still mode	$I_{VDD-Normal}$	--	1.8	2.1	mA	
Power consumption in 8 Color Partial Mode (Frame inversion , 50 Hz , 32 Line)	$P_{Partial}$	--	1.7	2.0	mW	Note 5-1
VDD Current consumption in 8 Color Partial Mode	$I_{VDD-Partial}$	--	0.6	0.7	mA	
Power consumption in Sleep Mode	P_{Sleep}	--	69	200	µW	
VCI Current consumption in Sleep Mode	$I_{VDD-Sleep}$	--	25	72	µA	

Note: 5-1: Power consumption test condition (VSS=0V, Ta=25   )

    a. Input voltage (VDD=2.8 V)

    b. Test pattern: Color Bar
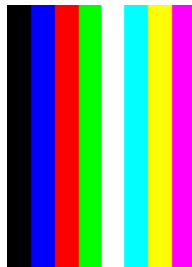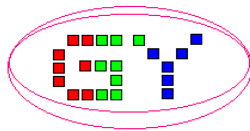
5.2 Driving TFT LCD Panel Block Diagram

5.3 Driving Backlight

Ta=25

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	--	30	30	mA	
Forward Current Voltage	V_F	3.0	3.2	3.4	V	Note 5-2
Backlight Power Consumption	W_{BL}	--	120	--	mW	

Note 5-2: Backlight driving circuit is recommend as the fix current circuit.

5.4 TFT LCD Panel Driver ASIC

The specifics please refer to the file: "C1L1-05 AISC CUSTOMER SPEC"
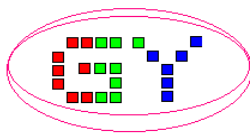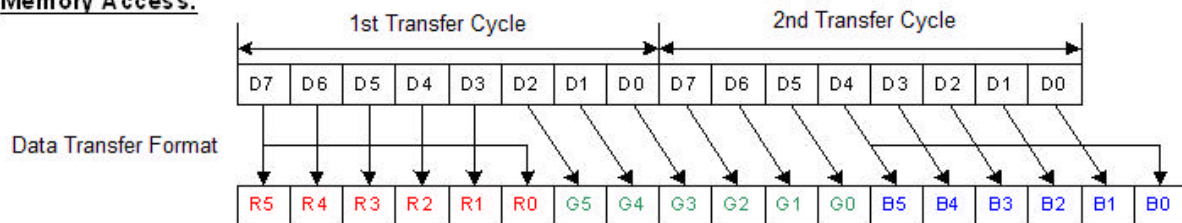
6. TIMING CHART

the Software Design Guide please refer to the file:"C1L1-05 Software Design Guide"
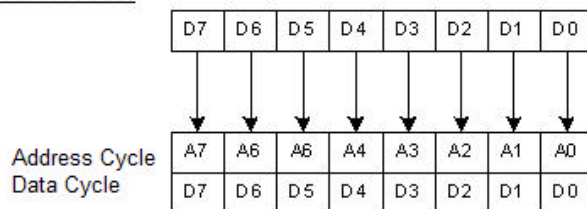
6.1 CPU Interface Mode

8-bit CPU Interface Mode
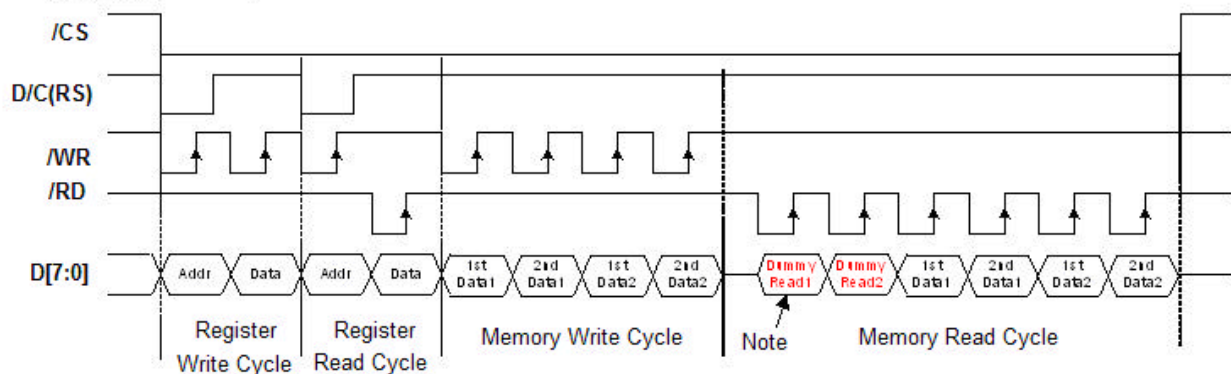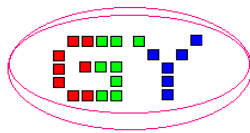
CPU Interface 8080 Mode
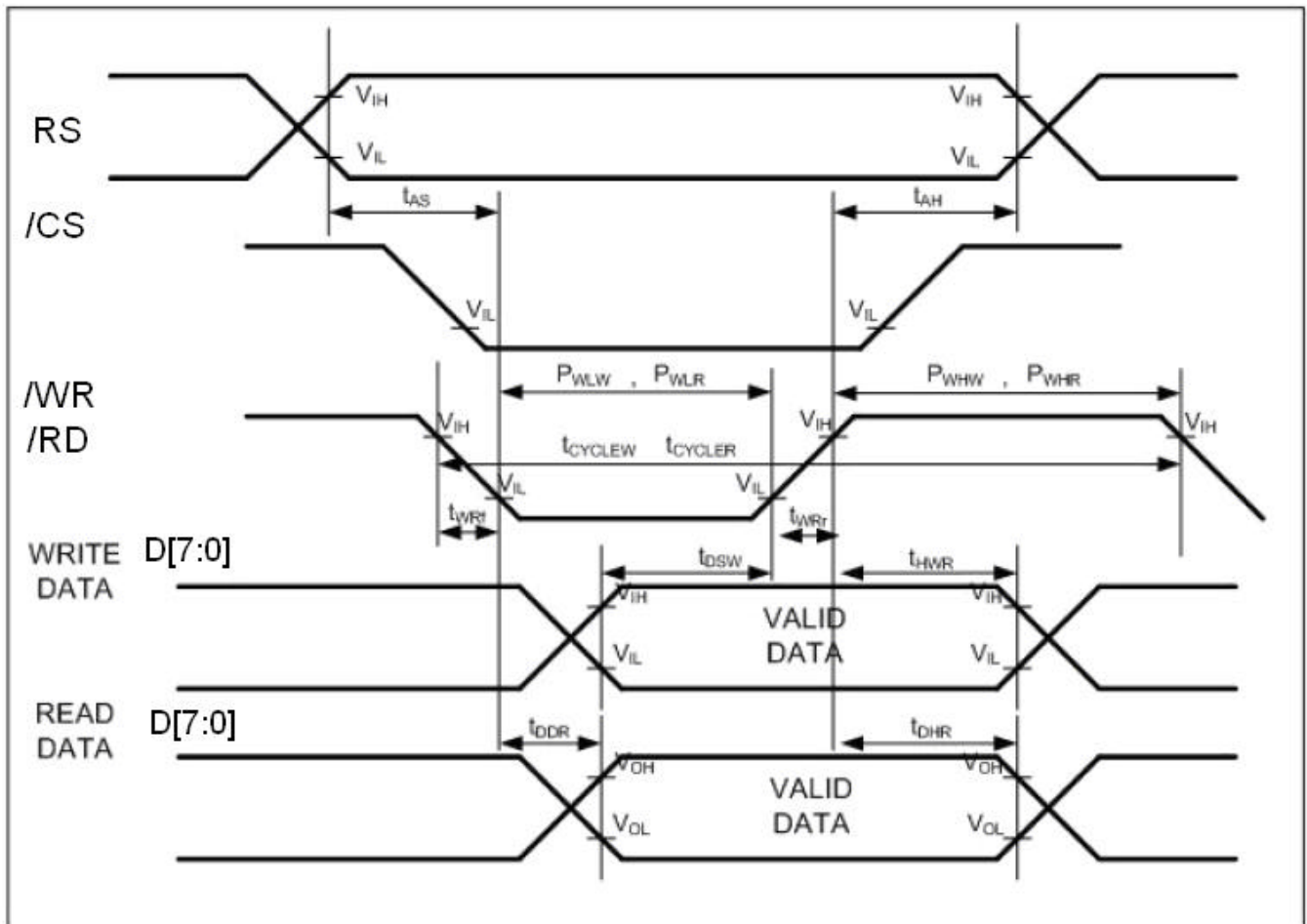
Normal Write Mode:

Item	Symbol	Min	Typ	Max	unit
Bus cycle time	t_{CYCLEW}	100			ns
	t_{CYCLER}	500			ns
/WR, /RD pulse width low	P_{WLW}	40			ns
	P_{WLR}	250			ns
/WR, /RD pulse width high	P_{WHW}	50			ns
	P_{WHR}	200			ns
Pulse rise/fall time	t_{WRr}, t_{WRf}			25	ns
Setup time [RS, /CS, /WR, RD]	t_{AS}	10			ns
Hold time [RS, /CS, /WR, RD]	t_{AH}	2			ns
Data setup time	t_{DSW}	25			ns
Data hold time	t_{HWR}	5			ns
Data output setup time	t_{DDR}			100	ns
Data output hold time	T_{DHR}	5			ns

6.2 Display Power Up Timing and Register Initialization Sequence

6.3.1.1 Initial Power Up in Normal Mode

Power Up
- VDDIO = 1.6V ~ 3.3V
- VCI = 2.5V ~ 3.3V

Hardware Reset
- Active low ≥ 16.67 ms
- Active high ≥ 16.67 ms

Initial Code
- Display Register Initialization
  Sequence – Normal Mode

Normal Mode

Normal Mode Register Setting

128x160

128x160
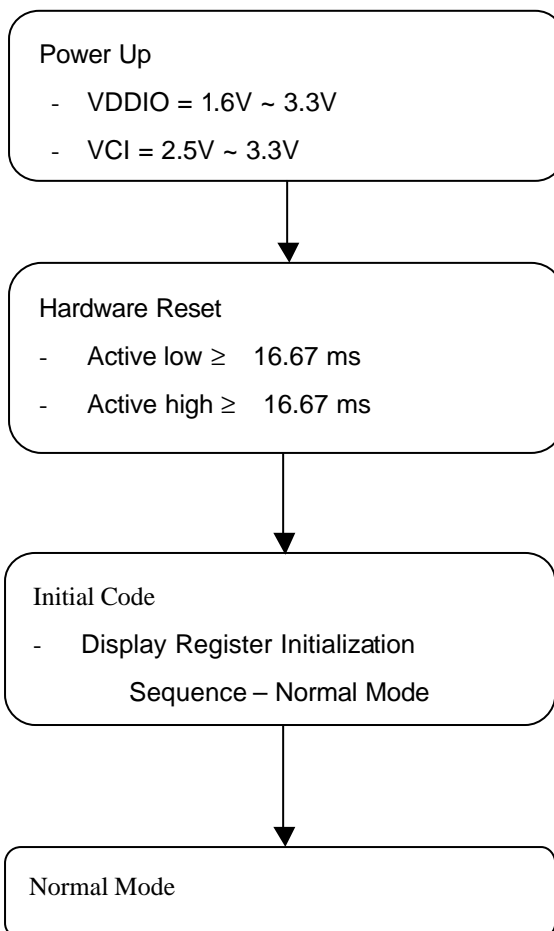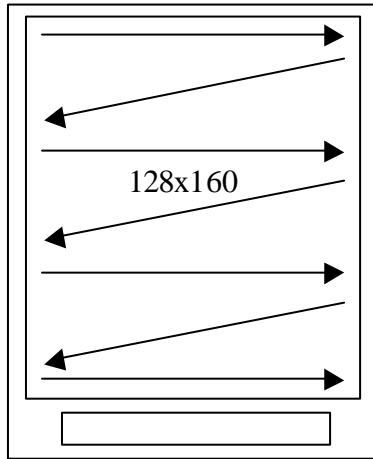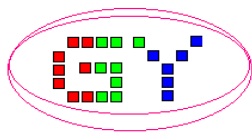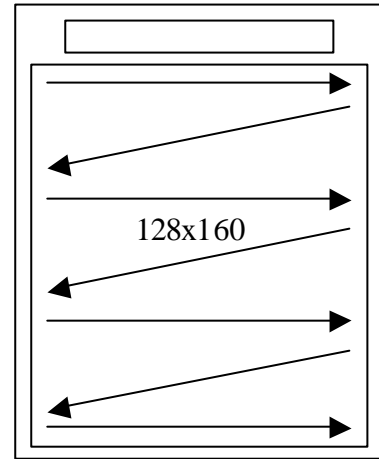
IC on Bottom
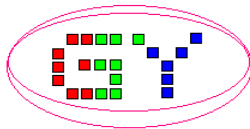
IC on Top

6.3.1.2 Normal Mode Command Setting

	Instruction	R/W	D/C	IC on Bottom	IC on Top	Description
1	MODE_SEL1	0	0	0x01h	0x01h	1. Resolution 128x160
		0	1	0x02h	0x02h	2. 16/18 bits color
2	MODE_SEL2	0	0	0x02h	0x02h	1. Single Panel (Main On/Sub off)
		0	1	0x12h	0x12h	2. Line Inversion
3	MODE_SEL3	0	0	0x03h	0x03h	1.CPU Interface 8 bits mode
		0	1	0x00h	0x00h	
4	VCO_Mode	0	0	0x05h	0x05h	1.VCO frequency 1.82 MHz
		0	1	0x08h	0x08h	
5	VCOMH_CTRL	0	0	0x07h	0x07h	1. Set VCOM_H = 4.184V
		0	1	0x7Fh	0x7Fh	
6	VCOML_CTRL	0	0	0x08h	0x08h	1. Set VCOM_L = 0.377V
		0	1	0x17h	0x17h	
7	SRAM_Position_X	0	0	0x18h	0x18h	1. Set starting position in x-axis as writing SRAM
		0	1	0x00h	0x7Fh	
8	SRAM_Position_Y	0	0	0x19h	0x19h	1. Set starting position in y-axis as writing SRAM
		0	1	0x00h	0x9Fh	
9	SRAM_Control	0	0	0x17h	0x17h	
		0	1	0x00h	0x06h	

Integer x,y
for x = 0 to 127
for y = 0 to 159
Write White data(R : G : B = 0x3Fh : 0x3Fh : 0X3Fh) to SRAM

	Instruction	R/W	D/C	IC on Bottom	IC on Top	Description
10	DAC_OP_CTRL	0	0	0x06h	0x06h	1. Set nPWDN = 1 to turn on DC/DC
		0	1	0xC7h	0xC7h	
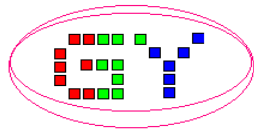
6.3.1.3 Normal Mode → Partial Mode Register Setting

Enter Partial Mode

	Instruction	R/W	D/C	IC on Bottom	IC on Top	Description
1	SRAM_Position_X	0	0	0x18h	0x15h	1. Set starting position in x-axis as writing SRAM.
		0	1	0x00h	0x7Fh	
2	SRAM_Position_Y	0	0	0x19h	0x19h	1. Set starting position in y-axis as writing SRAM.
		0	1	0x00h	0x9Fh	
3	SRAM_Control	0	0	0x17h	0x17h	
		0	1	0x00h	0x06h	

Integer x,y
for x = 0 to 127
for y = 0 to 159
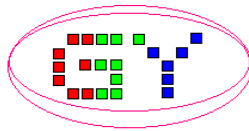Write White data(R : G : B = 0x3Fh : 0x3Fh : 0X3Fh) to SRAM

Wait 2 frame (16.67x2 ms) time to show at least one white frame

	Instruction	R/W	D/C	IC on Bottom	IC on Top	Description
4	MODE_SEL2	0	0	0x02h	0x02h	
		0	1	0x32h	0x32h	
5	MODE_SEL1	0	0	0x01h	0x01h	
		0	1	0xDEh	0xDEh	

Wait 3 frame (16.67x3 ms) time to enter 8 color partial mode and frame inversion

	Instruction	R/W	D/C	IC on Bottom	IC on Top	Description
6	PDE-Y	0	0	0x16h	0x16h	Set partial Area 1st Horizontal Line
		0	1	0x40h	0x40h	
7	PDS-Y	0	0	0x14h	0x14h	Set partial Area Last Horizontal Line
		0	1	0x1Fh	0x1Fh	
8	SRAM_Position_X	0	0	0x18h	0x18h	1. Set starting position in x-axis as writing SRAM
		0	1	0x00h	0x7Fh	
9	SRAM_Position_Y	0	0	0x19h	0x19h	1. Set starting position in y-axis as writing SRAM
		0	1	0x20h	0x3Fh	
10	SRAM_Control	0	0	0x17h	0x17h	
		0	1	0x00h	0x06h	

Integer x,y
for x = 0 to 127
for y = 0 to 31
Write display data to SRAM

	Instruction	R/W	D/C	IC on Bottom	IC on Top	Description
11	VCO_Mode	0	0	0x05h	0x05h	1. Set VCO = 1.92*3.4MHz
		0	1	0x28h	0x28h	

Register 0x14 = A-1th Line
Register 0x16 = B+1th Line

Non-Partial Area

Partial Area

Non-Partial Area

Panel

Non-Partial Area

Partial Area

Non-Partial Area

SRAM

Ath Line

Bth Line

Exit Partial Mode

	Instruction	R/W	D/C	IC on Bottom	IC on Top	Description
1	SRAM_Position_X	0	0	0x18h	0x18h	1. Set starting position in x-axis as writing SRAM
		0	1	0x00h	0x7Fh	
2	SRAM_Position_Y	0	0	0x19h	0x19h	1. Set starting position in y-axis as writing SRAM
		0	1	0x20h	0x3Fh	
3	SRAM_Control	0	0	0x17h	0x17h	
		0	1	0x00h	0x06h	

Integer x,y
   for x = 0 to 127
   for y = 0 to 31
     Write White data(R : G : B = 0x3Fh : 0x3Fh : 0X3Fh) to SRAM					

Wait 2 frame (16.67x2 ms) time to show at least one white frame					
6	MODE_SEL2	0	0	0x02h	0x02h	Set Line Inversion
		0	1	0x12h	0x12h	
7	MODE_SEL1	0	0	0x01h	0x01h	Set 16/18 bits color
		0	1	0x02h	0x02h	
Wait 2 frame (16.67x2 ms) time to enter normal mode and line inversion					
8	SRAM_Position_X	0	0	0x18h	0x18h	1. Set starting position in x-axis as writing SRAM
		0	1	0x00h	0x7Fh	
9	SRAM_Position_Y	0	0	0x19h	0x19h	1. Set starting position in y-axis as writing SRAM
		0	1	0x00h	0x9Fh	
10	SRAM_Control	0	0	0x17h	0x17h	
		0	1	0x00h	0x06h	

Integer x,y
   for x = 0 to 127
   for y = 0 to 159
     Write display data to SRAM					

11	VCO_Mode	0	0	0x05h	0x05h	
		0	1	0x08h	0x08h	
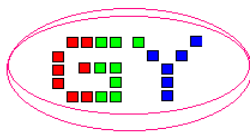
6.3.1.5   Normal Mode → Sleep Mode Register Setting

Enter Sleep Mode

Instruction		R/W	D/C	IC on Bottom	IC on Top	Description
1	DAC_OP_CTRL	0	0	0x06h	0x06h	1. nPWDN = 0
		0	1	0x87h	0x87h	
Wait 2 frame (16.67 x 2 ms) time						
2	MODE_SEL1	0	0	0x01h	0x01h	1. SLP = Sleep Mode
		0	1	0x00h	0x00h	

6.3.1.6   Sleep Mode → Normal Mode Register Setting

Exit Sleep Mode

Instruction		R/W	D/C	IC on Bottom	IC on Top	Description
1	MODE_SEL1	0	0	0x01h	0x01h	1. SLP = Normal Mode
		0	1	0x02h	0x02h	
Wait 2 frame (16.67 x 2 ms) time						
2	DAC_OP_CTRL	0	0	0x06h	0x06h	1. nPWDN = 1
		0	1	0xC7h	0xC7h	
Wait 10 frame (16.67 x 10 ms) time						

6.3.1.12 Normal Mode → Power Down

Normal Operation

Power OFF
-    Display off
-    Enter Sleep mode
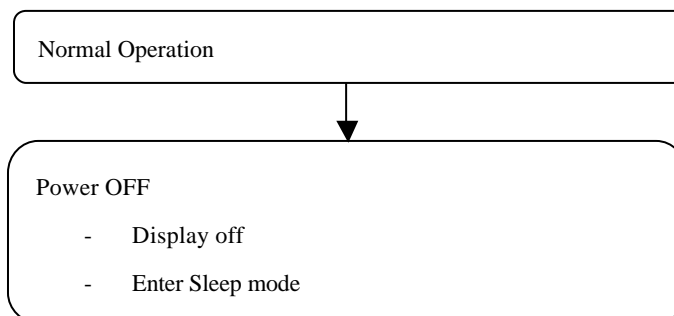
6.3.1.13 Normal Mode → Power Down Register Setting

Instruction		R/W	D/C	IC on Bottom	IC on Top	Description
1	DAC_OP_CTRL	0	0	0x06h	0x06h	1. nPWDN = 0
		0	1	0x87h	0x87h	
Wait 2 frame (16.67 x 2 ms) time						
2	MODE_SEL1	0	0	0x01h	0x01h	1. SLP = Sleep Mode
		0	1	0x00h	0x00h	

t_{PDWON}=min. 20 frame

VDD

/RESET

/WR

/CS

RS

D[7:0]   0x06   0x87   0x01   0x00

2 frame

Last Command

6.4 Gray Scale of Each Color

65K

| Color	Display	Data Signal																Gray Scale
		Red					Green						Blue					
		R0	R1	R2	R3	R4	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	Blue	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	-
	Green	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	-
	Cyan	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	-
	Red	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	-
	Magenta	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	-
	Yellow	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	-
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	Dark	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
																		R3~
																		R28
		1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	R29
	Light	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	R30
	Red	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	R31
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	Dark	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G1
		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	G2
																		G3~
																		G60
		0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	G61
	Light	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	G62
	Green	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	G63
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	Dark	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B1
		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	B2
																		B3~
																		B28
		0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	B29
	Light	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	B30
	Blue	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B31
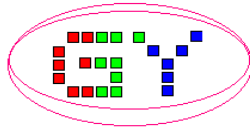
7. OPTICAL CHARACTERISTICS

7.1 Optical Specification

7.1.1 Transmissive Mode (Back Light On, LED current = 20mA)

Ta=25

| Item		Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Viewing angles	3 o`clock	11	CR = 2 (Gray Scale Inversion Direction: 9 o`clock)	TBD	35	--	Degree	Note 7-1
	9 o`clock	12		TBD	60	--		
	12 o`clock	21		TBD	60	--		
	6 0`clock	22		TBD	60	--		
Contrast ratio		CR	=0°	250	300	--		Note 7-2
Uniformity		Lu		70	80	--		Note 7-9
Response Time		Tr + Tf		--	35	--	ms	Note 7-3
Luminance		L		TBD	150	--	cd/m^2	Note 7-4
Chromaticity	White	u`		TBD	0.201	TBD		Note 7-5
		v`		TBD	0.467	TBD		
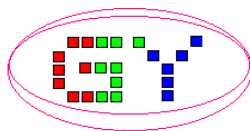
7.2 Basic Measure Condition

(1) Ambient Temperature: Ta=25

(2) Testing Point: Measure in the display center point and the test angleT=0°

(3) Measuring System

    a. Measure System C

TFT LCD Module with Backlight

Photometer

35cm
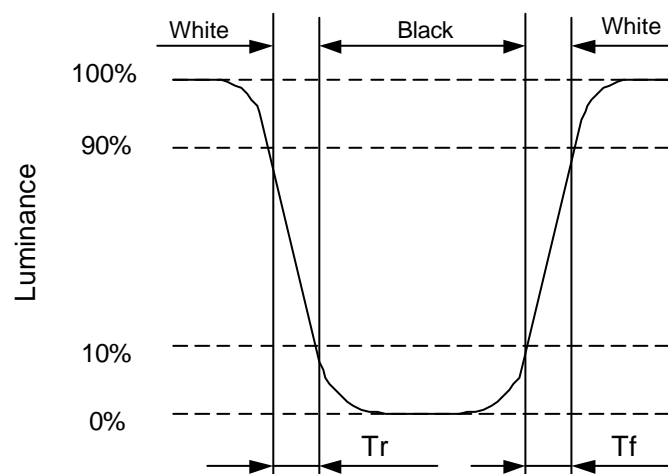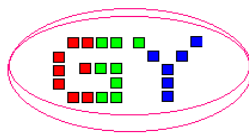
Data Signal Input
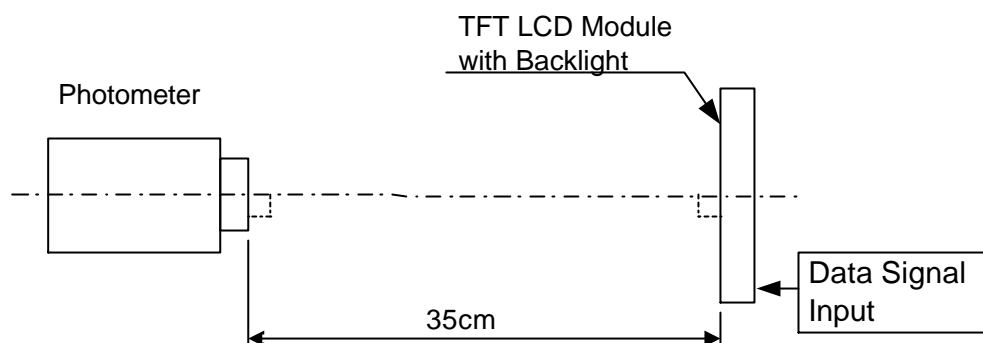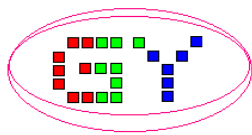
Note 7-1: Viewing angle diagram:
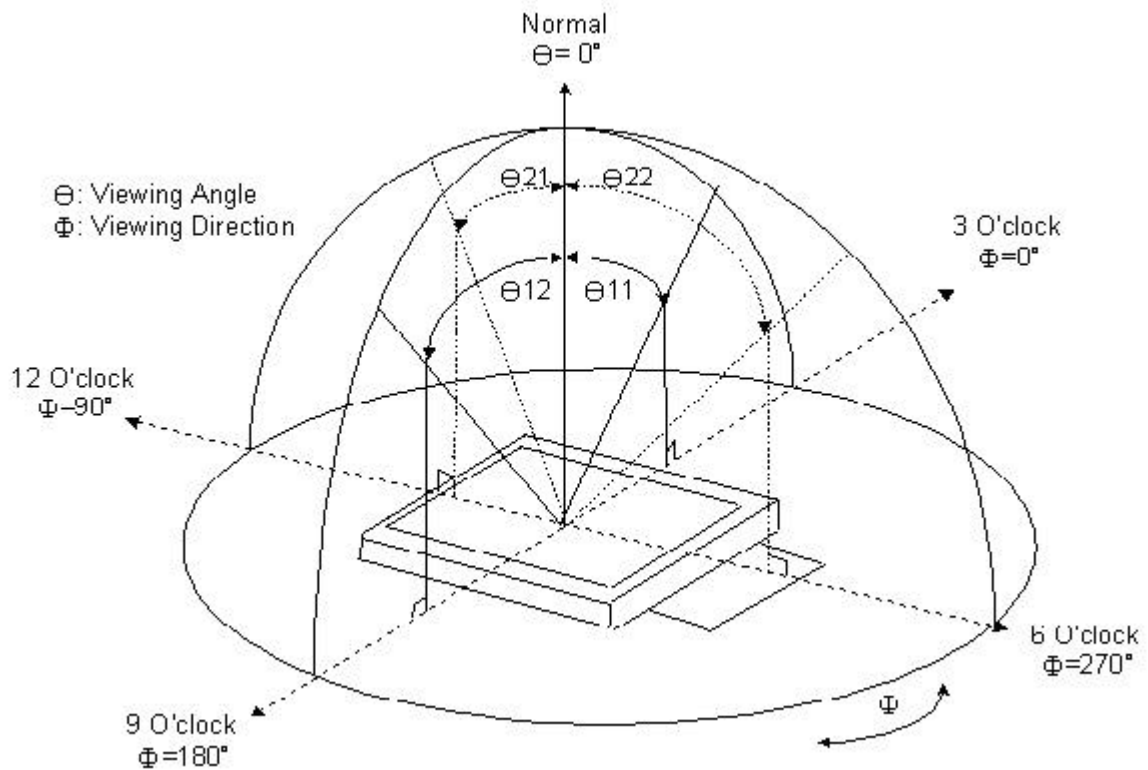
Note 7-2: Contrast Ratio as Backlight On: (Measure System C)

Contrast ratio is measured in optimum common electrode voltage. The signal amplitude

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 7-3: Definition of response time: (Measure System C)

Note 7-4: Luminance: (Measure System C)

       Test Point: Display Center

       LED Current I_F = 20 mA

Note 7-5: Chromaticity: The same test condition as Note 7-4.

Note: 7-6: Contrast Ratio as Backlight Off (Measure System B)

       Contrast ratio is measured in optimum common electrode voltage. The signal amplitude

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 7-7: White chromaticity as back light off (Measure System A)
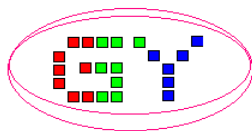
Note 7-8: Reflectance (Measure System B)

$$\text{Reflection ratio(R)} = \frac{\text{Light detected level of refection by the LCD module}}{\text{Light detected level of refection by the standard white}}$$

Notes 7-9: Definition of uniformity: Light on backlight 5 minutes before test.

$$\text{Uniformity (Lu)} = \frac{\text{Minimum Luminance of 9 test points}}{\text{Center Point Luminance of 9 test points}}$$

       The definition of 9 test points:
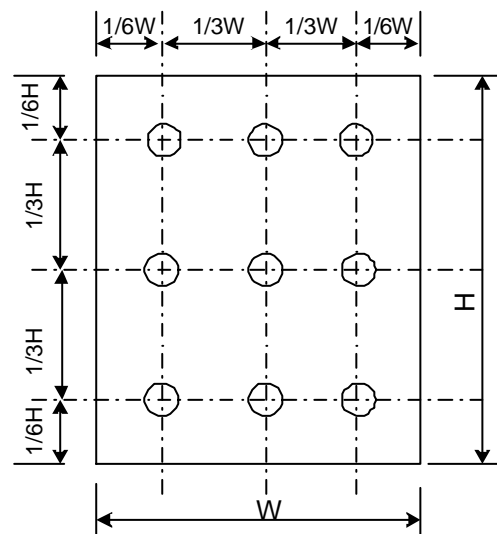
8. HANDLING CAUTIONS

8.1 ESD (Electrical Static Discharge) Strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

8.1.1 In handling LCD panel, please wear non-charged material gloves. Connect the wrist conduction ring to the earth and the conducting shoes to the earth are necessary.

8.1.2 The machine and working table for the panel should have ESD protection strategy.

8.1.3 In handling the panel, using ionized air to decrease the charge in the environment is necessary.

8.1.4 In the process of assembly the module, shield case should connect to the ground.
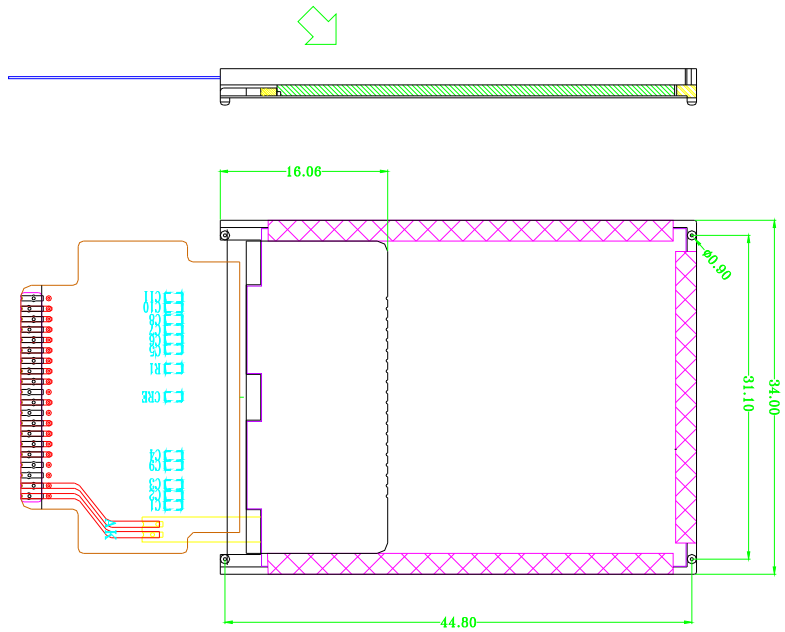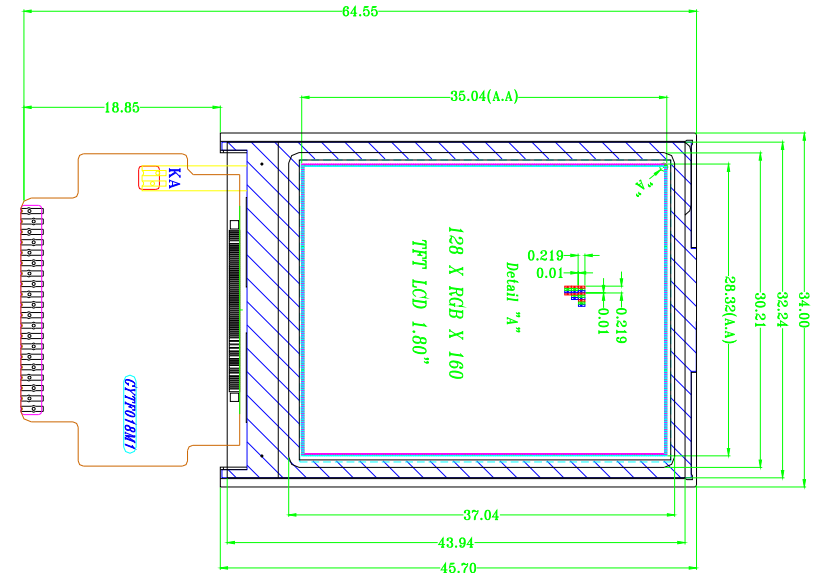
8.2 Environment

8.2.1 Working environment of the panel should be in the clean room.

8.2.2 The front polarizer is easy damaged. Handle it carefully and do not scratch it by sharp material.

8.2.3 Panel has polarizer protective film in the surface. Please remove the protection film of polarizer slowly with ionized air to prevent the electrostatic discharge.

8.3 Others

8.3.1 Turn off the power supply before connecting and disconnecting signal input cable.

8.3.2 Water drop on the surface or condensation as panel power on will corrode panel electrode.

8.3.3 As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

8.3.4 When the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hand cleanly by water and soap as soon as possible.
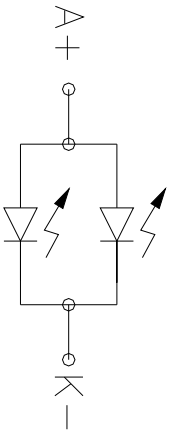
9 MECHANICAL DRAWING

NOTES:
1. DISPLAY TYPE: TFT-LCD.
2. VIEWING DIRECTION: 6 O'CLOCK.
3. DRIVE METHOD:
4. OPERATING VOLTAGE: 3.0 V.
5. POLARIZER MODE: TRANSMISSIVE/POSITIVE.
6. OPERATING TEMP: -20 ~ +70°C.
7. STORAGE TEMP: -30 ~ +80°C.
8. RESOLUTIAN: TF018TUYM1+CILI

押膨随时间变化有改良，不另行通知。

128 X RGB X 160
TFT LCD 1.80"

Detail "A"
0.219
0.01
0.219
0.01

64.55
35.04(A.A)
18.85
34.00
32.24
30.21
28.32(A.A)
37.04
43.94
45.70
16.06
34.00
31.10
Ø0.90
44.80

KA

GYTF018M1

A+

K-

PIN	DESC
1	LED_K
2	LED_A
3	GND
4	VDD
5	NC
6	NC
7	/CS
8	/RST
9	RS
10	/WR
11	/RD
12	D7
13	D6
14	D5
15	D4
16	D3
17	D2
18	D1
19	D0
20	GND

TITLE	L C D		
PROJECTION	DATE 2008.06.15		
DRWN lsj	DATE		
CHK	DATE		
APVD	DATE		
MODEL	GYTF018M1BOM	REVISION 0	
UNITS mm	SCALE /	SHEET 1/1	

TEL:0755-27917055,27794928 FAX:0755-27911170
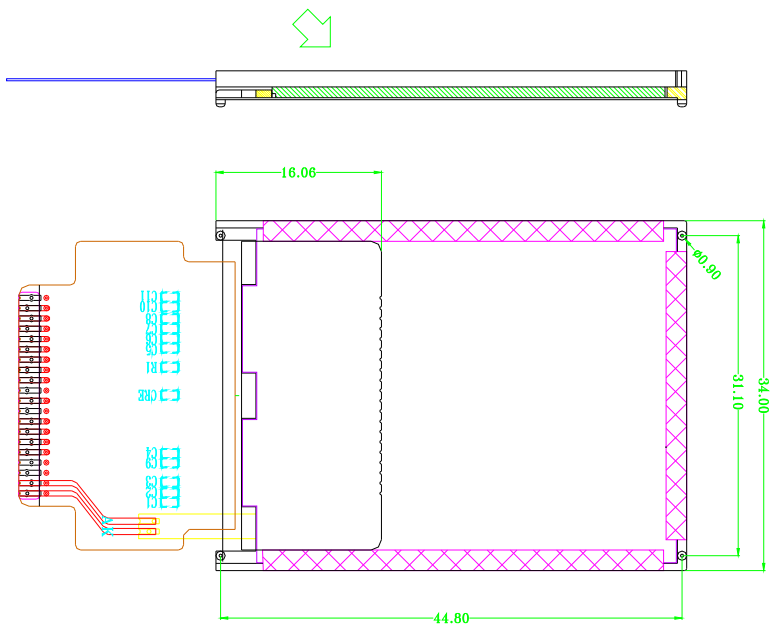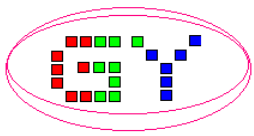SHENZHEN G.Y. LCD.TECHNOLOGY.
广源液晶科技

NOTES:
1. DISPLAY TYPE: TFT-LCD.
2. VIEWING DIRECTION: 6 O'CLOCK.
3. DRIVE METHOD:
4. OPERATING VOLTAGE: 3.0 V.
5. POLARIZER MODE: TRANSMISSIVE/POSITIVE.
6. OPERATING TEMP: -20 ~ +70°C.
7. STORAGE TEMP: -30 ~ +80°C.
8. RESOLUTIAN: TF018TUYM1+C1L1

128 X RGB X 160
TFT LCD 1.80"

Detail "A"

0.219
0.01
0.219
0.01

64.55
18.85
35.04(A.A)
37.04
43.94
45.70
34.00
32.24
30.21
28.32(A.A)

16.06
44.80
34.00
31.10
Ø0.90

GYTF018MI

KA

A+
K-

@级视图内有直径0.2MM以下白点或红点或蓝点，仅限一个！

PIN	DESC
1	LED_K
2	LED_A
3	GND
4	VDD
5	NC
6	NC
7	/CS
8	/RST
9	RS
10	/WR
11	/RD
12	D7
13	D6
14	D5
15	D4
16	D3
17	D2
18	D1
19	D0
20	GND

TITLE			LCD		
PROJECTION	DRWN lsj	DATE 2008.06.15			
	CHK	DATE			
	APVD	DATE			

MODEL GYTF018M1BOM-S
UNITS mm SCALE / REVISION 0 SHEET 1/1

广深源电科技
SHENZHEN G.Y. LCD.TECHNOLOGY.
TEL:0755-27917065,27794928 FAX:0755-27911170

10   PACKING DRAWING

①

Module with display face down

Module Qty =18pcs/Tray

③

Cardboard

Carton

②

Desiccant(2pcs)

Empty Tray(1pcs)

20 Layers
(with Modules)

Total 21Layers

LDPE bag

④

210

270

350

Module Qty =360pcs/Carton
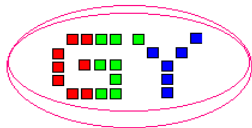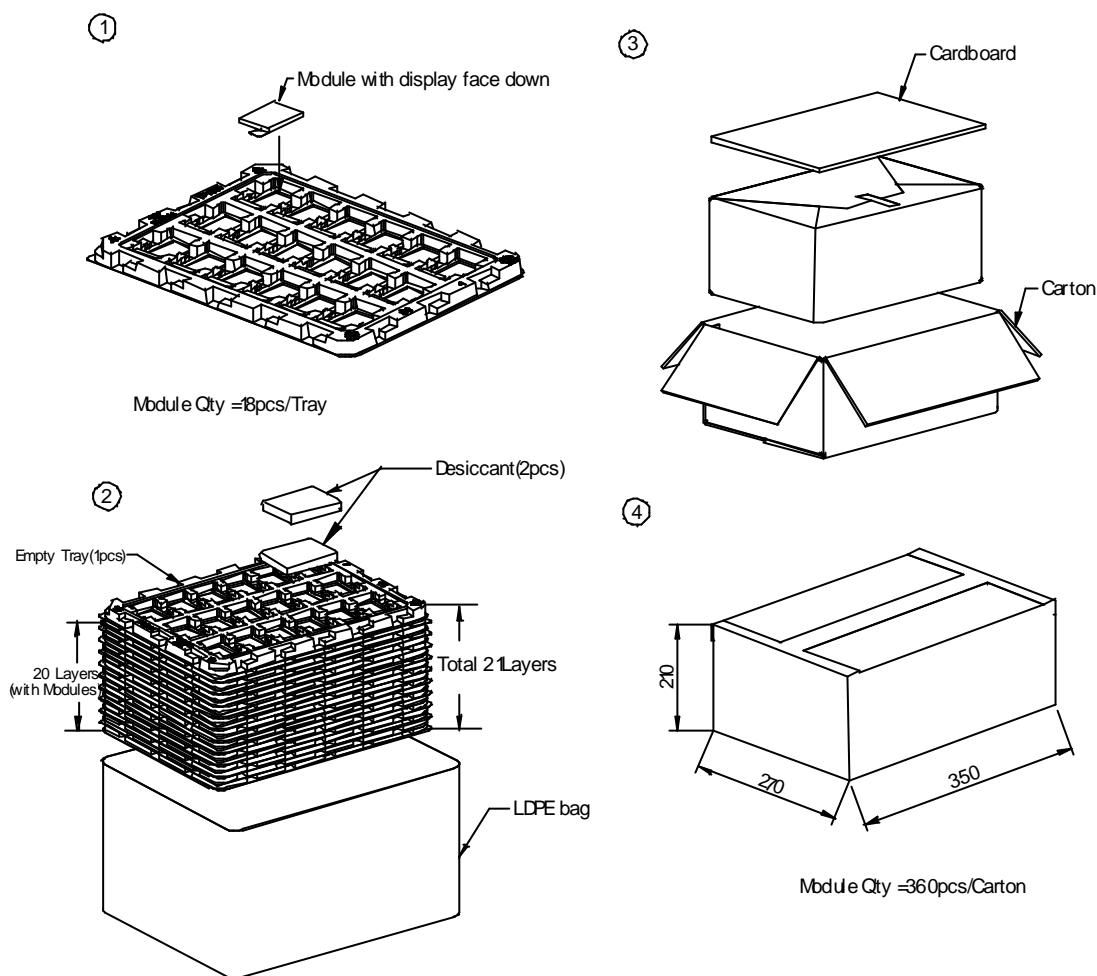
1.8" Module delivery packing method

(1).Placed the module into tray cavity(with panel display face down).

(2).The tray stacking with 20 layers and with 1 empty tray above the stacking tray unit.
Place 2 pcs desiccants above the empty tray then place the stacking tray unit into
the LDPE bag and sealing the bag opening by adhesion tape.

(3).Placed the package unit into the carton and cover 1pc cardboard above the package unit.

(4).Carton sealing with adhesive tape.