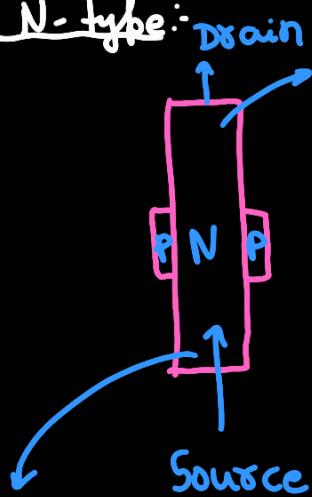


# JFET Amplifiers

\* Consider N-type :-

Recap of  
POE



Consists of  $e^-$  as majority charge carrier

Minority charge carrier is due  
to thermal agitation  $\Rightarrow e^-$  are  
sourced

$e^-$  move in  
one dir<sup>n</sup> based on biasing  
but always  
from -ve to +ve

Semiconductor bar consist of two terminals

\* Source

\* Drain

P-type diffused to the bar forms a terminal called "Gate"

$\therefore$  JFET is a three terminal device consisting of source, drain & gate

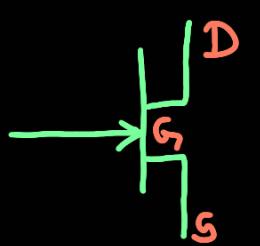
$e^-$  move from source to drain when biaser voltage is applied

b/w source & drain.

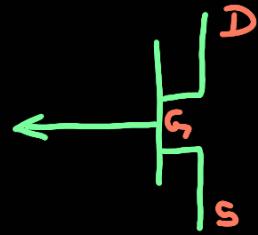
$\downarrow$              $\downarrow$   
 -ve            +ve  
 Voltage      Voltage

\* JFET is either N-channel or P-channel  
(The bar is the channel)

## # Circuit symbol for JFET:-



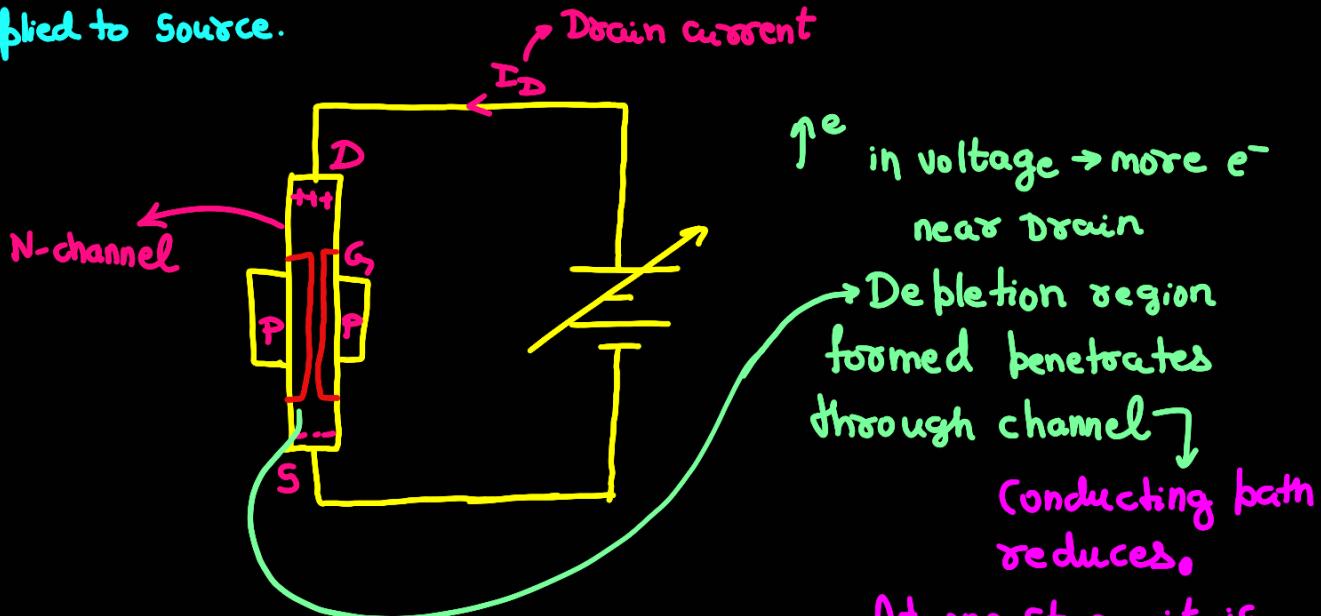
N-channel FET



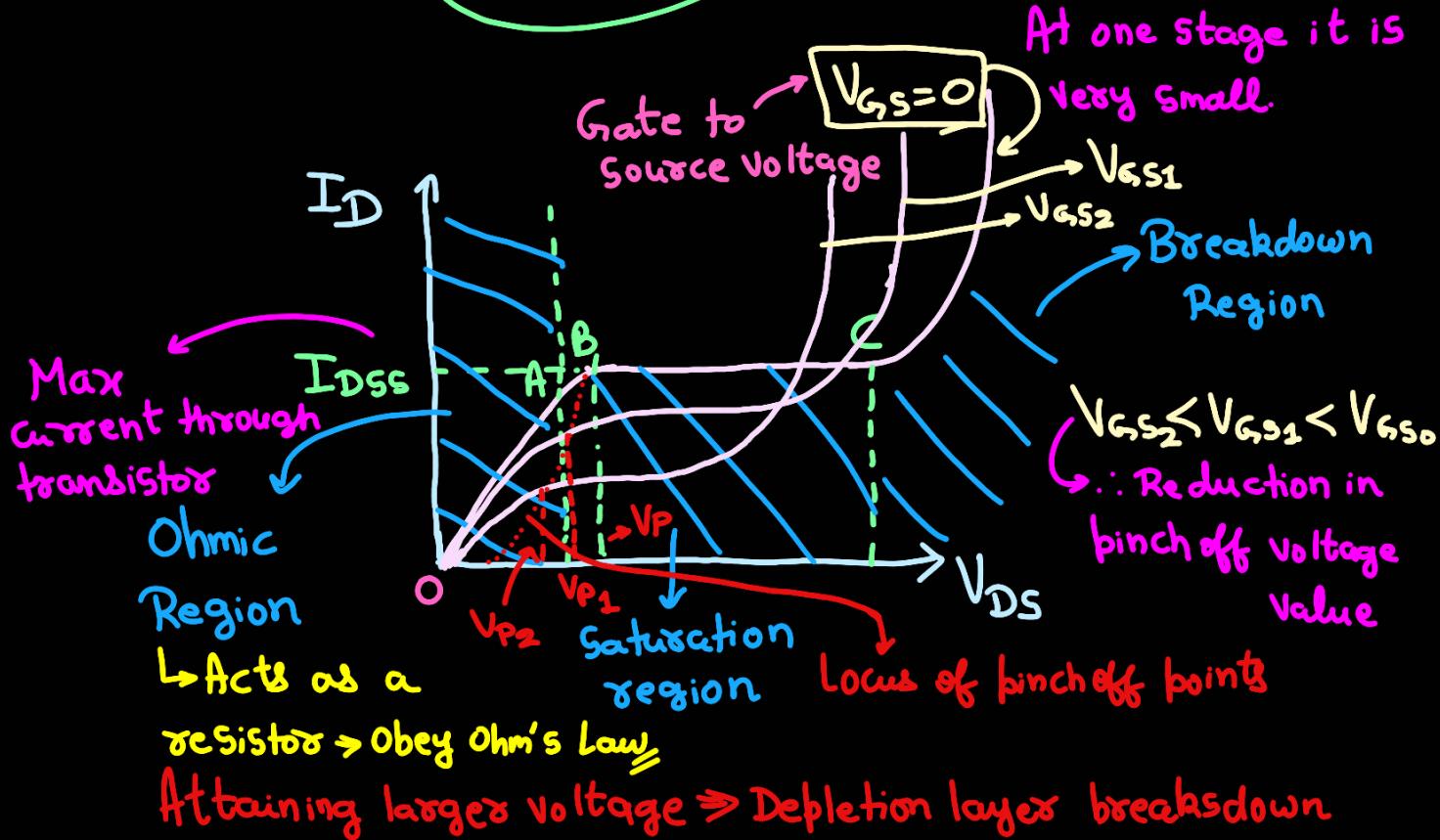
P-channel FET

## # Characteristics of JFET:-

Consider N-channel FET, +ve voltage applied to drain, -ve voltage applied to Source.



$\uparrow e^-$  in voltage  $\rightarrow$  more  $e^-$  near Drain  
 Depletion region formed penetrates through channel  $\downarrow$   
 (conducting path reduced)



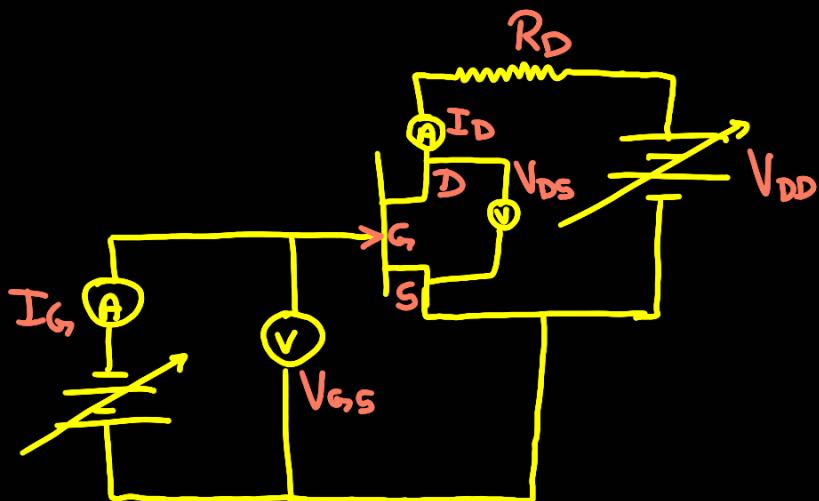
## $\star$ O to A $\rightarrow$ Ohmic Region

→ A to B → Drain keeps decreasing because of depletion region b/w gate & drain

At B, drain current is pinched off.

Point B is called Pinchoff point

The drain to source to source voltage ( $V_{DS}$ ) at B is  
Pinch off Voltage



Therefore, there is  
no IP characteristics

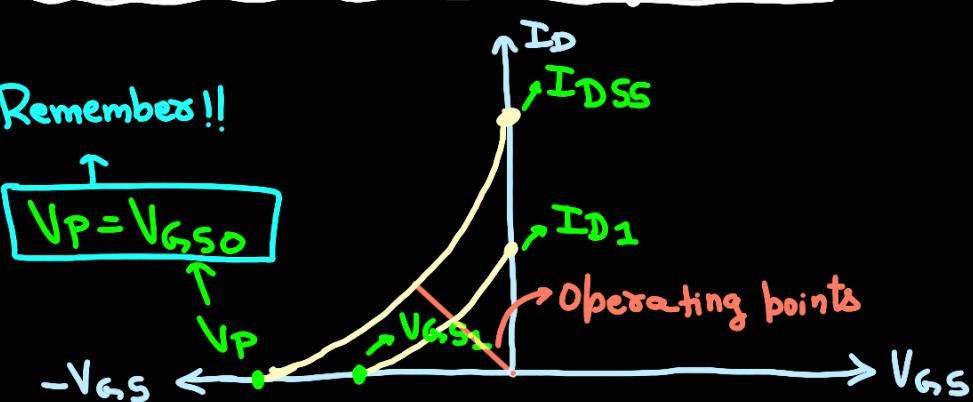
$I_G = 0$  as P-N junction here is operated in reverse bias  
 Only a very small negligible saturation current flows which is  $\approx$  zero

$$M = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

## # Transfer characteristics of JFET:-

# Remember!!

$$\overline{V_P} = V_{GSO}$$



\* O/P resistance =  $\delta_d = \frac{\Delta V_{DS}}{\Delta I_D}$   
 (From O/P char)

\* Transconductance ( $g_m$ ) =  $\frac{I_D}{V_{GS}}$

\* Transconductance ( $g_m$ ) =  $\frac{\Delta I_D}{\Delta V_{GS}}$

$$\begin{aligned} \therefore \mu &= \frac{\Delta V_{DS} \times I_D}{\Delta V_{GS} \quad I_D} \\ &= \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} \\ &\downarrow \quad \downarrow \\ \delta_d & \quad g_m \end{aligned}$$

$\therefore \mu = \delta_d \cdot g_m$

### # Current Equation of JFET:-

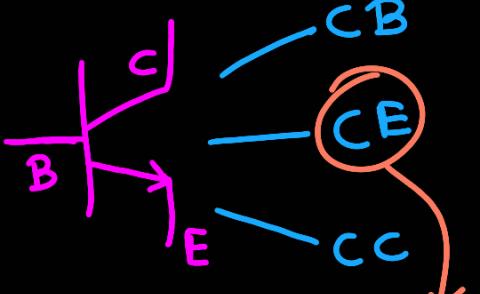
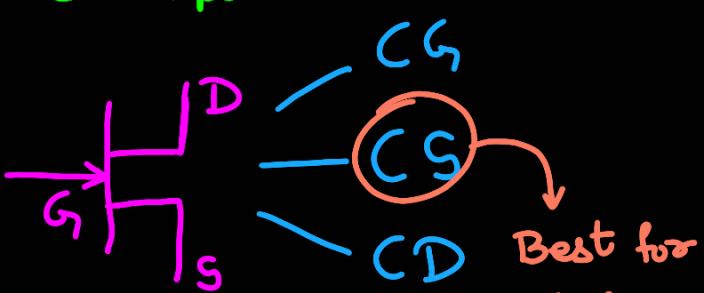
Called  
Shockley's eqn

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

To remember

$$\begin{aligned} V_{DS} &= V_{DD} - I_D (R_s + R_D) \\ V_{GS} &= -V_S = I_S R_S = I_D R_S \\ V_{DS} &= V_D - V_S \end{aligned}$$

### # Difference b/w BJT & JFET:-

BJT	FET
<ul style="list-style-type: none"> <li>Current operated device</li> <li>Both majority &amp; minority carriers are used for conduction Thus "Bipolar"</li> </ul> 	<ul style="list-style-type: none"> <li>Voltage operated Device</li> <li>Only majority carriers are used for conduction Thus "Unipolar"</li> </ul> 
<p>Best for amplifiers</p>	<p>Best for amplifiers</p>

## # JFET Biasing :-

Start of  
AEC notes

- 1) Fixed Bias Config
- 2) Self-Bias Config
- 3) Voltage-Divider Config
- 4) Common Gate configuration

## # Intro to FET Biasing :-

Comparing DC analysis of BJTs & FETs :-

BJT :- Constant

$$I_C = \beta I_B$$

$$I_C \approx I_E$$

$$V_{BE} = 0.7V$$

Q-point :- Linear

i) Mathematical approach

ii) Graphical approach

Non-linear

Same for Depletion type MOSFET

For JFET :-

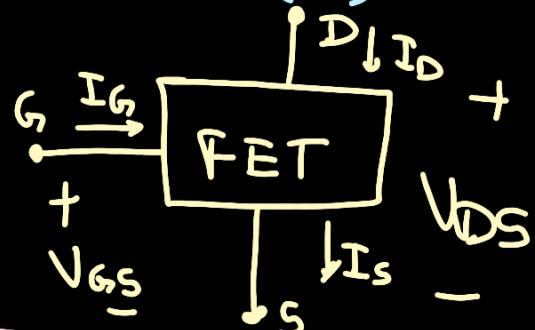
$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

For Enhancement type MOSFET :-

$$I_D = k(V_{GS} - V_T)^2$$

FETs :- Non-linear  
↑ Logarithmic term exists

$$I_D = f(V_{GS})$$



$$I_{GS} = 0A$$

$$I_D = I_S$$

$I_{GS} = 0A \Rightarrow$  High input impedance  $Z_i$

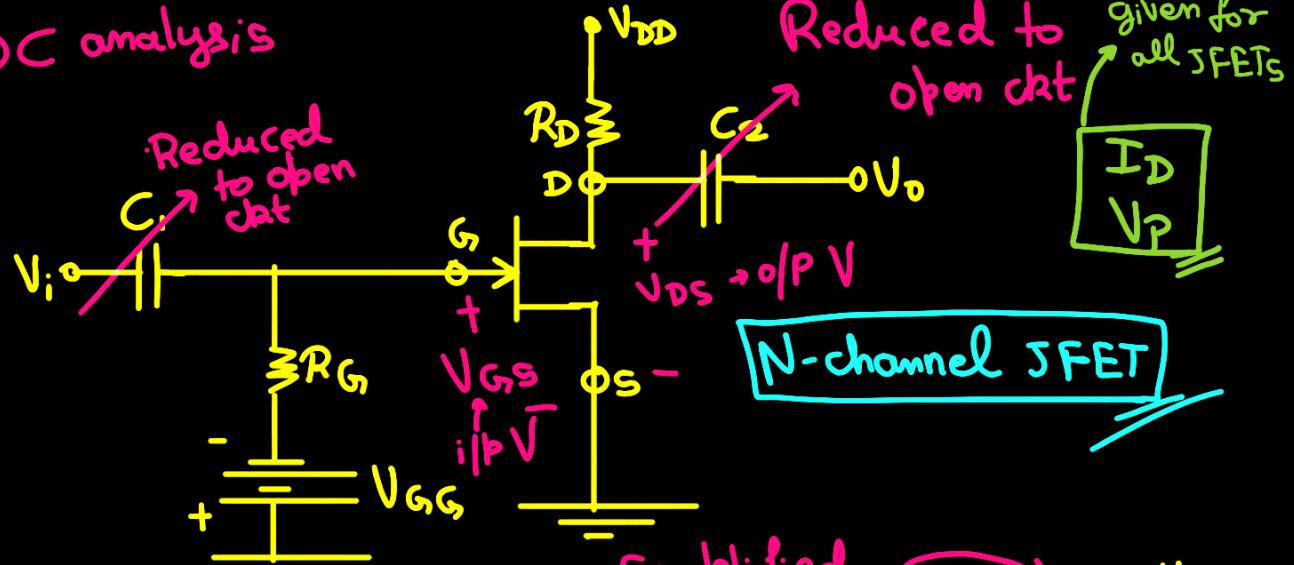
Shockley's eqn

Why DC analysis?  $\Rightarrow$  To find Q-point

Here  $Q = (V_{GSQ}, I_{DQ})$

## # Fixed-Bias Configuration :- ★ Mathematical approach

DC analysis



Simplified for DC analysis

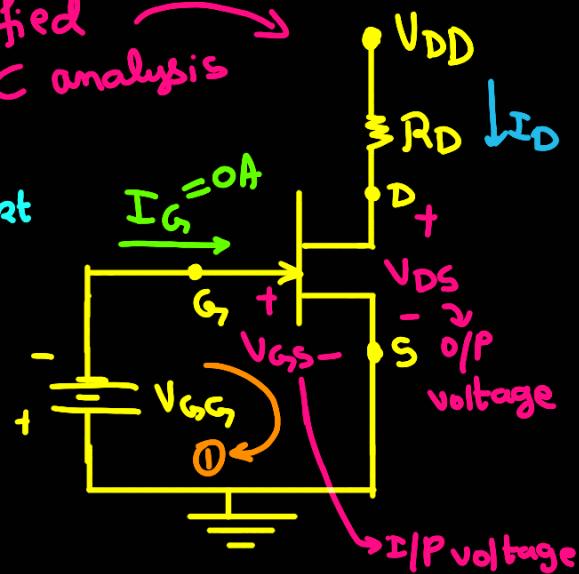
$$V_{RG} = I_G \times R_G = 0 \text{ V} \Rightarrow R_G \approx \text{Short ckt}$$

KVL in loop -1

$$Q = (V_{GSQ}, I_{DQ})$$

$$-V_{GG} - V_{GS} = 0$$

$$V_{GS} = -V_{GG} \rightarrow x\text{-coordinate}$$



Since this is fixed, hence the name of this biasing.

Using JFET (Shockley's eqn)

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

$$\therefore Q = (V_{GSQ}, I_{DQ}) = \left( -V_{GG}, I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \right)$$

Applying KVL in o/p loop (from VDD to GND)

o/p voltage

$$V_{DD} - I_D R_D - V_{DS} = 0 \Rightarrow V_{DS} = V_{DD} - I_D R_D$$

## Graphical approach:-

Shockley's eqn:-  $I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$

Case-i :-  $V_{GS} = 0V$

$$I_D = I_{DSS}$$

$$P_1 \equiv (0, I_{DSS})$$

Case -ii :-

$$I_D = 0A$$

$$V_{GS} = V_P$$

Case -iii :-  $V_{GS} = V_P/2$

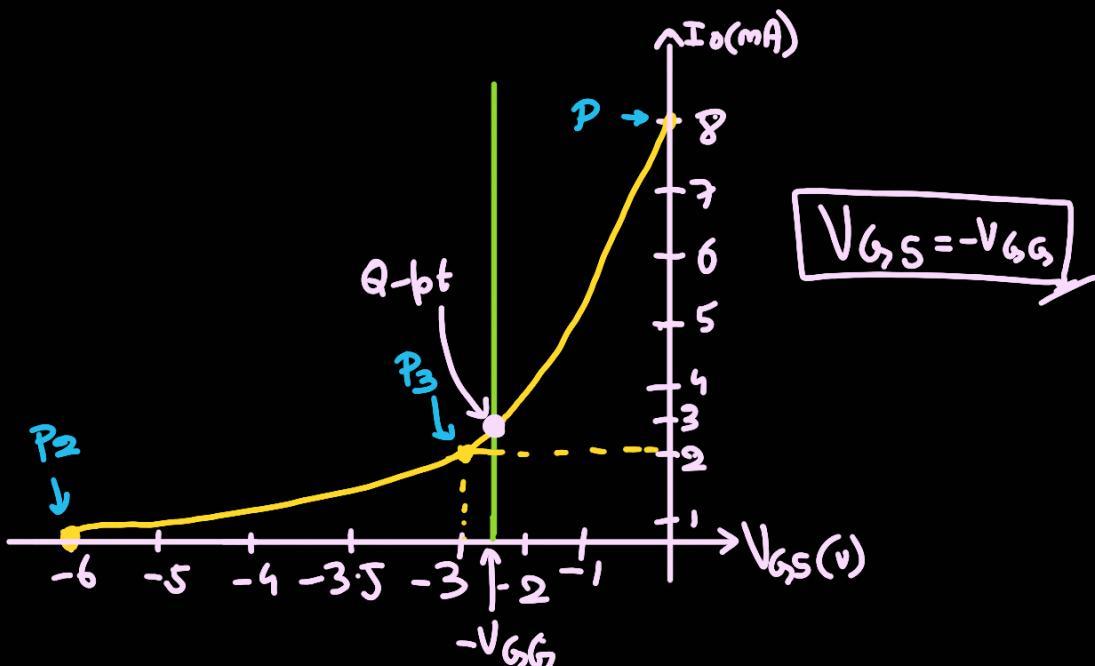
$$I_D = I_{DSS} \left( 1 - \frac{V_P}{2V_P} \right)^2$$

$$P_2 \equiv (V_P, 0)$$

$$I_D = \frac{I_{DSS}}{4}$$

$$P_3 \equiv \left( \frac{V_P}{2}, \frac{I_{DSS}}{4} \right)$$

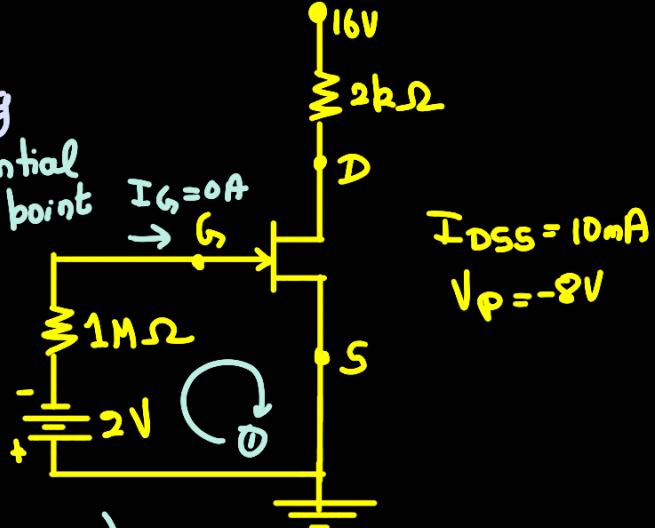
We now plot transfer characteristics



$$Q\text{-pt} = (-V_{GG}, I_{DQ})$$

Q) Determine the following

- a)  $V_{GSQ}$
- b)  $I_{DQ}$
- c)  $V_{DS}$
- d)  $V_D$
- e)  $V_G$
- f)  $V_s$



$$I_{DSS} = 10mA$$

$$V_P = -8V$$

Sol:- Q-point =  $(V_{GSQ}, I_{DQ})$

f)  $V_s = 0V$

a) Apply KVL in loop ①

$$-2V - (0A)(1M\Omega) - V_{GS} = 0$$

$$\Rightarrow \boxed{V_{GS} = -2V} = V_{GSQ}$$

c)  $V_{GS} = V_G - V_s$

$$-2 = V_G - 0 \Rightarrow \boxed{V_G = -2V}$$

b)  $I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 = 10mA \left( 1 - \left( \frac{-2V}{-8V} \right)^2 \right)$

$$\Rightarrow \boxed{I_D = 5.625mA} = I_{DQ}$$

c) Apply KVL in o/p loop

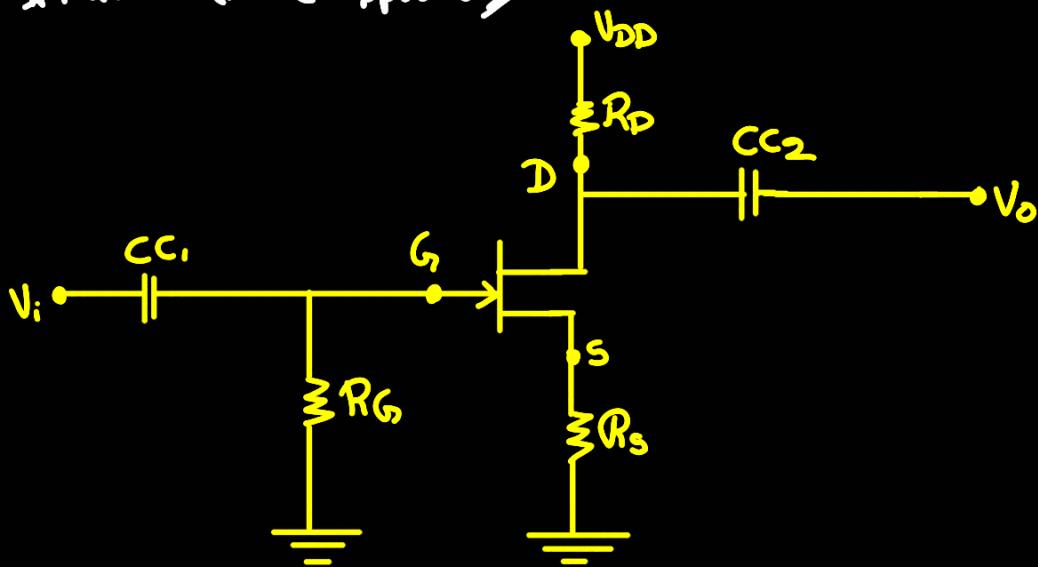
$$16 - (5.625mA)(2k\Omega) - V_{DS} = 0$$

$$\Rightarrow \boxed{V_{DS} = 4.75V}$$

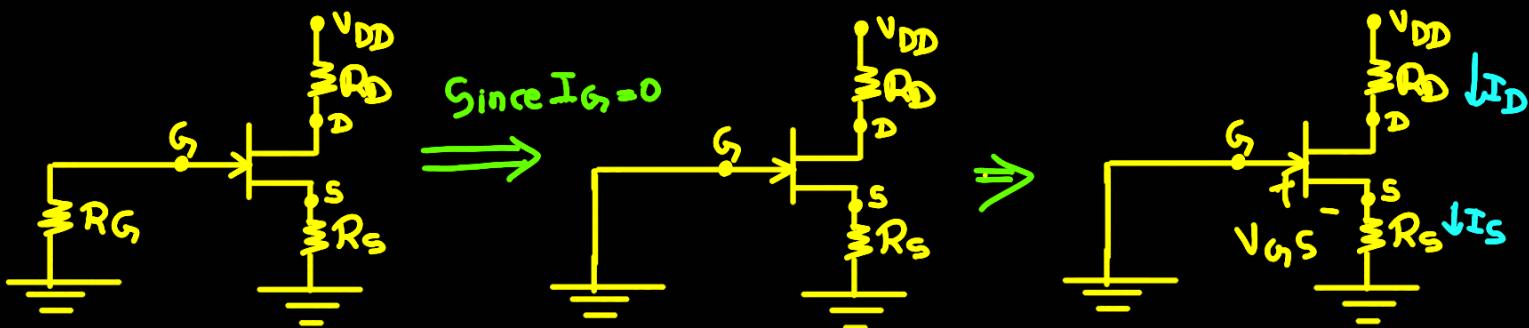
d)  $V_{DS} = V_D - V_s \Rightarrow 4.75 = V_D - 0 \Rightarrow \boxed{V_D = 4.75V}$  Ans.

## # Self Bias Configuration :-

★ Mathematical Approach



Simplifying for DC analysis.



$$Q-Pt = (V_{GSQ}, I_{DQ})$$

KVL in i/p loop

$$-V_{GS} - V_{RS} = 0 \\ \text{WKT, } I_D = I_S$$

$$\Rightarrow -V_{GS} - V_{RS} = 0 \Rightarrow -V_{GS} - I_S R_S = 0 \Rightarrow -V_{GS} - I_D R_S = 0 \\ \boxed{\underline{\underline{V_{GS} = -I_D R_S}}}$$

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \Rightarrow I_D = I_{DSS} \left( 1 + \frac{I_D R_S}{V_P} \right)^2$$

$$I_D = \frac{I_{DSS}}{2} \left( V_P + I_D R_S \right)^2$$

$$\Rightarrow I_D = \frac{I_{DSS}}{V_P^2} \left( V_P^2 + I_D^2 R_S + 2V_P I_D R_S \right)$$

$$I_D = I_{DSS} + \frac{I_{DSS}^2 R_S}{V_P^2} I_D^2 + 2 \frac{I_{DSS} R_S}{V_P} I_D$$

$$0 = \left( \frac{I_{DSS}^2 R_S}{V_P^2} \right) I_D^2 + \left( \frac{2 I_{DSS} R_S}{V_P} - 1 \right) I_D + I_{DSS} = 0$$

$$\div \text{ by } \frac{I_{DSS}^2 R_S}{V_P^2}$$

$$\Rightarrow I_D^2 + \left( \frac{\frac{2 I_{DSS} R_S - V_P}{V_P}}{\frac{I_{DSS}^2 R_S}{V_P^2}} \right) I_D + \frac{\frac{V_P^2}{R_S}}{K_2} = 0$$

$K_1$       Constant       $K_2$

$$\Rightarrow I_D^2 + K_1 I_D + K_2 = 0$$

Solving this quadratic eqn  
we get  $I_D //$

Apply KVL in O/P loop.

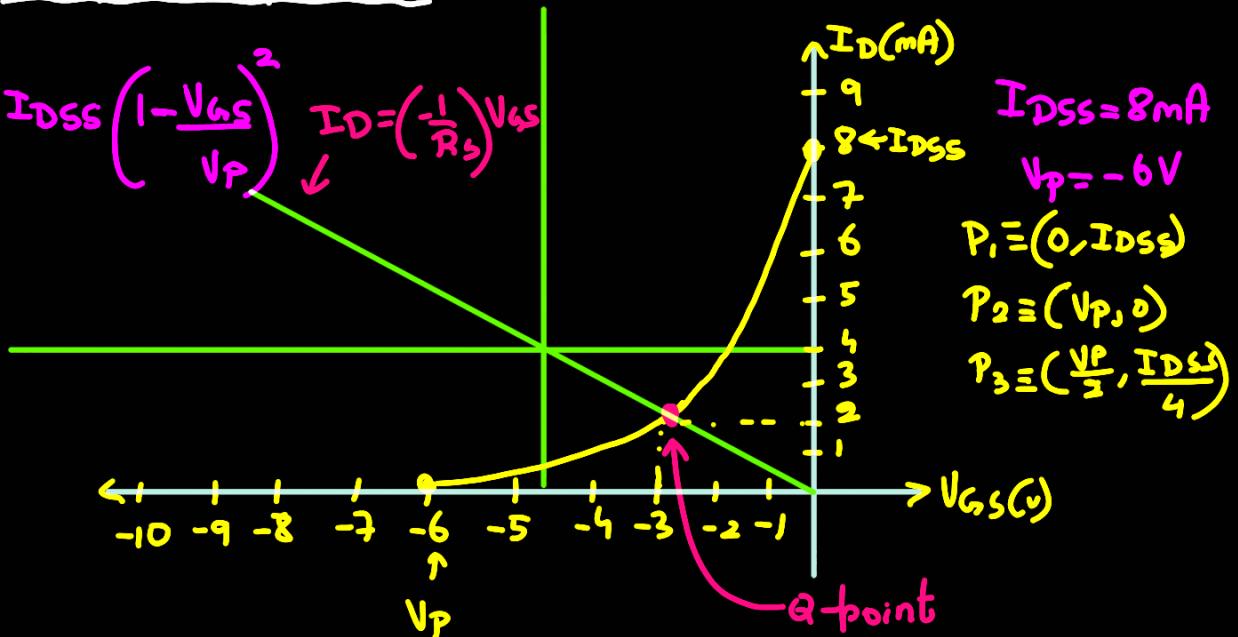
$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\Rightarrow V_{DS} = V_{DD} - I_D (R_D + R_S)$$

O/P voltage

## \* Graphical approach :-

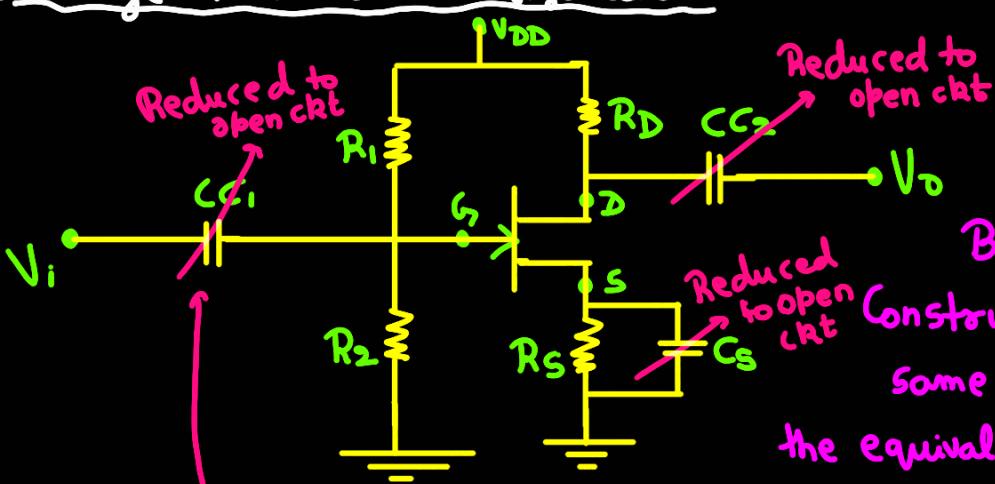
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad I_D = \left(\frac{-1}{R_S}\right) V_{GS}$$



$$y = mx + c$$

$$\begin{aligned} V_{GS} &= -I_D R_S \quad \Rightarrow \quad I_D = \left(\frac{-1}{R_S}\right) V_{GS} \\ V_{GS} &= 0 \quad \left| \begin{array}{l} I_D = I_{DSS}/2 \\ V_{GS} = -\frac{I_{DSS} R_S}{2} \end{array} \right. \\ I_D &= 0 \text{ A} \end{aligned}$$

## # Voltage Divider Bias Configuration:-



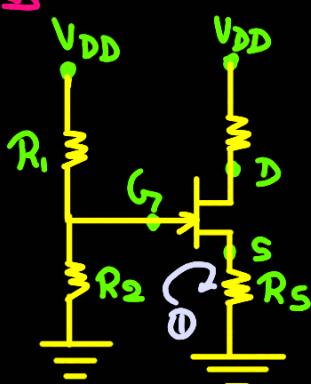
All capacitors  $\rightarrow$  open ckt

$\nwarrow$  Simplified for DC analysis

Since  $I_G \approx 0 \text{ mA}$

$R_1 \& R_2$  have series connection.

Basic  
Construction is  
same as that of  
the equivalent BST ckt,  
 $\downarrow$   
DC analysis is different



$$I_1 = I_2 + I_G \Rightarrow I_1 = I_2 = I$$

$$R_{eq} = R_1 + R_2$$

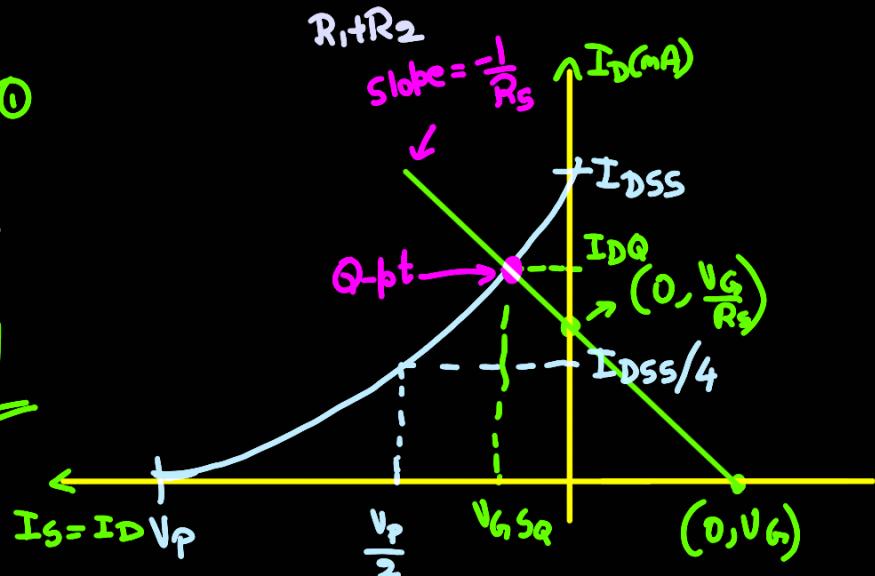
$$I = \frac{V}{R} = \frac{V_{DD}}{(R_1 + R_2)}$$

Voltage drop across  $R_2 = I \times R_2 = R_2 V_{DD}$

Apply KVL in loop ①

$$V_G - V_{GS} - I_D R_S = 0$$

$$\boxed{V_{GS} = V_G - I_D R_S}$$

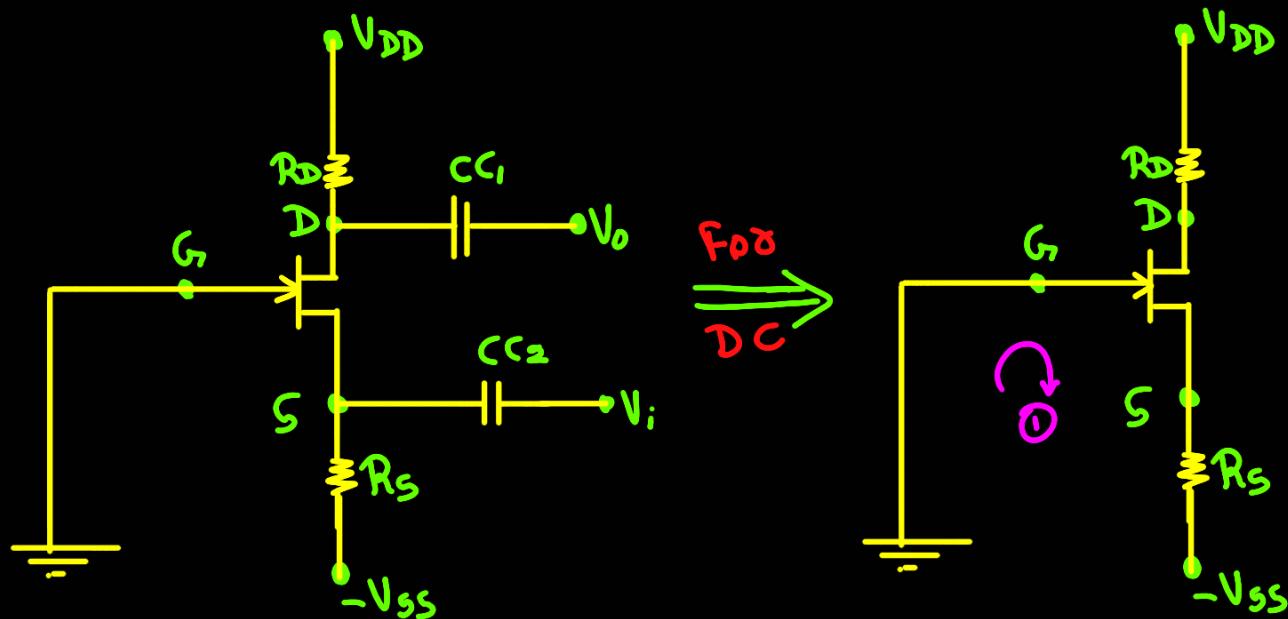


$$y = mx + c$$

$$I_D = \left( -\frac{1}{R_S} \right) V_{GS} + \frac{V_G}{R_S}$$

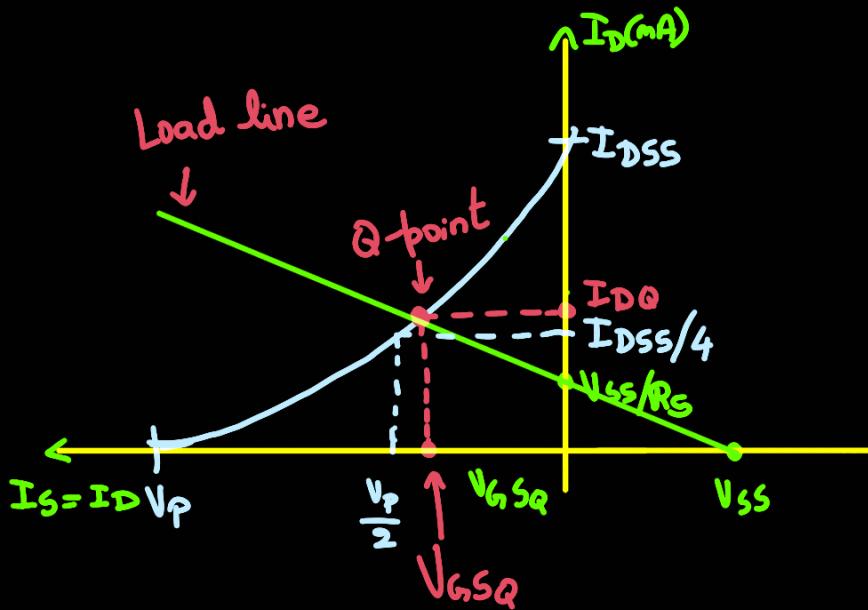
$$y = mx + c$$

### # Common Gate Configuration :-



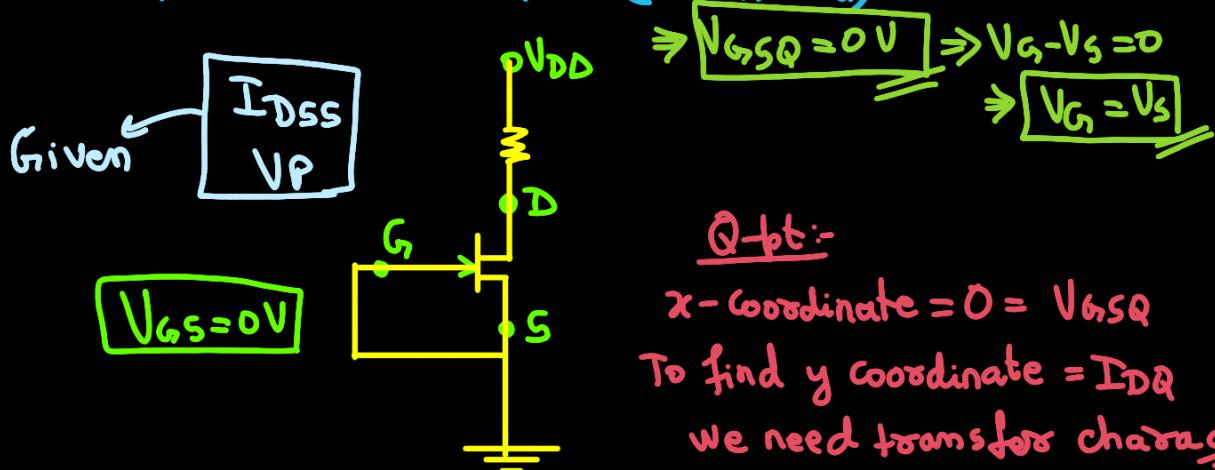
Apply KVL in loop ①

$$0 - V_{GS} - I_D R_S = -V_{SS} \Rightarrow V_{GS} = V_{SS} - I_D R_S \Rightarrow I_D = \left( -\frac{1}{R_S} \right) V_{GS} + \frac{V_{SS}}{R_S}$$



# JFET biasing (Special case):

Special case  $\Rightarrow$  Q-pt  $\equiv (V_{GSQ}, I_{DQ})$



Q-pt :-

x-coordinate  $= 0 = V_{GSQ}$

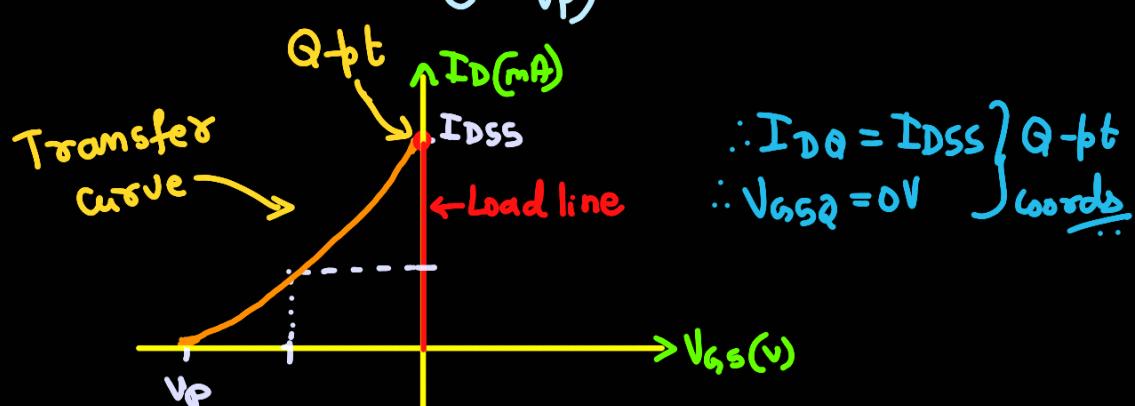
To find y coordinate  $= I_{DQ}$

We need transfer charac. graph

& load line.

Using Shockley's eqn:-  $I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2$

Same 3 pts from  
above graphs //



## # Small signal model of JFET :-

$$\text{Shockley's eqn} :- I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

The change in drain current will result from a change in gate to source voltage, can be determined using transconductance factor ( $g_m$ )

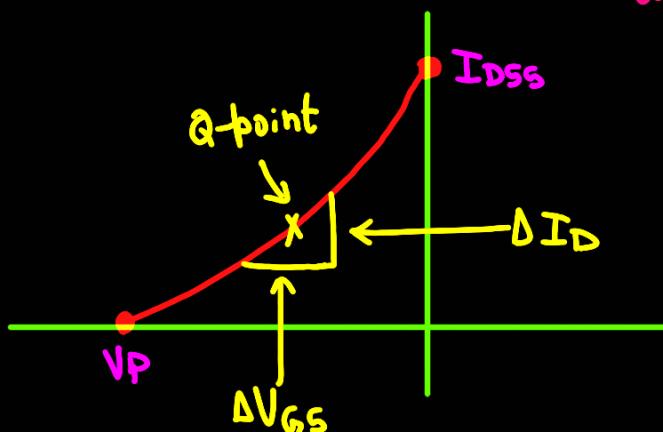
$$\Delta I_D = g_m \Delta V_{GS} \Rightarrow g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Trans conductance  
↳ Current to voltage ratio.

blw of & i/p quantity

## \* Graphical Determination of $g_m$

From eqn  $\Delta I_D = g_m \Delta V_{GS} \Rightarrow g_m$  is slope of characteristics graph at operating point



$g_m \uparrow^\infty$  as we progress from  $V_P$  to  $I_{DSS} \Rightarrow$  As  $V_{GS} \rightarrow 0$   
 $\Rightarrow g_m \uparrow^\infty$  in value

## \* Mathematical definition of $g_m$ :-

WKT, the derivative of a  $f^n$  at a point is equal to the slope of the tangent line drawn at that point.

Taking the derivative of  $I_D$  w.r.t  $V_{GS}$  using Shockley's eqn

$$g_m = \left. \frac{d I_D}{d V_{GS}} \right|_{Q-pt} = \frac{d}{d V_{GS}} \left[ I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \right]$$

$$= 2 I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right) \left( -\frac{1}{V_P} \right)$$

$$\therefore g_m = \frac{2 I_{DSS}}{|V_P|} \left[ 1 - \frac{V_{GS}}{V_P} \right]$$

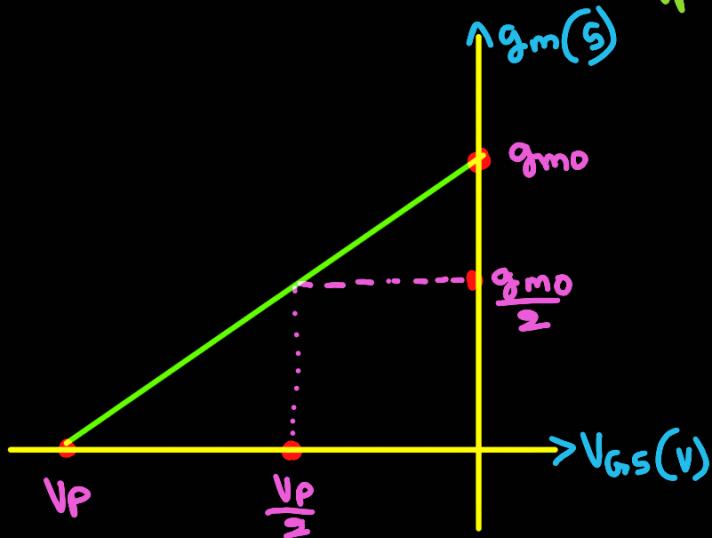
Maximum value of slope ( $g_m$ ) is when  $V_{GS} = 0V$ .

$$\therefore g_{m0} = \frac{2 I_{DSS}}{|V_P|}$$

$$\Rightarrow g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right]$$

Since  $\left( 1 - \frac{V_{GS}}{V_P} \right)$  is  $< 1$  for any value of  $V_{GS} > 0V$ ,

$g_m$  will decrease as  $V_{GS} \rightarrow V_P$  &  $\frac{V_{GS}}{V_P}$  will increase in magni.



## Relation b/w $I_D$ & $g_m$ :

From Shockley's Eq<sup>n</sup>, we get

$$\frac{1 - V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$\therefore g_m = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}}$$

## JFET input impedance $Z_i$ :

$$Z_i(\text{JFET}) = \infty \Omega$$

$$\text{Practically } Z_i = 10^9 \Omega$$

## JFET o/p impedance:-

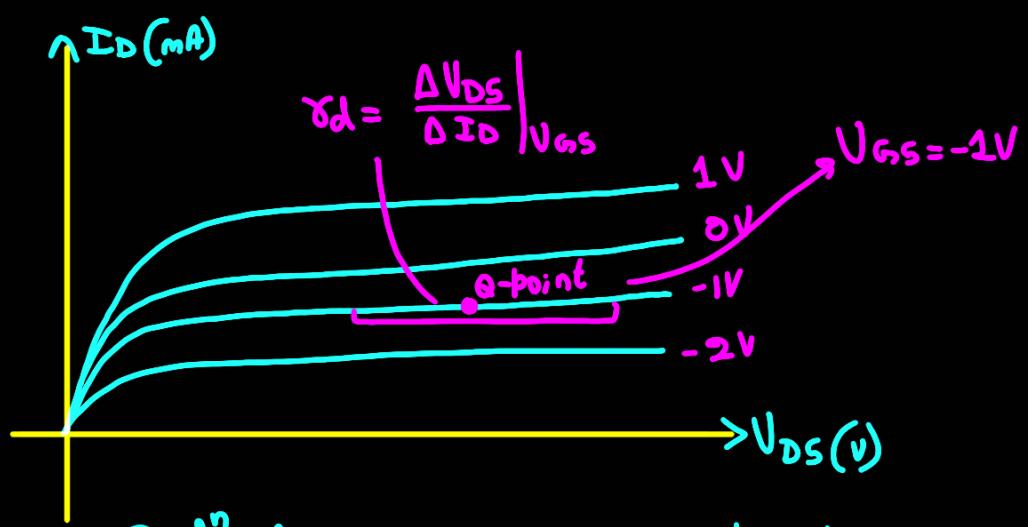
$$Z_o(\text{JFET}) = \gamma_d = \frac{1}{g_{os}} = \frac{1}{y_{os}}$$

Component of admittance equivalent ckt

$y_{os}$   
o/p network parameters

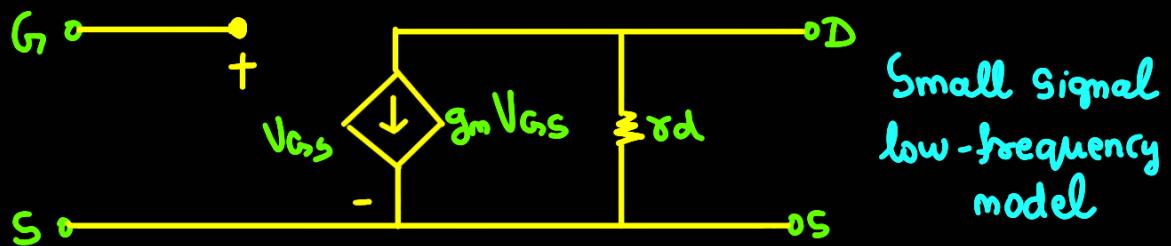
Source  $\Rightarrow$  it is attached to it in the model

$$\gamma_d = \frac{\Delta V_{DS}}{\Delta I_D} \quad \boxed{V_{GS} = \text{constant}}$$



Def<sup>n</sup> of  $r_d$  in JFET characteristics.

### JFET AC equivalent circuit:-



The control of  $I_d$  by  $V_{GS}$  is included as the current source  $g_m V_{GS}$  connected from drain to source, with arrow pointing down to establish a  $180^\circ$  phase shift b/w o/p & i/p voltages.

→ I/P impedance is represented by open ckt at i/p terminal

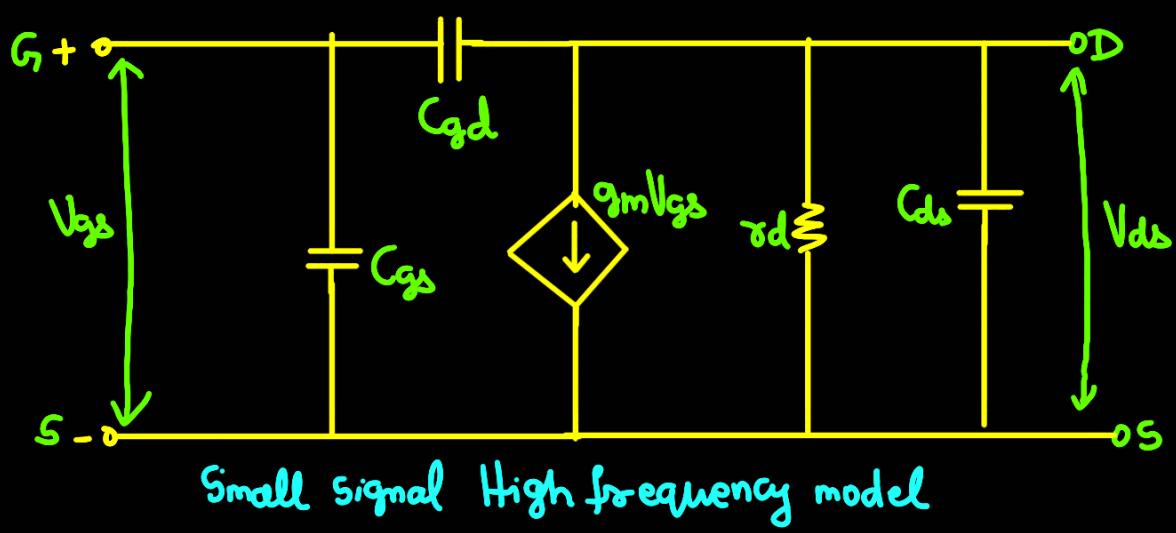
→ O/P impedance  $\gg r_d$

→ Gate & drain are in touch through current controlled source  $g_m V_{GS}$   
To small letters to indicate AC

→ If  $r_d$  is ignored, i.e., when it is large in relation to other elements of the network

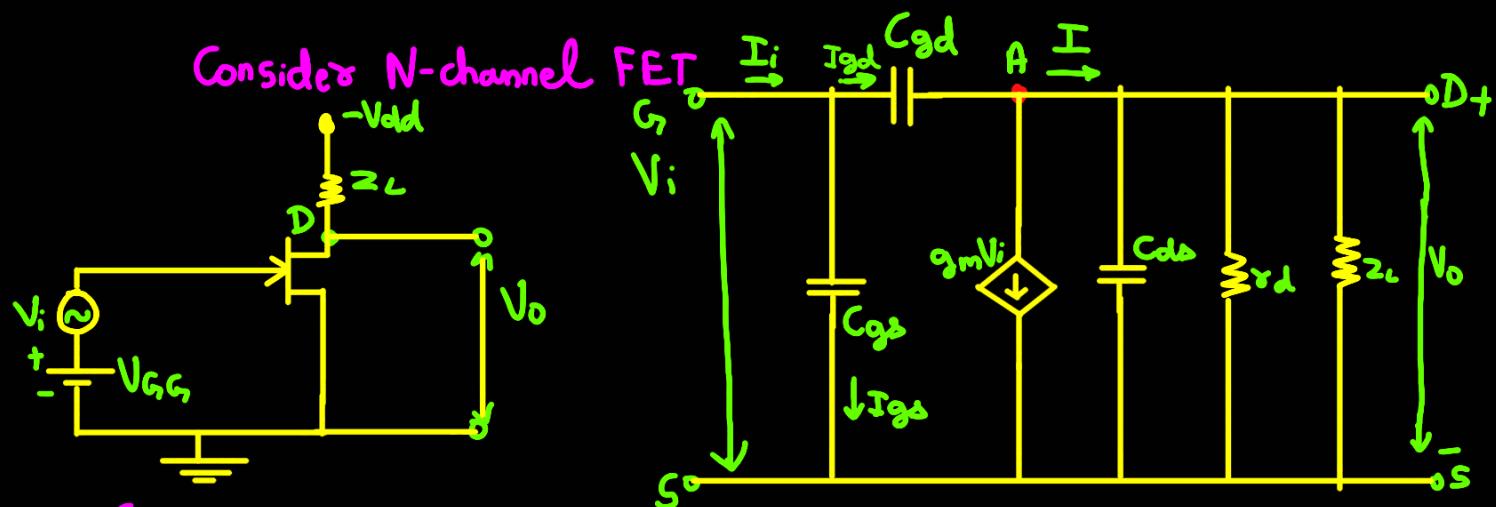
⇒ The equivalent circuit is simply a current source whose magnitude is controlled by  $V_{GS}$  →

It is a voltage controlled current source



### # Common Source (CS) Amplifier :-

↪ Ckt discussed is applicable to JFET & MOSFET unless specified.



Common Source  
amplifiers

Small Signal high frequency equivalent  
ckt of CS amplifiers

### Voltage Gain:-

Parallel combination of  $Z_L$ ,  $C_{DS}$ ,  $\gamma_d$  can be replaced by an impedance  $Z$  b/w D & S as follows:-

$$Z = \frac{1}{Y_L + Y_{DS} + g_d}$$

where :-  $Y_L = 1/Z_L$  = Admittance corresponding to  $Z_L$

$Y_{DS} = j\omega C_{DS}$  = Admittance corresponding to  $C_{DS}$

$g_d = 1/\gamma_d$  = Conductance corresponding to  $\gamma_d$

Voltage across  $C_{gd}$  is  $V_i - V_o$  & since voltages at A & D are same as  $V_o$ , we get

$$I_{gd} = Y_{gd}(V_i - V_o)$$

where  $Y_{gd} = j\omega C_{gd}$

Apply KCL at node A

$$I = -g_m V_i + I_{gd} = (-g_m + Y_{gd}) V_i - Y_{gd} V_o$$

$$V_o = I \Rightarrow V_o = \frac{(-g_m + Y_{gd}) V_i - Y_{gd} V_o}{Y_L + Y_{ds} + g_d}$$

$$AV = \frac{V_o}{V_i} = \frac{-g_m + Y_{gd}}{Y_L + Y_{ds} + g_d + Y_{gd}}$$

At high frequencies

At low frequencies, capacitances can be neglected

$$\Rightarrow Y_{ds} = Y_{gd} = 0$$

$$\therefore AV = \frac{-g_m}{Y_L + g_d} = \frac{-g_m Z_L}{1 + g_d Z_L} = -g_m Z'_L$$

where  $Z'_L = \tau_d // Z_L$

\* Input admittance:-

Current through capacitor  $C_{gs} = I_{gs} = Y_{gs} V_i$

$$\therefore I_i = I_{gs} + I_{gd} = Y_{gs} V_i + Y_{gd} (V_i - V_o) \rightarrow ①$$

where  $Y_{gs} = j\omega C_{gs}$

I/P admittance =  $\gamma_i = \frac{I_i}{V_i}$

÷ ① by  $V_i$

$$\Rightarrow Y_i = Y_{gs} + Y_{gd}(1-A_v) \rightarrow \text{I/P admittance}$$

## Miller Effect Capacitance / Input capacitance

Part of Unit-2

Consider FET with drain-dkt resistance  $R_d$

$$\Rightarrow \text{Gain } A_v = -g_m R'_d$$

$$\text{where } R'_d = R_d // \tau_d$$

$\therefore$  I/P admittance eqn becomes

$$Y_i = C_i = C_{gs} + (1+g_m R'_d) C_{gd}$$

$j\omega$

This increase in  $C_i$  over  $C_{gs}$  is due to Miller Effect

I/P capacitance is most important in the operation of cascaded amplifier where o/p from one amplifier stage is used as i/p to a second amplifier.

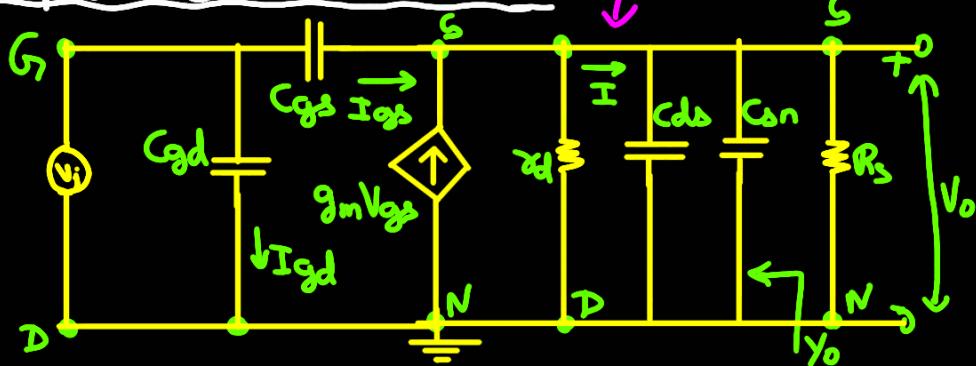
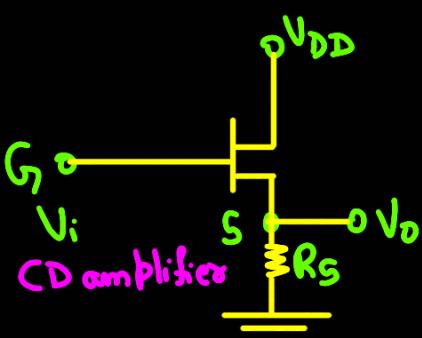
Output resistance :- o/p resistance  $R_o$  is  $\tau_d // R_d$

$$\Rightarrow R_o = \frac{\tau_d R_d}{\tau_d + R_d}$$

where  $Z_L = R_d$

# Common Drain Amplifier Source Follower :-

Small signal high freq equivalent model



$\Rightarrow$  Voltage Gain:  $A_v = \frac{V_o}{V_i}$  is determined similarly to CS amplifier

$$Z = \frac{1}{(g_d + j\omega(C_{ds} + C_n) + 1/R_s)}$$

$$I_{gs} = j\omega C_{gs}(V_i - V_o) \quad \& \quad I = I_{gs} + g_m(V_i - V_o)$$

$$\text{From } V_o = IZ$$

$$V_o = \frac{(g_m + j\omega C_{gs})(V_i - V_o)}{g_d + j\omega(C_{ds} + C_n) + 1/R_s}$$

$$A_v = \frac{V_o}{V_i} = \frac{(g_m + j\omega C_{gs})R_s}{1 + (g_m + g_d + j\omega C_T)R_s}$$

$$\text{where } C_T = C_{gs} + C_{ds} + C_n$$

At low frequencies,  $A_v$  becomes

$$A_v = \frac{g_m R_s}{1 + (g_m + g_d)R_s}$$

$\Rightarrow$  I/O admittance:-

Source follower offers an important advantage of lower input capacitance than the CS amplifier.

$$\therefore I_{gd} = j\omega C_{gd} V_i ; \quad I_{gs} = j\omega C_{gs}(V_i - V_o)$$

$$I_i = I_{gd} + I_{gs} = (j\omega(C_{gd} + j\omega C_{gs}(1 - A_v)))V_i$$

$$\text{O/P admittance } Y_i = \frac{I_i}{V_i}$$

$$\Rightarrow Y_i = j\omega C_{gd} + j\omega C_{gs}(1 - A_v)$$

I/O admittance:-

$Y_o$  with  $R_s$ , taking interelectrode capacitances into account is obtained by adding  $g_m + g_d$  of total shunting capacitance  $C_T$

At low freqy

$$Y_o = g_m + g_d + C_T$$

$$R_o = \frac{1}{g_m + g_d} \approx \frac{1}{g_m}$$

Large signal amplifiers also known as power amplifiers are capable of providing large amount of power to the load. They are used as last stage in electronic systems. A power amplifier takes the d.c. power supply connected to the output circuit and converts it into a.c. signal power. Output power is controlled by input signal.

## Important Features of Power Amplifiers:

- Some of the features of power amplifiers are
- Impedance matching with the load is necessary for delivering max power to the load.
- Power transistors are needed. (To withstand large voltages and currents)
- Power amplifiers are bulk.
- Due to the non-linear characteristics of transistors, Harmonic Distortions are available at the output.

## Classification of power amplifiers

For an amplifier, a quiescent operating point (Q point) is fixed by selecting the proper d.c. biasing to the transistors used. The quiescent operating point is shown on the load line, which is plotted on the output characteristics of the transistor. The position of the quiescent point on the load line decides the class of operation of the power amplifier. The various classes of the power amplifiers are :

- i) Class A
- ii) Class B
- iii) Class C and
- iv) Class AB

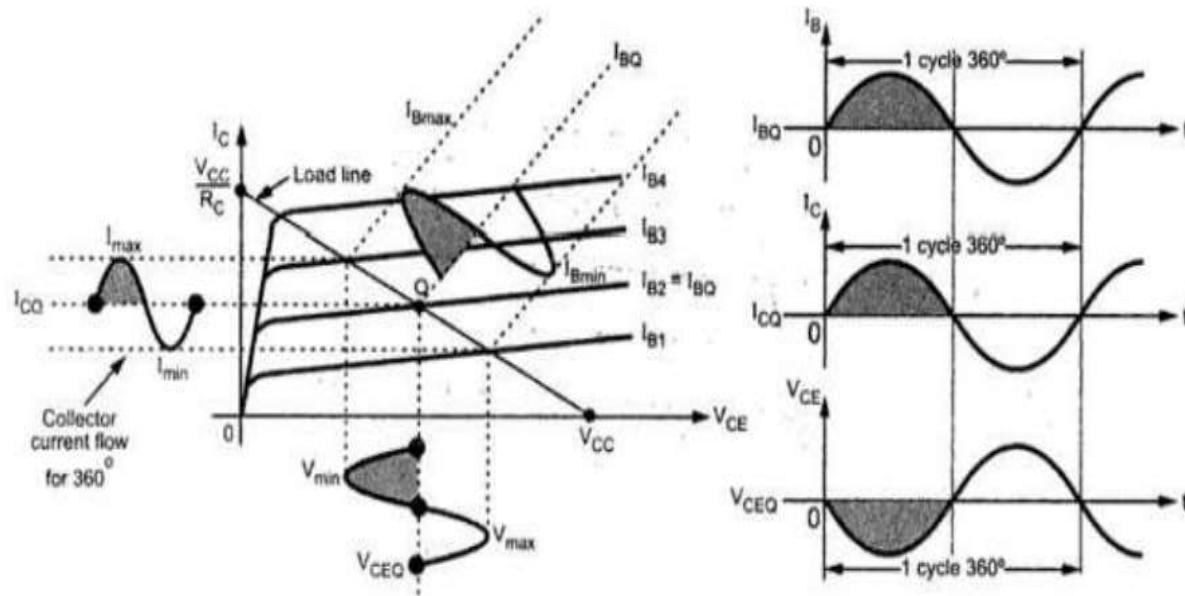
### Class A amplifiers:

The power amplifier is said to be class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input cycle.

**Key Point:** *For this class, position of the Q point is approximately at the midpoint of the load line.*

For all values of input signal, the transistor remains in the active region and never enters into cut-off or saturation region. When an a.c. input signal is applied, the collector voltage varies sinusoidally hence the collector current also varies sinusoidally. The collector current flows for  $360^\circ$  (full cycle) of the input signal. In other words, the angle of the collector current flow is  $360^\circ$  i.e. one full cycle.

## Waveforms representing class A operation



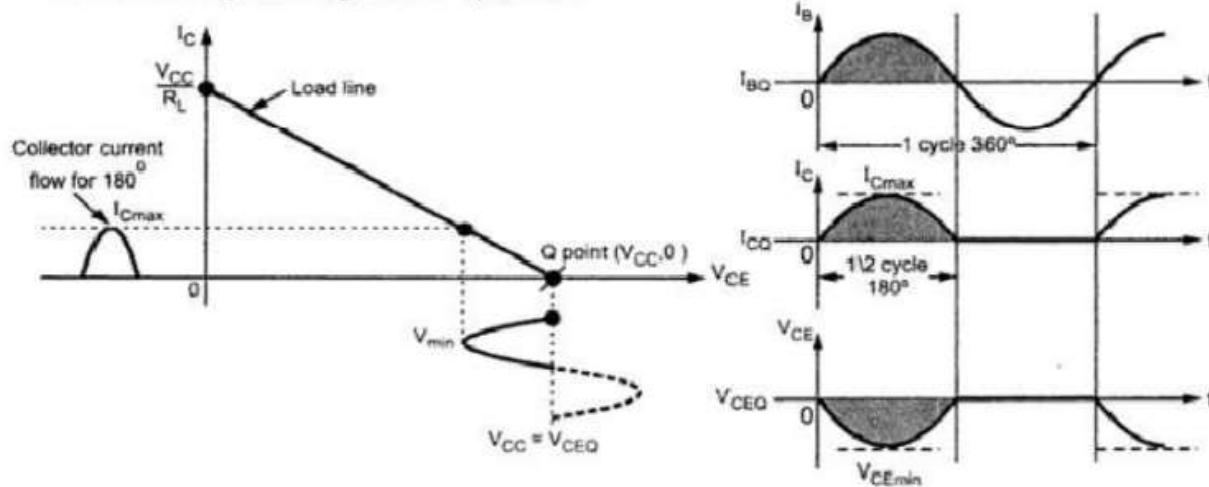
## Class B amplifiers:

The power amplifier is said to be class B amplifier if the Q point and the input signal are selected, such that the output signal is obtained only for one half cycle for a full input cycle.

**Key Point:** For this operation, the Q point is shifted on X-axis i.e. transistor is biased to cut-off.

Due to the selection of Q point on the X-axis, the transistor remains, in the active region, only for positive half cycle of the input signal. Hence this half cycle is reproduced at the output. But in a negative half cycle of the input signal, the transistor enters into a cut-off region and no signal is produced at the output. The collector current flows only for  $180^\circ$  (half cycle) of the input signal. In other words, the angle of the collector current flow is  $180^\circ$  i.e. one half cycle.

Waveforms representing class B operation

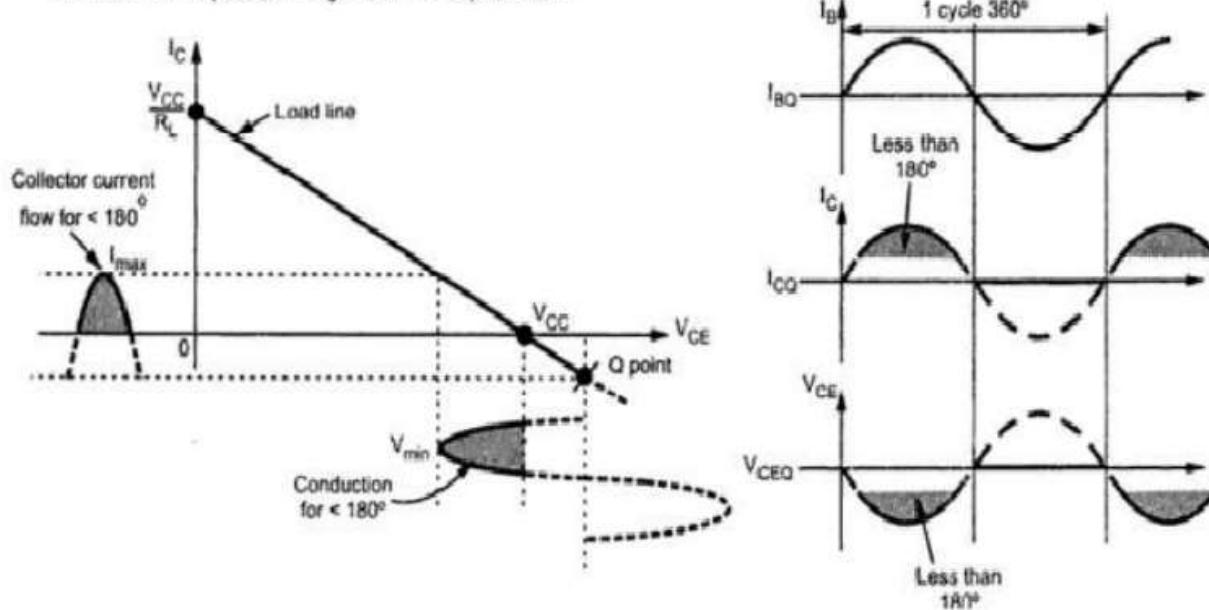
**Class C amplifiers:**

The power amplifiers is said to be class C amplifier, if the Q point and the input signal are selected such that the output signal is obtained for less than a half cycle, for a full input cycle.

**Key Point:** For this operation, the Q point is to be shifted below X-axis.

Due to such a selection of the Q point, transistor remains active, for less than a half cycle. Hence only that much part is reproduced at the output. For remaining cycle of the input cycle, the transistor remains cut-off and no signal is produced at the output. The angle of the collector current flow is less than 180°.

Waveform representing class C operation

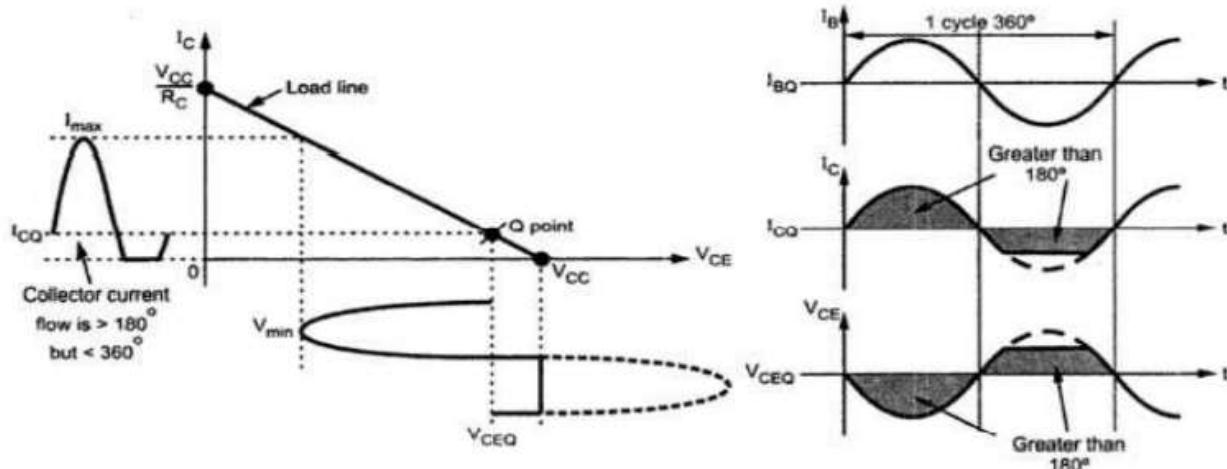


### Class AB amplifiers:

The power amplifier is said to be class AB amplifier, if the Q point and the input signal are selected such that the output signal is obtained for more than  $180^\circ$  but less than  $360^\circ$ , for a full input cycle.

**Key Point:** The Q point position is above X-axis but below the midpoint of a load line.

Waveforms representing class AB operation



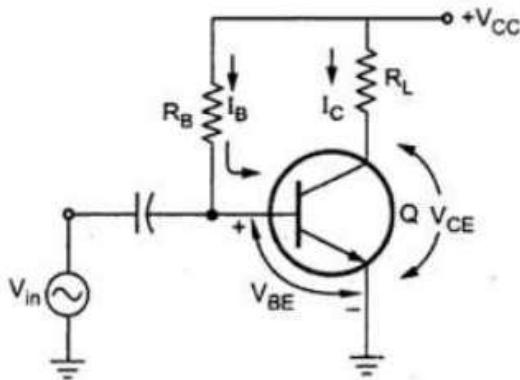
### Comparison of amplifier classes

Class	A	B	C	AB
Operating Cycle	$360^\circ$	$180^\circ$	Less than $180^\circ$	$180^\circ$ to $360^\circ$
Position of Q point	Centre of load line	On X axis	Below X axis	Above X-axis but below the centre of load line
Efficiency	Poor, 25% to 50%	Better, 78.5%	High	Higher than A but less than B 50% to 78.5%
Distortion	Absent No distortion	Present More than class A	Highest	Present

Series fed, directly coupled class A amplifier:

► **Figure 5.13**

Large signal class A amplifier



A simple fixed-bias circuit can be used as a large signal class A amplifier as shown in the Fig. 5.13.

The difference between small signal version of this circuit is that the signals handled by this large signal circuit are of the order of few volts. Similarly the transistor used, is a power transistor. The value of  $R_B$  is selected in such a way that the Q point lies at the centre of the d.c. load line.

The circuit represents the directly coupled class A amplifier as the load resistance is directly connected in the collector circuit. Most of the times the load is a loudspeaker, the

impedance of which varies from 3 to 4 ohms to 16 ohms. The beta of the transistor used is less than 100.

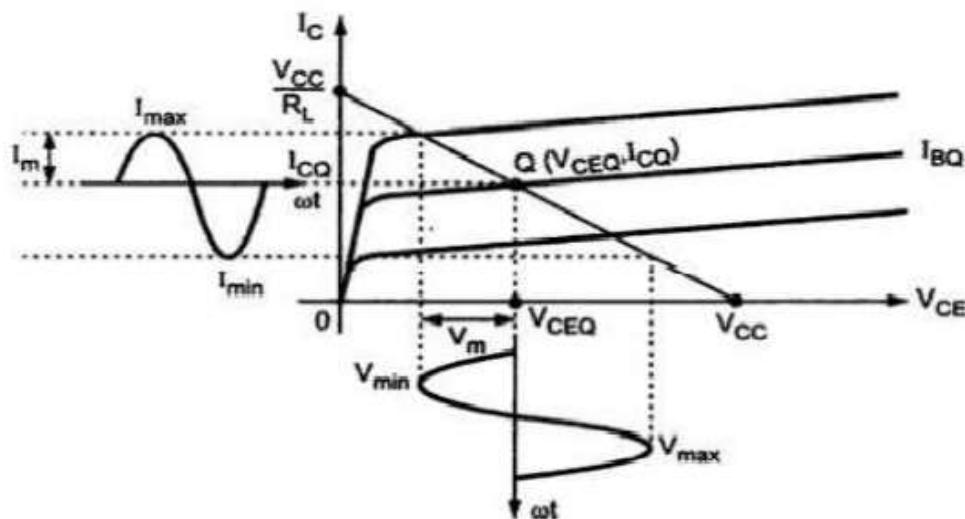
**Key Point:** This is called *directly coupled*, as the load  $R_L$  is directly connected in the collector circuit of power transistor.

The overall circuit handles large power, in the range of a few to tens of watts without providing much voltage gain.

The graphical representation of a class A amplifier is shown in the Fig. 5.14.

► **Figure 5.14**

Graphical representation of class A amplifier



Applying Kirchhoff's voltage law to the circuit shown in the Fig. 5.13, we get

$$\begin{aligned} V_{CC} &= I_C R_L + V_{CE} \\ \therefore I_C R_L &= -V_{CE} + V_{CC} \\ \therefore I_C &= \left[ -\frac{1}{R_L} \right] V_{CE} + \frac{V_{CC}}{R_L} \quad \dots (1) \end{aligned}$$

The equation is similar to equation (1) of section 7.3 and thus the slope of the load line is  $-\frac{1}{R_L}$  while the Y-intercept is  $\frac{V_{CC}}{R_L}$ .

The change is because the collector resistance  $R_C$  is named as load resistance  $R_L$  in this circuit. The Q point is adjusted approximately at the centre of the load line.

### DC operation:

The collector supply voltage  $V_{CC}$  and resistance  $R_B$  decides the d.c. base-bias current  $I_{BQ}$ . The expression is obtained applying KVL to the B-E loop and with  $V_{BE} = 0.7$  V.

$$\therefore I_{BQ} = \frac{V_{CC} - 0.7}{R_B} \quad \dots (2)$$

The corresponding collector current is then,

$$I_{CQ} = \beta I_{BQ} \quad \dots (3)$$

From the equation (1), the corresponding collector to emitter voltage is,

$$V_{CEQ} = V_{CC} - I_{CQ} R_L \quad \dots (4)$$

Hence the Q point can be defined as Q ( $V_{CEQ}$ ,  $I_{CQ}$ ).

### D.C power input:

The d.c. power input is provided by the supply. With no a.c input signal, the d.c. current drawn is the collector bias current  $I_{CQ}$ . Hence d.c. power input is,

$$P_{DC} = V_{CC} I_{CQ} \quad \dots (5)$$

It is important to note that even if a.c. input signal is applied, the average current drawn from the d.c. supply remains same. Hence equation (5) represents d.c. power input to the class A series fed amplifier.

**A.C operation:**

When an input a.c. signal is applied, the base current varies sinusoidally.

Assuming that the nonlinear distortion is absent, the nature of the collector current and collector to emitter voltage also vary sinusoidally as shown graphically in the Fig. 5.14.

The output current i.e. collector current varies around its quiescent value while the output voltage i.e. collector to emitter voltage varies around its quiescent value. The varying output voltage and output current deliver an a.c. power to the load. Let us find the expressions for the a.c. power delivered to the load.

**A.C power output:**

For an alternating output voltage and output current swings, shown in the Fig. 5.14, we can write,

$V_{\min}$  = Minimum instantaneous value of the collector (output) voltage

$V_{\max}$  = Maximum instantaneous value of the collector (output) voltage

and  $V_{pp}$  = Peak to peak value of a.c. output voltage across the load.

$$\therefore V_{pp} = V_{\max} - V_{\min} \quad \dots (6)$$

Now  $V_m$  = Amplitude (peak) of a.c. output voltage as shown in the Fig. 5.14.

$$\boxed{\therefore V_m = \frac{V_{pp}}{2} = \frac{V_{\max} - V_{\min}}{2}} \quad \dots (7)$$

Similarly we can write for the output current as,

$I_{\min}$  = Minimum instantaneous value of the collector (output) current

$I_{\max}$  = Maximum instantaneous value of the collector (output) current

and  $I_{pp}$  = Peak to peak value of a.c. output (load) current

$$\therefore I_{pp} = I_{\max} - I_{\min} \quad \dots (8)$$

Now  $I_m$  = Amplitude (peak) of a.c. output (load) current as shown in the Fig. 5.14

$$\boxed{\therefore I_m = \frac{I_{pp}}{2} = \frac{I_{\max} - I_{\min}}{2}} \quad \dots (9)$$

Hence the r.m.s. values of alternating output voltage and current can be obtained as,

$$V_{rms} = \frac{V_m}{\sqrt{2}} \quad \dots (10)$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \dots (11)$$

Hence we can write,

$$V_{\text{rms}} = I_{\text{rms}} R_L \quad \dots (12)$$

$$\text{i.e.} \quad V_m = I_m R_L \quad \dots (13)$$

The a.c. power delivered by the amplifier to the load can be expressed by using r.m.s values, maximum i.e. peak values and peak to peak values of output voltage and current.

### i) Using r.m.s values

$$P_{\text{ac}} = V_{\text{rms}} I_{\text{rms}} \quad \dots (14)$$

$$\text{or} \quad P_{\text{ac}} = I_{\text{rms}}^2 R_L \quad \dots (15)$$

$$\text{or} \quad P_{\text{ac}} = \frac{V_{\text{rms}}^2}{R_L} \quad \dots (16)$$

### ii) Using peak values

$$P_{\text{ac}} = V_{\text{rms}} I_{\text{rms}} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}$$

$$\therefore P_{\text{ac}} = \frac{V_m I_m}{2} \quad \dots (17)$$

$$\text{or} \quad P_{\text{ac}} = \frac{I_m^2 R_L}{2} \quad \dots (18)$$

$$\text{or} \quad P_{\text{ac}} = \frac{V_m^2}{2 R_L} \quad \dots (19)$$

**iii) Using peak to peak values**

$$P_{ac} = \frac{V_m I_m}{2} = \frac{\left(\frac{V_{pp}}{2}\right)\left(\frac{I_{pp}}{2}\right)}{2}$$

$$P_{ac} = \frac{V_{pp} I_{pp}}{8} \quad \dots (20)$$

or  $P_{ac} = \frac{I_{pp}^2 R_L}{8} \quad \dots (21)$

or  $P_{ac} = \frac{V_{pp}^2}{8 R_L} \quad \dots (22)$

But as  $V_{pp} = V_{max} - V_{min}$  and  $I_{pp} = I_{max} - I_{min}$ ; from equation (20), the a.c. power can be expressed as below, for graphical calculations.

$$P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8} \quad \dots (22)$$

**Efficiency:**

The efficiency of an amplifier represents the amount of a.c. power delivered or transferred to the load, from the d.c. source i.e. accepting the d.c. power input. The generalised expression for an efficiency of an amplifier is,

$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 \quad \dots (24)$$

Now for class A operation, we have derived the expressions for  $P_{ac}$  and  $P_{dc}$ , hence using equations (5) and (23), we can write

$$\% \eta = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{CC} I_{CQ}} \times 100 \quad \dots (25)$$

The efficiency is also called **conversion efficiency** of an amplifier.

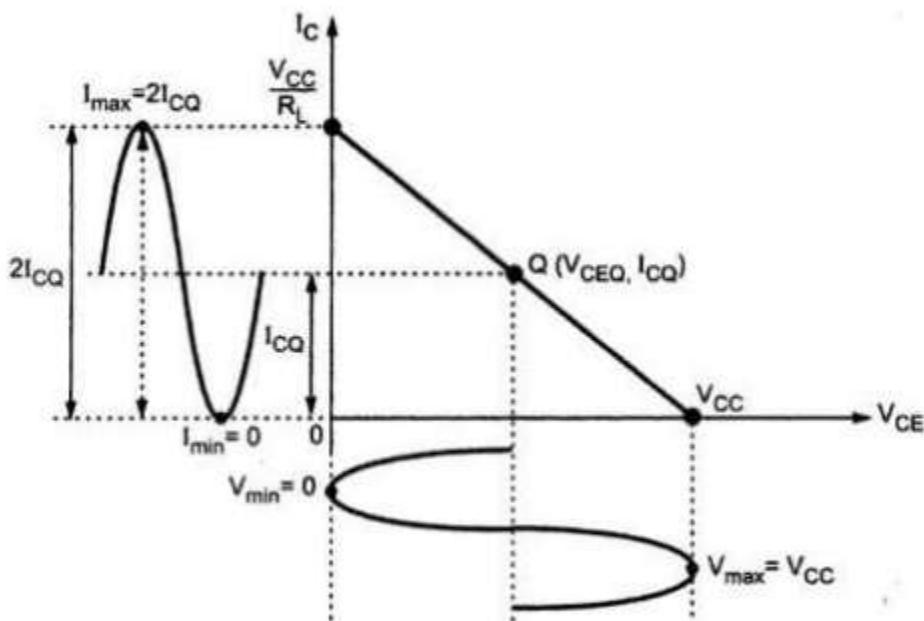
**Maximum efficiency:**

For maximum efficiency calculation, assume maximum swings of both the output voltage and the output current. The maximum swings are shown in the Fig. 5.15.

From the Fig. 5.15, we can see that the minimum voltage possible is zero and maximum voltage possible is  $V_{CC}$ , for a maximum swing. Similarly the minimum current is zero and the maximum current possible is  $2 I_{CQ}$ , for a maximum swing.

► Figure 5.15

Maximum voltage and current swings



$$\left. \begin{array}{l} V_{\max} = V_{CC} \text{ and } V_{\min} = 0 \\ I_{\max} = 2I_{CQ} \text{ and } I_{\min} = 0 \end{array} \right\} \text{for maximum swing}$$

Using equation (25) we can write,

$$\begin{aligned} \% \eta_{\max} &= \frac{(V_{CC} - 0)(2I_{CQ} - 0)}{8V_{CC}I_{CQ}} \times 100 = \frac{2V_{CC}I_{CQ}}{8V_{CC}I_{CQ}} \times 100 \\ &= 25\% \end{aligned}$$

**Key Point:** Thus the maximum efficiency possible in case of directly coupled series fed class A amplifier is just 25%.

This maximum efficiency is an ideal value. For a practical circuit, it is much less than 25%, of the order of 10 to 15%.

**Key Point:** Very low efficiency is the biggest disadvantage of class A amplifier.

### Power dissipation:

As stated earlier, power dissipation in large signal amplifier is also large. The amount of power that must be dissipated by the transistor is the difference between the d.c. power input  $P_{dc}$  and the a.c. power delivered to the load  $P_{ac}$ .

$$\begin{aligned} P_d &= \text{Power dissipation} \\ \text{i.e. } P_d &= P_{DC} - P_{ac} \end{aligned} \quad \dots (26)$$

The maximum power dissipation occurs when there is zero a.c. input signal. When a.c. input is zero, the a.c. power output is also zero. But transistor operates at quiescent condition, drawing d.c. input power from the supply equal to  $V_{CC} I_{CQ}$ . This entire power gets dissipated in the form of heat. Thus d.c. power input without a.c. input signal is the maximum power dissipation.

$$(P_d)_{\max} = V_{CC} I_{CQ} \quad \dots (27)$$

**Key Point:** Thus value of maximum power dissipation decides the maximum power dissipation rating of the transistor to be selected for the amplifier.

### Advantages and disadvantages:

The advantages of directly coupled class A amplifier can be stated as,

1. The circuit is simple to design and to implement
2. The load is connected directly in the collector circuit hence the output transformer is not necessary. This makes the circuit cheaper.
3. Less number of components required as load is directly coupled.

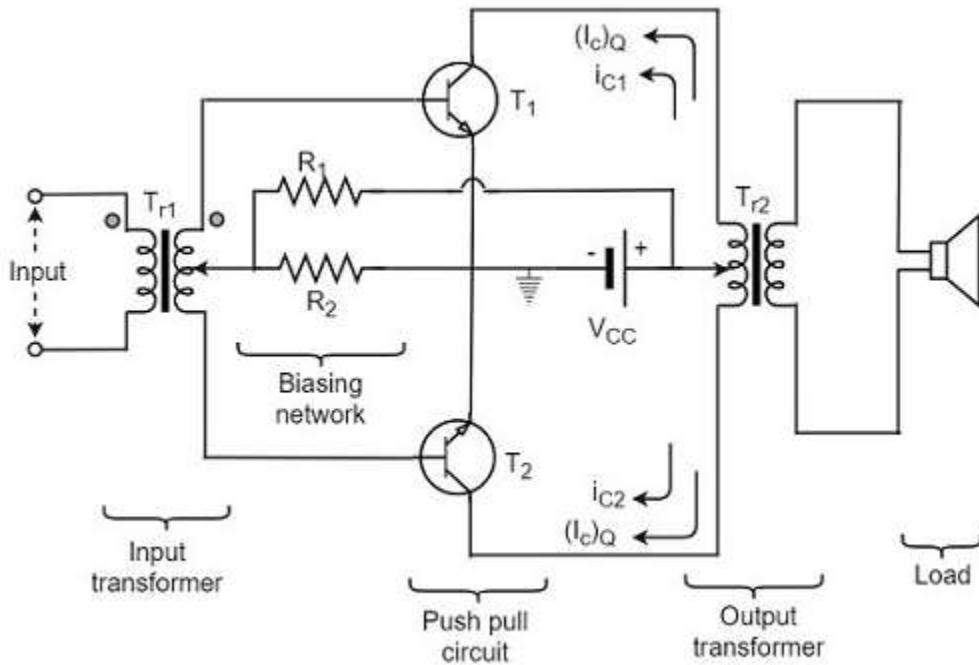
The disadvantages are :

1. The load resistance is directly connected in collector and carries the quiescent collector current. This causes considerable wastage of power.
2. Power dissipation is more. Hence power dissipation arrangements like heat sink are essential.
3. The output impedance is high hence circuit cannot be used for low impedance loads, such as loudspeakers.
4. The efficiency is very poor, due to large power dissipation.

### Push-Pull Class A Power Amplifier

Class A amplifier uses a combinational transistor pair called as **Push-Pull** configuration.

In this circuit, we use two complementary transistors in the output stage with one transistor being an NPN or N-channel type while the other transistor is a PNP or P-channel (the complement) type connected in order to operate them like **PUSH a transistor to ON** and **PULL another transistor to OFF** at the same time.



In Push-pull arrangement, the two identical transistors  $T_1$  and  $T_2$  have their emitter terminals shorted. The input signal is applied to the transistors through the transformer  $T_{r1}$  which provides opposite polarity signals to both the transistor bases. The collectors of both the transistors are connected to the primary of output transformer  $T_{r2}$ . Both the transformers are center tapped. The  $V_{CC}$  supply is provided to the collectors of both the transistors through the primary of the output transformer.

The resistors  $R_1$  and  $R_2$  provide the biasing arrangement. The load is generally a loudspeaker which is connected across the secondary of the output transformer. The turns ratio of the output transformer is chosen in such a way that the load is well matched with the output impedance of the transistor. So maximum power is delivered to the load by the amplifier.

### Circuit Operation

The output is collected from the output transformer  $T_{r2}$ . The primary of this transformer  $T_{r2}$  has practically no dc component through it. The transistors  $T_1$  and  $T_2$  have their collectors connected to the primary of transformer  $T_{r2}$  so that their currents are equal in magnitude and flow in opposite directions through the primary of transformer  $T_{r2}$ .

When the a.c. input signal is applied, the base of transistor  $T_1$  is more positive while the base of transistor  $T_2$  is less positive. Hence the collector current  $i_{c1}$  of transistor  $T_1$  increases while the collector current  $i_{c2}$  of transistor  $T_2$  decreases. These currents flow in opposite directions in two halves of the primary of output transformer. Moreover, the flux produced by these currents will also be in opposite directions.

Hence, the voltage across the load will be induced voltage whose magnitude will be proportional to the difference of collector currents i.e.

$$(i_{c1} - i_{c2})$$

Similarly, for the negative input signal, the collector current  $i_{c2}$  will be more than  $i_{c1}$ . In this case, the voltage developed across the load will again be due to the difference

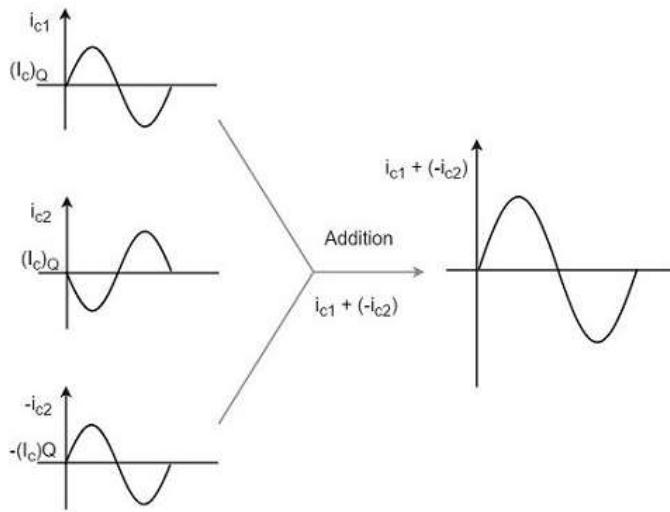
$$(i_{c1} - i_{c2})$$

As  $i_{c2} > i_{c1}$

The polarity of voltage induced across load will be reversed.

$$i_{c1} - i_{c2} = i_{c1} + (-i_{c2})$$

To have a better understanding, let us consider the below figure.



It is understood that, during any given half cycle of input signal, one transistor is being driven (or pushed) deep into conduction while the other being non-conducting (pulled out). Hence the name **Push-pull amplifier**.

## Advantages

The advantages of class A Push-pull amplifier are as follows

- High a.c. output is obtained.
- The output is free from even harmonics.
- The effect of ripple voltages are balanced out. These are present in the power supply due to inadequate filtering.

## Disadvantages

The disadvantages of class A Push-pull amplifier are as follows

- The transistors are to be identical, to produce equal amplification.
- Center-tapping is required for the transformers.
- The transformers are bulky and costly.

### Circuit Diagram of Class AB Push-pull Amplifier

This circuit is similar to the Class A Push-pull amplifier. But unlike Class A in Class AB biasing resistor values are selected such that the transistors Q1 and Q2 are biased just above the cut in voltages. This arrangement reduces the time during which the transistors will be simultaneously OFF. Thus, the cross over distortion is reduced in the Class AB amplifier.

### Push-pull Amplifier Working

The output stage of this amplifier can drive the current in both directions through the load. It contains two anti-phased transistors Q1 and Q2. The input coupling transformer T1 divides the input signal into two identical halves, every 180 degrees out of phase. One transistor gets forward biased during the positive half-cycle and passes the current. The other transistor stays reverse biased during the positive half cycle. This condition is reversed when the negative half cycle is applied to the transistors.

The collector currents I1 and I2 from Q1 and Q2 flows in the same direction through the corresponding halves of the primary of the transformer T2. This induces an amplified output of the input signal in the secondary of the T2 transformer. Thus, the current through secondary of T2 is the difference between the collector currents of the transistors.

### Class B push pull amplifier:

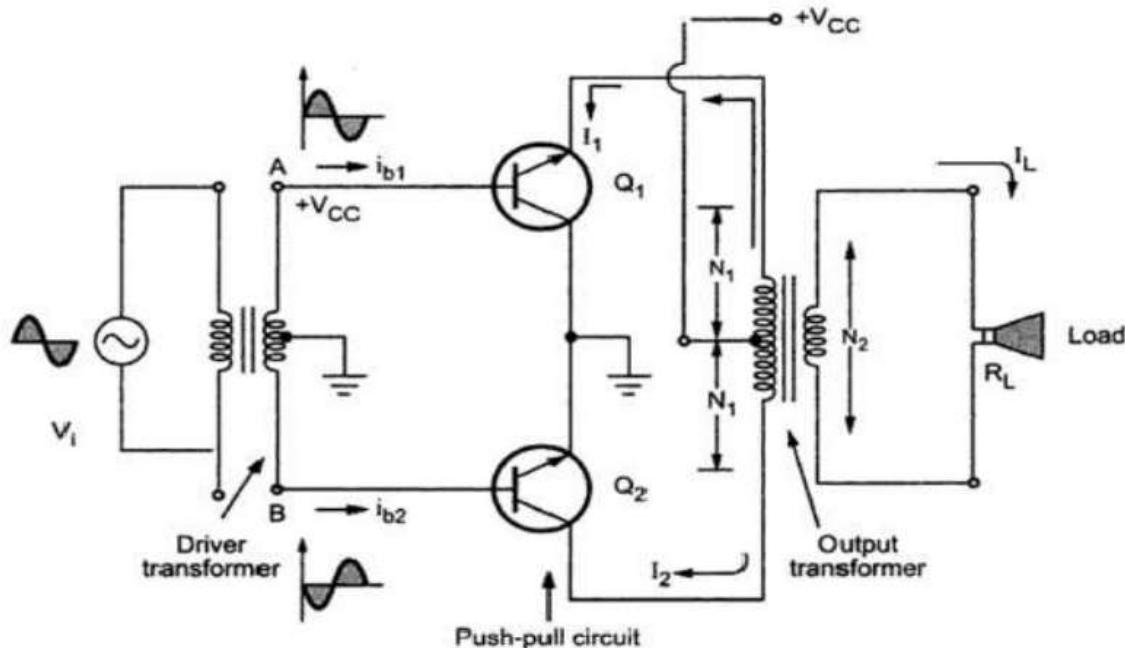
The push pull circuit requires two transformers, one as input transformer called **driver transformer** and the other to connect the load called **output transformer**. The input signal is applied to the primary of the driver transformer. Both the transformers are centre tapped transformers. The push pull class B amplifier circuit is shown in the Fig. 5.25.

In the circuit, both Q<sub>1</sub> and Q<sub>2</sub> transistors are of n-p-n type. The circuit can use both Q<sub>1</sub> and Q<sub>2</sub> of p-n-p type. In such a case, the only change is that the supply voltage must be  $-V_{CC}$ , the basic circuit remains the same. Generally the circuit using n-p-n transistors is used. Both the transistors are in common emitter configuration.

The driver transformer drives the circuit. The input signal is applied to the primary of the driver transformer. The centre tap on the secondary of the driver transformer is grounded. The centre tap on the primary of the output transformer is connected to the supply voltage + V<sub>CC</sub>.

► Figure 5.25

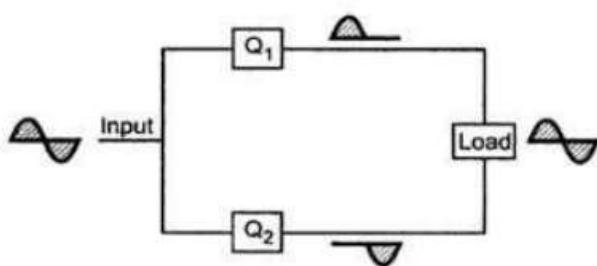
Push pull class B amplifier



With respect to the centre tap, for a positive half cycle of input signal, the point A shown on the secondary of the driver transformer will be positive. While the point B will be negative. Thus the voltages in the two halves of the secondary of the driver transformer will be equal but with opposite polarity. Hence the input signals applied to the base of the transistors  $Q_1$  and  $Q_2$  will be  $180^\circ$  out of phase.

► Figure 5.26

Basic push pull operation



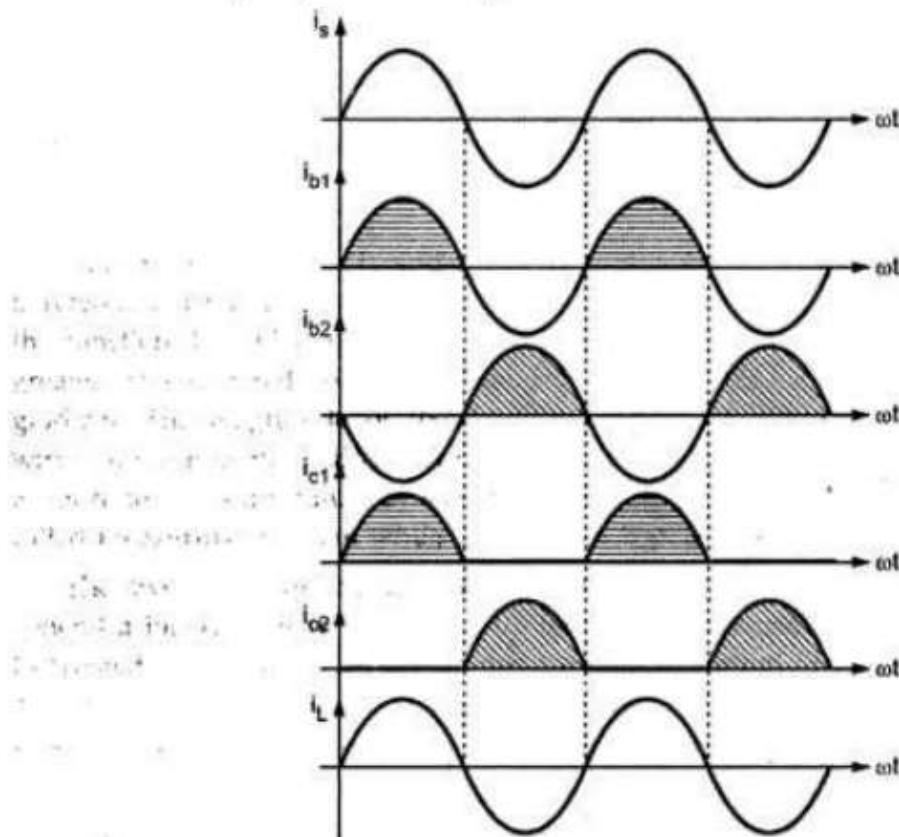
The transistor  $Q_1$  conducts for the positive half cycle of the input producing positive half cycle across the load. While the transistor  $Q_2$  conducts for the negative half cycle of the input producing negative half cycle across the load. Thus across the load, we get a full cycle for a full input cycle. The basic push pull operation is shown in the Fig. 5.26.

When point A is positive, the transistor  $Q_1$  gets driven into an active region while the transistor  $Q_2$  is in cut off region. While when point A is negative, the point B is positive, hence the transistor  $Q_2$  gets driven into an active region while the transistor  $Q_1$  is in cut off region.

The waveforms of the input current, base currents, collector currents and the load current are shown in the Fig. 5.27.

► **Figure 5.27**

Waveforms for push pull class B amplifier



#### D.C Operation:

The d.c. biasing point i.e. Q point is adjusted on the X-axis such that  $V_{CEQ} = V_{CC}$  and  $I_{CEQ}$  is zero. Hence the co-ordinates of the Q point are  $(V_{CC}, 0)$ . There is no d.c. base bias voltage.

#### D.C power input:

Each transistor output is in the form of half rectified waveform. Hence if  $I_m$  is the peak value of the output current of each transistor, the d.c. or average value is  $\frac{I_m}{\pi}$ , due to half rectified waveform. The two currents, drawn by the two transistors, form the d.c. supply are in the same direction. Hence the total d.c. or average current drawn from the supply is the algebraic sum of the individual average current drawn by each transistor.

$$\therefore I_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2 I_m}{\pi} \quad \dots (1)$$

The total d.c. power input is given by,

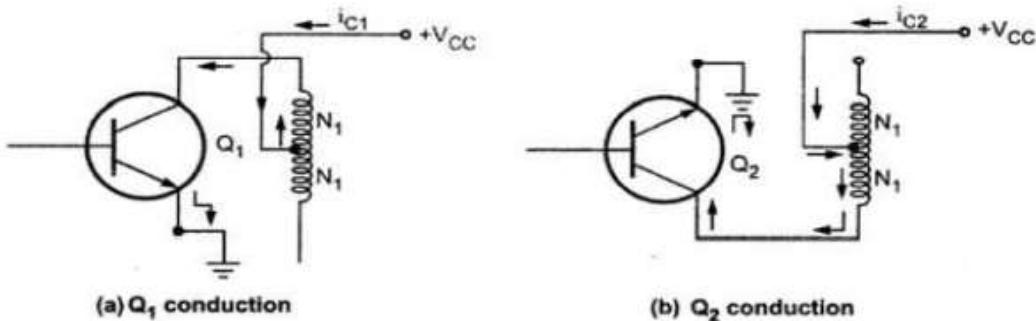
$$\begin{aligned} P_{DC} &= V_{CC} \times I_{dc} \\ \therefore P_{DC} &= \frac{2}{\pi} V_{CC} I_m \end{aligned} \quad \dots (2)$$

### A.C operation:

When the a.c. signal is applied to the driver transformer, for positive half cycle  $Q_1$  conducts. The path of the current drawn by the  $Q_1$  is shown in the Fig. 5.28.

For the negative half cycle  $Q_2$  conducts. The path of the current drawn by the  $Q_2$  is shown in the Fig. 5.28 (b).

► **Figure 5.28**



It can be seen that when  $Q_1$  conducts, lower half of the primary of the output transformer does not carry any current. Hence only  $N_1$  number of turns carry the current. While when  $Q_2$  conducts, upper half of the primary does not carry any current. Hence again only  $N_1$  number of turns carry the current. Hence the reflected load on the primary can be written as,

$$\therefore R'_L = \frac{R_L}{n^2} \quad \dots (3)$$

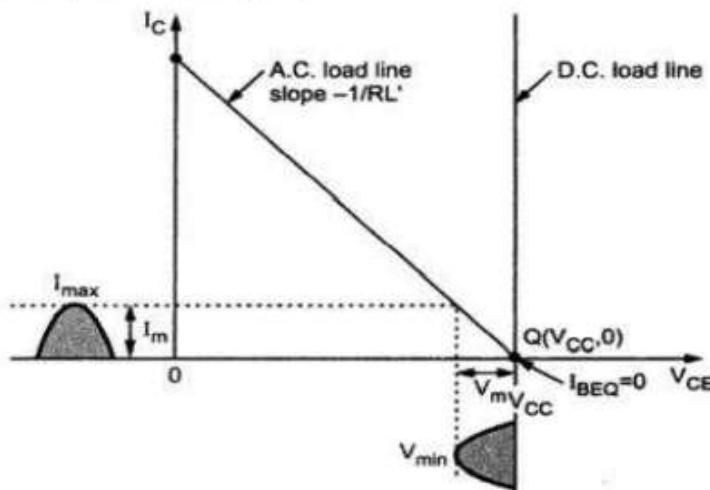
where  $n = \frac{N_2}{N_1}$

It is important to note that the step down turns ratio is  $2N_1 : N_2$  but while calculating the reflected load, the ratio  $n$  becomes  $N_2/N_1$ . So each transistor shares equal load which is the reflected load  $R'_L$  given by the equation (3).

The slope of the a.c. load line is  $-1/R'_L$  while the d.c. load line is the vertical line passing through the operating point Q on the x-axis. The load lines are shown in the Fig. 5.29.

► **Figure 5.29**

Load lines for push pull class B amplifier



The slope of the a.c. load line (magnitude of slope) can be represented in terms of  $V_m$  and  $I_m$  as,

$$\frac{1}{R'_L} = \frac{I_m}{V_m}$$

$$\therefore R'_L = \frac{V_m}{I_m} \quad \dots (4)$$

where  $I_m$  = Peak value of the collector current

### A.C power output:

As  $I_m$  and  $V_m$  are the peak values of the output current and the output voltage respectively, then

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$\text{and } I_{rms} = \frac{I_m}{\sqrt{2}}$$

Hence the a.c. power output is expressed as,

$$P_{ac} = V_{rms} I_{rms} = I_{rms}^2 R_L = \frac{V_{rms}^2}{R_L} \quad \dots (5)$$

While using peak values it can be expressed as,

$$\therefore P_{ac} = \frac{V_m I_m}{2} = \frac{I_m^2 R_L}{2} = \frac{V_m^2}{2 R_L} \quad \dots (6)$$

### Efficiency:

The efficiency of the class B amplifier can be calculated using the basic equation.

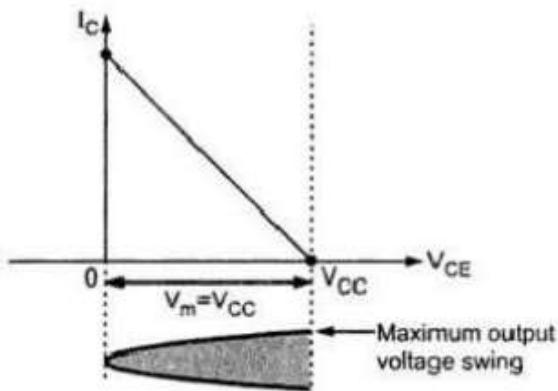
$$\% \eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{\left( \frac{V_m I_m}{2} \right)}{\frac{2}{\pi} V_{CC} I_m} \times 100$$

$$\therefore \% \eta = \frac{\pi}{4} \frac{V_m}{V_{CC}} \times 100 \quad \dots (7)$$

### Maximum efficiency:

From the equation (7), it is clear that as the peak value of the collector voltage  $V_m$  increases, the efficiency increases. The maximum value of  $V_m$  possible is equal to  $V_{CC}$  as shown in the Fig. 5.30.

► **Figure 5.30**



$$V_m = V_{CC} \text{ for maximum } \eta$$

$$\therefore \% \eta_{\max} = \frac{\pi}{4} \times \frac{V_{CC}}{V_{CC}} \times 100 \\ = 78.5 \%$$

**Key Point:** Thus the maximum possible theoretical efficiency in case of push pull class B amplifier is 78.5% which is much higher than the transformer coupled class A amplifier.

### Power dissipation:

The power dissipation by both the transistors is the difference between a.c. power output and d.c. power input.

$$\therefore P_d = P_{DC} - P_{ac} = \frac{2}{\pi} V_{CC} I_m - \frac{V_m I_m}{2}$$

$$\therefore P_d = \frac{2}{\pi} V_{CC} \frac{V_m}{R'_L} - \frac{V_m^2}{2R'_L} \quad \dots (8)$$

Let us find out the condition for maximum power dissipation. In case of class A amplifier, it is maximum when no input signal is there. But in class B operation, when the input signal is zero,  $V_m = 0$  hence the power dissipation is zero and not the maximum.

**Maximum power dissipation :** The condition for maximum power dissipation can be obtained by differentiating the equation (8) with respect to  $V_m$  and equating it to zero.

$$\therefore \frac{d P_d}{d V_m} = \frac{2}{\pi} \frac{V_{CC}}{R'_L} - \frac{2V_m}{2R'_L} = 0$$

$$\therefore \frac{2}{\pi} \frac{V_{CC}}{R'_L} = \frac{V_m}{R'_L}$$

$$V_m = \frac{2}{\pi} V_{CC}$$

... For maximum power dissipation ... (9)

This is the condition for maximum power dissipation. Hence the maximum power dissipation is,

$$\begin{aligned} (P_d)_{max} &= \frac{2}{\pi} V_{CC} \times \frac{2}{\pi} \frac{V_{CC}}{R'_L} - \frac{4}{\pi^2} \frac{V_{CC}^2}{2R'_L} \\ &= \frac{4}{\pi^2} \frac{V_{CC}^2}{R'_L} - \frac{2}{\pi^2} \frac{V_{CC}^2}{R'_L} \end{aligned}$$

$$(P_d)_{max} = \frac{2}{\pi^2} \frac{V_{CC}^2}{R'_L}$$

... (10)

### Harmonic Distortion:

The harmonic distortion means the presence of the frequency components in the output wave form, which are not present in the input signal. The component with frequency same as the input signal is called fundamental frequency component. The additional frequency components present in the output signal are having frequency components which are integer multiples of fundamental frequency component. These components are called harmonic components or harmonics. For example if the fundamental frequency is  $f$  Hz, then the output signal contains fundamental frequency component at  $f$  Hz and additional frequency components at  $2f$  Hz,  $3f$  Hz,  $4f$  Hz and so on. The  $2f$  component is called **second harmonic**, the  $3f$  component is called **third harmonic** and so on. The fundamental frequency component is not considered as a harmonic. Out of all the harmonic components, the second harmonic has the largest amplitude.

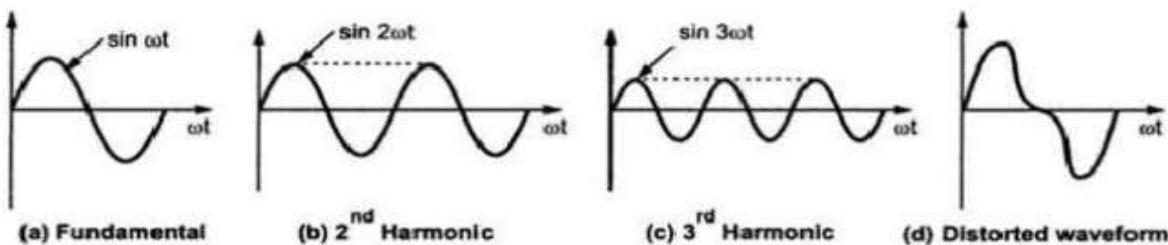
**Key Point:** As the order of the harmonic increases, its amplitude decreases.

As the second harmonic amplitude is largest, the second harmonic distortion is more important in the analysis of A.F. power amplifiers. The Fig. 5.21 shows the various harmonic components.

It can be seen from the Fig. 5.21 that the distorted waveform can be obtained by adding the fundamental and the harmonic components. The percentage harmonic distortion due to each order ( $2^{\text{nd}}$ ,  $3^{\text{rd}}$  and so on) can be calculated by comparing the amplitude of each order of harmonic with the amplitude of the fundamental frequency component.

► Figure 5.21

Distortion due to harmonic components



If the fundamental frequency component has an amplitude of  $B_1$  and the  $n^{\text{th}}$  harmonic component has an amplitude of  $B_n$  then the percentage harmonic distortion due to  $n^{\text{th}}$  harmonic component is expressed as,

$$\% n^{\text{th}} \text{ harmonic distortion} = \% D_n = \frac{|B_n|}{|B_1|} \times 100 \quad \dots (1)$$

So

$$\% D_2 = \frac{|B_2|}{|B_1|}, \% D_3 = \frac{|B_3|}{|B_1|} \text{ and so on.}$$

### Total Harmonic distortion:

When the output signal gets distorted due to various harmonic distortion components, the total harmonic distortion, which is the effective distortion due to all the individual components is given by

$$\%D = \sqrt{D_2^2 + D_3^2 + D_4^2 + \dots} \times 100 \quad \dots (2)$$

where  $D$  = Total Harmonic Distortion

As stated earlier, the most important component in the distortion is the second harmonic distortion. Let us discuss the graphical method of calculating second harmonic distortion.

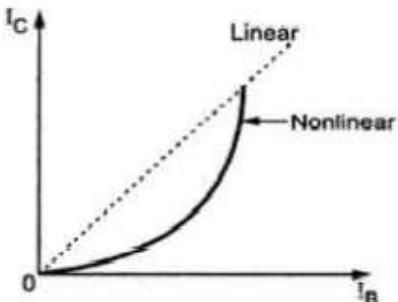
### Second harmonic distortion (Three point method)

To investigate the second harmonic distortion, assume that the dynamic transfer characteristics of the transistor is parabolic (nonlinear) in nature rather than a straight line (linear) as shown in the Fig. 5.22.

As discussed earlier such type of nonlinearity introduces harmonic distortion, in which second harmonic distortion is the most dominant.

► **Figure 5.22**

Nonlinear dynamic characteristics



Let an a.c. input signal, causes the base current swing which is cosine in nature

$$\therefore i_b = I_{Bm} \cos \omega t \quad \dots (3)$$

Due to this, collector current swings around its quiescent value but the relation between  $i_b$  and  $i_c$  is nonlinear as shown in the Fig. 5.22.

Mathematically this can be expressed as,

$$\begin{aligned} i_c &= G_1 i_b + G_2 i_b^2 \\ &= G_1 I_{Bm} \cos \omega t + G_2 I_{Bm}^2 \cos^2 \omega t \end{aligned} \quad \dots (4)$$

$$\text{But } \cos^2 \omega t = \frac{1 + \cos 2\omega t}{2}$$

Substituting in equation (4),

$$i_c = G_1 I_{Bm} \cos \omega t + G_2 I_{Bm}^2 \left( \frac{1 + \cos 2\omega t}{2} \right)$$

$$\therefore i_c = G_1 I_{Bm} \cos \omega t + \frac{1}{2} G_2 I_{Bm}^2 + \frac{G_2}{2} I_{Bm}^2 \cos 2\omega t$$

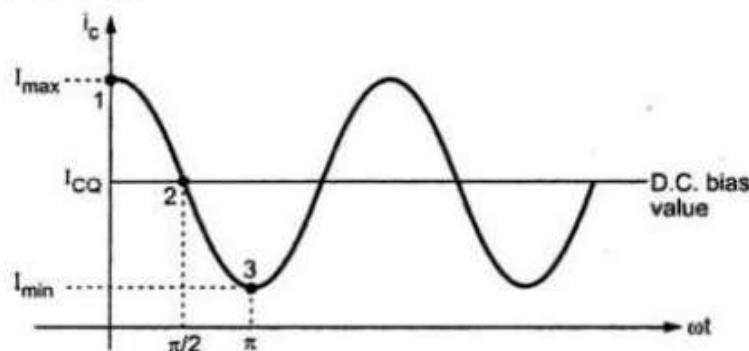
$$\therefore i_c = B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t \quad \dots (5)$$

The last term represents the second harmonic component. Thus the equation shows that, there is second harmonic component present.

Hence the total collector current waveform can be shown as in the Fig. 5.23, which is swinging about its quiescent value  $I_{CQ}$ .

► Figure 5.23

Output current waveform



Hence the total collector current can be expressed in terms of its d.c. bias value, d.c. signal component, fundamental frequency and second harmonic component as,

$$i_c = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t \quad \dots (6)$$

where  $(I_{CQ} + B_0)$  = The d.c. component, independent of time

where  $(I_{CQ} + B_0)$  = The d.c. component, independent of time

$B_1$  = Amplitude of the fundamental frequency

$B_2$  = Amplitude of the second harmonic component

It can be seen that due to the presence of harmonics, the d.c. current increases. Practically the presence of harmonics can be detected by connecting milliammeter in the collector circuit. The readings can be observed without an a.c. input signal and with a.c. input signal. If the two readings are almost same there are no harmonics present. But if milliammeter shows an increase in the current, when an a.c. input is applied, then the harmonics can be concluded to be present in the output signal.

Let us find out the value of the total collector current at the various instants 1, 2 and 3, shown in the Fig. 5.23.

At point 1,  $\omega t = 0$ , substituting in (6) we get,

$$\therefore i_c = I_{CQ} + B_0 + B_1 + B_2 \quad \dots (7)$$

At point 2,  $\omega t = \frac{\pi}{2}$ ,

$$\therefore i_c = I_{CQ} + B_0 - B_2 \quad \dots (8)$$

At point 3,  $\omega t = \pi$ ,

$$\therefore i_c = I_{CQ} + B_0 - B_1 + B_2 \quad \dots (9)$$

But at  $\omega t = 0$ ,  $i_c = I_{\max}$

at  $\omega t = \frac{\pi}{2}$ ,  $i_c = I_{CQ}$

at  $\omega t = \pi$ ,  $i_c = I_{\min}$

Hence the equations get modified as,

$$I_{\max} = I_{CQ} + B_0 + B_1 + B_2 \quad \dots (10)$$

$$I_{CQ} = I_{CQ} + B_0 - B_2 \quad \dots (11)$$

$$I_{\min} = I_{CQ} + B_0 - B_1 + B_2 \quad \dots (12)$$

From equation (11),

$$\boxed{B_0 = B_2} \quad \dots (13)$$

Now  $I_{\max} - I_{\min} = 2B_1$

$$\boxed{\therefore B_1 = \frac{I_{\max} - I_{\min}}{2}} \quad \dots (14)$$

$$\begin{aligned} I_{\max} + I_{\min} &= 2I_{CQ} + 2B_0 + 2B_2 \\ &= 2I_{CQ} + 2B_2 + 2B_2 \\ &= 2I_{CQ} + 4B_2 \end{aligned}$$

$$\boxed{\therefore B_2 = \frac{I_{\max} + I_{\min} - 2I_{CQ}}{4}} \quad \dots (15)$$

As the amplitudes of the fundamental and second harmonic are known, the second harmonic distortion can be calculated as,

$$\% D_2 = \frac{|B_2|}{|B_1|} \times 100 \quad \dots (16)$$

As the method uses three points on the collector current waveform to obtain the amplitudes of the harmonics, the method is called '**Three Point Method**' of determining the second harmonic distortion.

**Power output due to distortion:**

When the distortion is negligible, the power delivered to the load is given by,

$$P_{ac} = \frac{I_m^2 R_L}{2} \quad \dots \text{refer equation (18) in section 5.7}$$

But  $I_m$  = peak value of the output current

$$= \frac{I_{pp}}{2} = \frac{I_{\max} - I_{\min}}{2} \quad \dots \text{refer equation (9) in section 5.7}$$

$$\text{But } B_1 = \frac{I_{\max} - I_{\min}}{2}$$

$\therefore I_m = B_1$  = fundamental frequency component

$$\therefore P_{ac} = \frac{1}{2} B_1^2 R_L \quad \dots (17)$$

With distortion, the power delivered to the load increases proportional to the amplitude of the harmonic component.

$\therefore (P_{ac})_D$  = A.C. power output with harmonic distortion

$$= \frac{1}{2} B_1^2 R_L + \frac{1}{2} B_2^2 R_L + \frac{1}{2} B_3^2 R_L + \dots$$

$$\therefore (P_{ac})_D = \frac{1}{2} B_1^2 R_L \left( 1 + \frac{B_2^2}{B_1^2} + \frac{B_3^2}{B_1^2} + \dots \right)$$

$$\boxed{\therefore (P_{ac})_D = \frac{1}{2} B_1^2 R_L (1 + D_2^2 + D_3^2 + \dots)}$$

$$\boxed{\therefore (P_{ac})_D = P_{ac} [1 + D^2] \quad \dots D^2 = D_2^2 + D_3^2 + \dots} \quad \dots (18)$$

This is the power delivered to the load due to the harmonic distortion.

### Complementary symmetry class B amplifier:

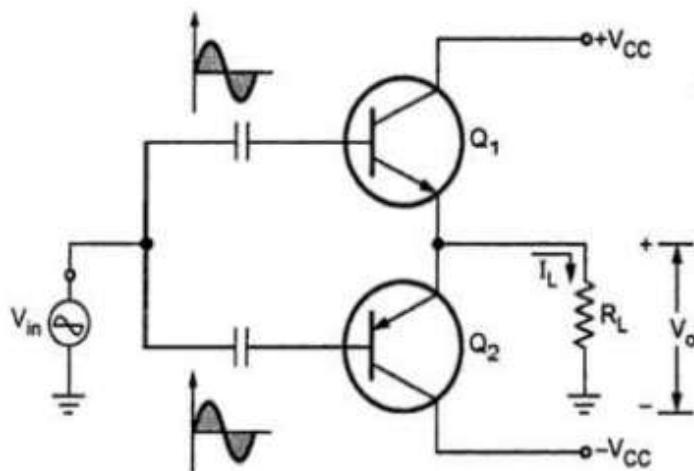
As stated earlier, instead of using same type of transistors (n-p-n or p-n-p), one n-p-n and other p-n-p is used, the amplifier circuit is called as complementary symmetry class B amplifier. This circuit is transformer less circuit. But with common emitter configuration, it becomes difficult to match the output impedance for maximum power transfer without an output transformers. Hence the matched pair of complementary transistors are used in common collector (emitter follower) configuration, in this circuit.

**Key Point:** This is because common collector configuration has lowest output impedance and hence the impedance matching is possible.

In addition, voltage feedback can be used to reduce the output impedance for matching.

► Figure 5.32

Complementary symmetry class B amplifier



The basic circuit of complementary symmetry class-B amplifier is shown in the Fig. 5.32.

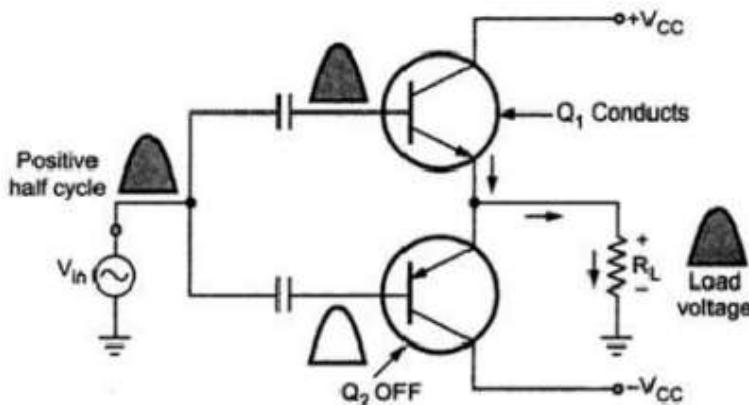
The circuit is driven from a dual supply of  $\pm V_{CC}$ . The transistor  $Q_1$  is n-p-n while  $Q_2$  is of p-n-p type.

In the positive half cycle of the input signal, the transistor  $Q_1$  gets driven into active region and starts conducting. The same signal gets applied to the base of the  $Q_2$

but as it is of complementary type, remains in off condition, during positive half cycle. This results into positive half cycle across the load  $R_L$ . This is shown in the Fig. 5.33.

► Figure 5.33

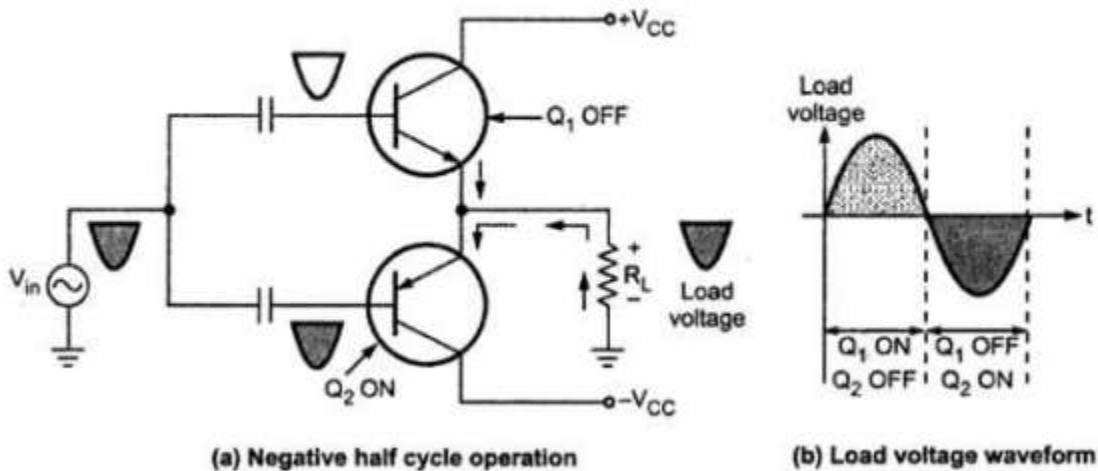
Positive half cycle operation



During the negative half cycle of the signal, the transistor  $Q_2$  being p-n-p gets biased into conduction. While the transistor  $Q_1$  gets driven into cut off region. Hence only  $Q_2$  conducts during negative half cycle of the input, producing negative half cycle across the load  $R_L$ , as shown in the Fig. 5.34 (a).

Thus for a complete cycle of input, a complete cycle of output signal is developed across the load as shown in the Fig. 5.34 (b)

► Figure 5.34



### **Comparison between push pull and complementary symmetry circuits:**

	<b>Push Pull Class B</b>	<b>Complementary Symmetry Class B</b>
1.	Both the transistors are similar either pnp or npn.	Transistors are complementary type i.e. one npn other pnp.
2.	The transformer is used to connect the load as well as input.	The circuit is transformerless.
3.	The impedance matching is possible due to the output transformer.	The impedance matching is possible due to common collector circuit.
4.	Frequency response is poor.	Frequency response is improved.
5.	Due to transformers, the circuit is bulky, costly and heavier.	As transformerless, the circuit is not bulky and costly.
6.	Dual power supply is not required.	Dual power supply is required.
7.	Efficiency is higher than class A.	The efficiency is higher than the push pull.

## Amplifier Efficiency

The power efficiency of an amplifier, defined as the ratio of power output to power input, improves (gets higher) going from class A to class D

a class A amplifier, with dc bias at one-half the supply voltage level, uses a good amount of power to maintain bias, even with no input signal applied. This results in very poor efficiency,

especially with small input signals, when very little ac power is delivered to the load. In fact, the maximum efficiency of a class A circuit, occurring for the largest output voltage and current swing, is only 25% with a direct or seriesfed load connection and 50% with a transformer connection to the load.

Class B operation, with no dc bias power for no input signal, can be shown to provide a maximum efficiency that reaches 78.5%.

Since class AB falls between class A and class B in bias, it also falls between their efficiency ratings—between 25% (or 50%) and 78.5%.

## **Linearity:**

linear amplifier is an electronic circuit whose output is proportional to its input, but capable of delivering more power into a load.

The term usually refers to a type of radio-frequency (RF) power amplifier, some of which have output power measured in kilowatts, and are used in amateur radio.

Other types of linear amplifier are used in audio and laboratory equipment. Linearity refers to the ability of the amplifier to produce signals that are accurate copies of the input.

A linear amplifier responds to different frequency components independently, and tends not to generate harmonic distortion or intermodulation distortion.