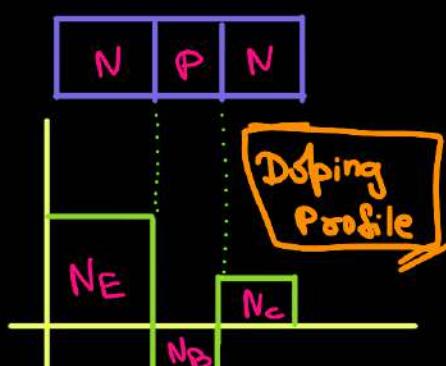
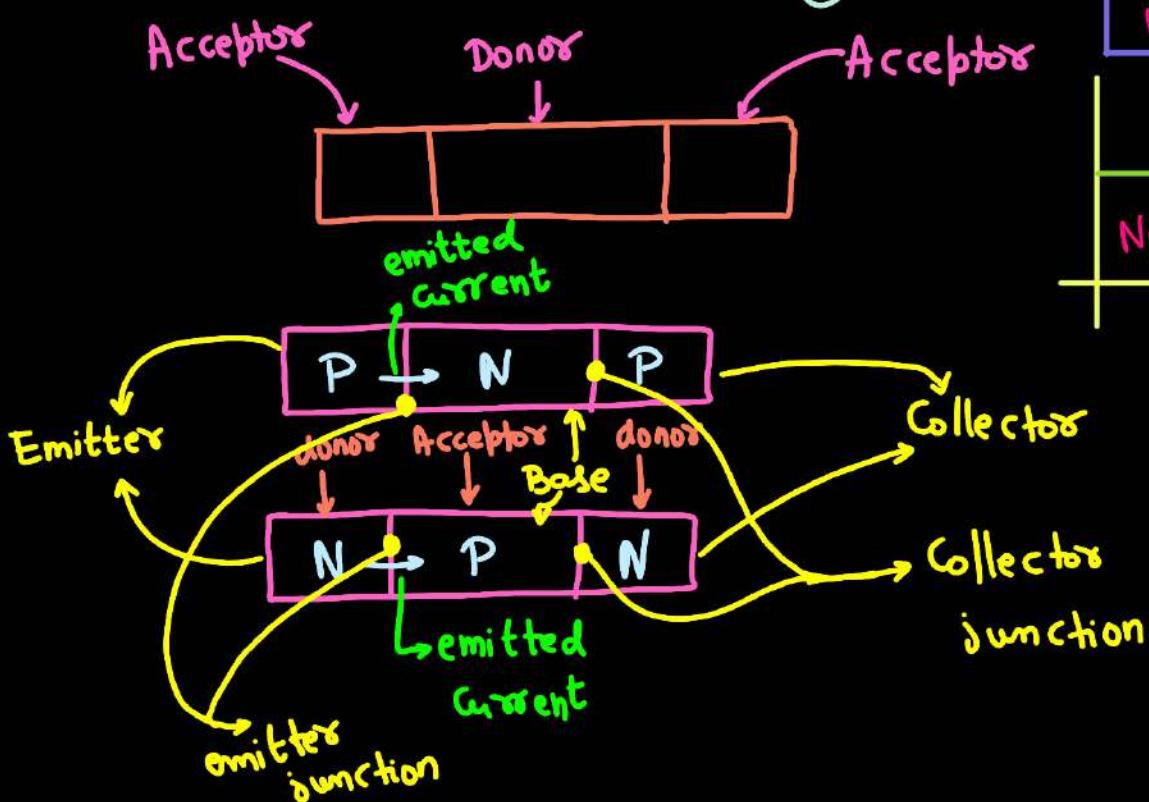


$$\text{Gain} = \frac{\text{O/P}}{\text{I/I P}}$$

### ★ Transistor

- Single crystal made of Si or Ge
- Crystal is continuous, such that 2 junctions are formed
- Can be either PNP or NPN



\* There are three regions in transistor:-

- ① Emitter: Provides large numbers of charge carriers. Heavily doped and moderately sized
- ② Base: Very thin & lightly doped
- ③ Collector: Large in size & moderately doped

# Ckt symbol of transistor:-



N-P-N  
transistor

P-N-P transistor  
 $\mu_n > \mu_p$   
 $\therefore$  NPN is preferred over PNP

Note:

Arrow always  
in dirn of  
forward  
Bias,  
i.e. from  
P to N

# Transistor Configurations:-

① Common Base (CB)

② Common Emitter (CE)

③ Common Collector (CC)

4 H Parameters:

Input Impedance

Reverse Voltage Ratio

&

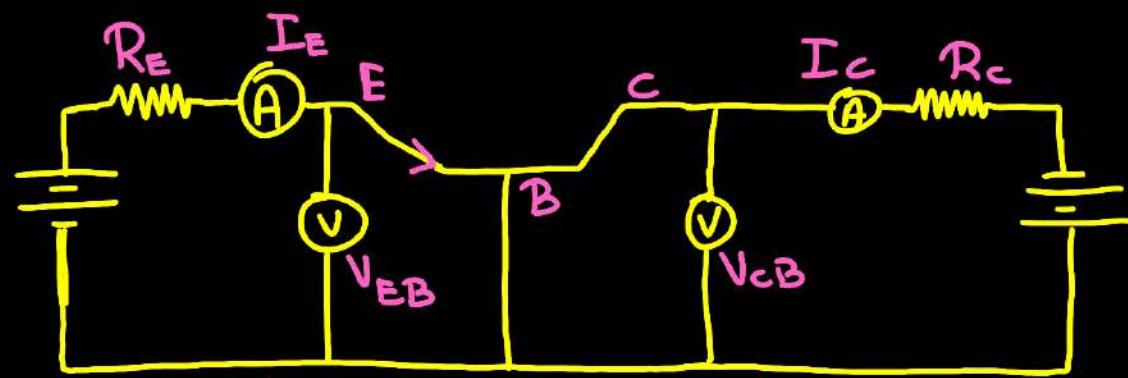
Output Admittance

Forward Current Gain

} I/P

} O/P

## # Common Base (CB) Configuration:-



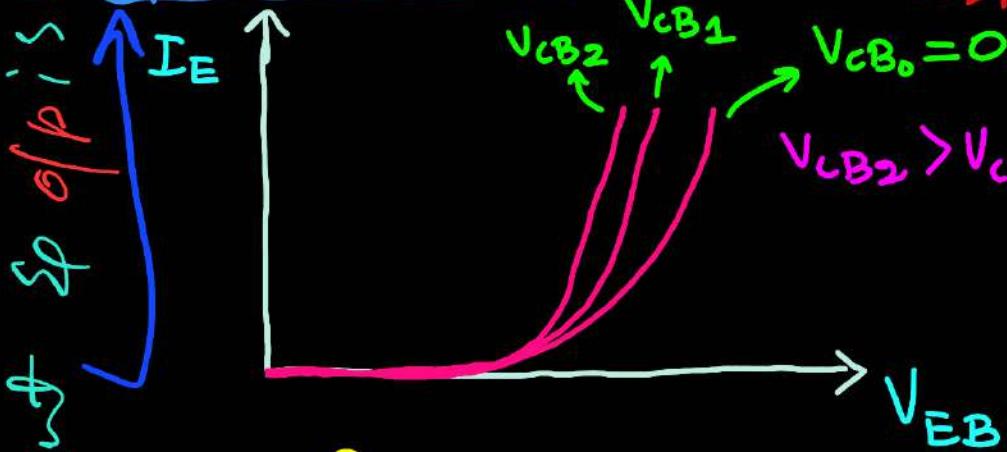
Input Circuit  
( $V_{EB}$ ,  $I_E$ )

Output Circuit  
( $V_{CB}$ ,  $I_C$ )

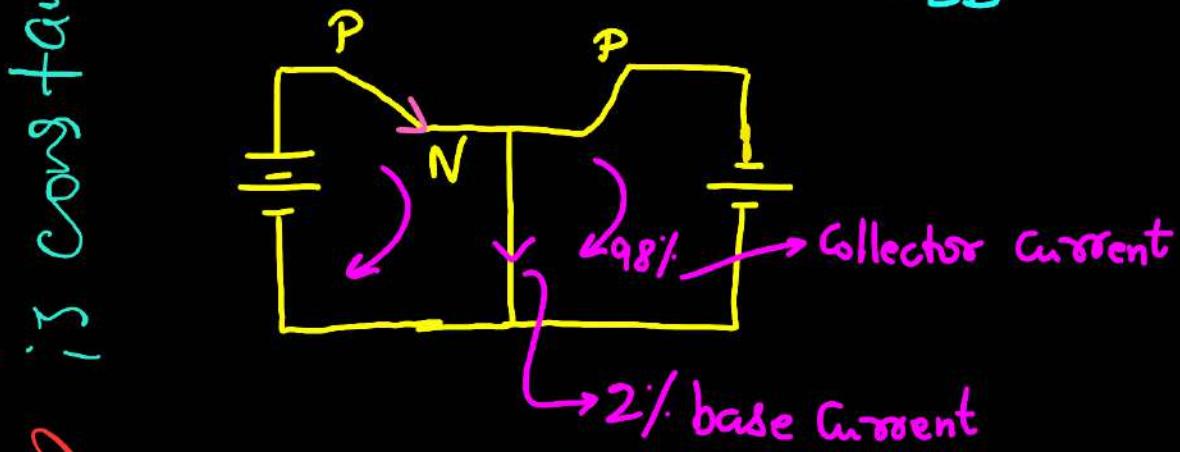
I/P characteristics

O/P characteristics

\* I/P characteristics:-



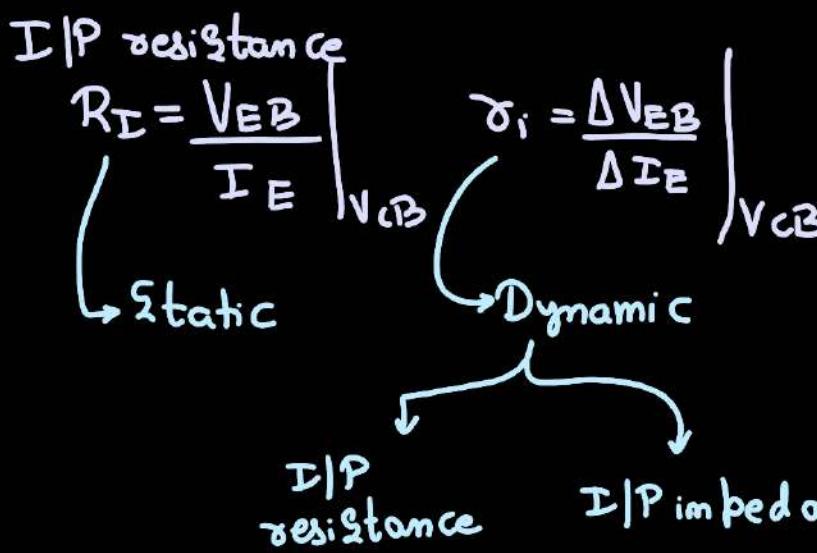
input characteristics  
is graph of p-i-p  
of n-p-n



Note

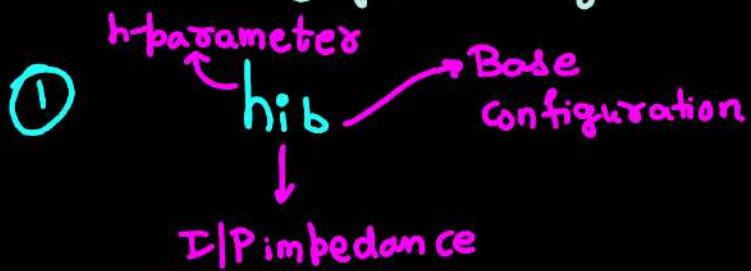
Emitter  $\delta^n \rightarrow$  F.B

Collector  $\delta^n$  is reverse biased



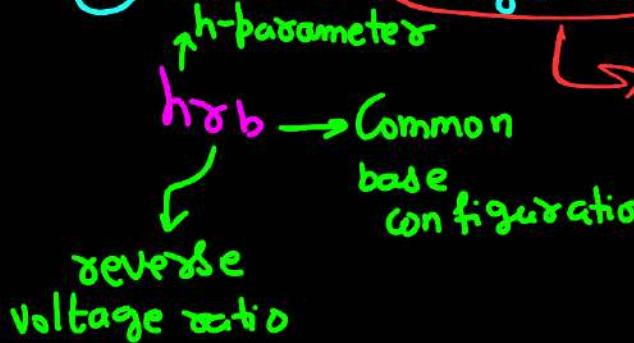
### # h-parameters:-

↳ A way of measuring → alternative for ohm's law



$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E} \quad \left|_{V_{CB}} \right.$$

② Reverse voltage ratio (h-parameter)



$$\frac{O/P}{I/P}$$

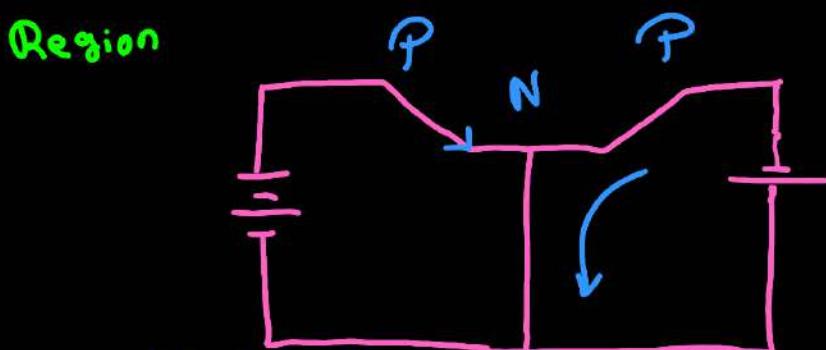
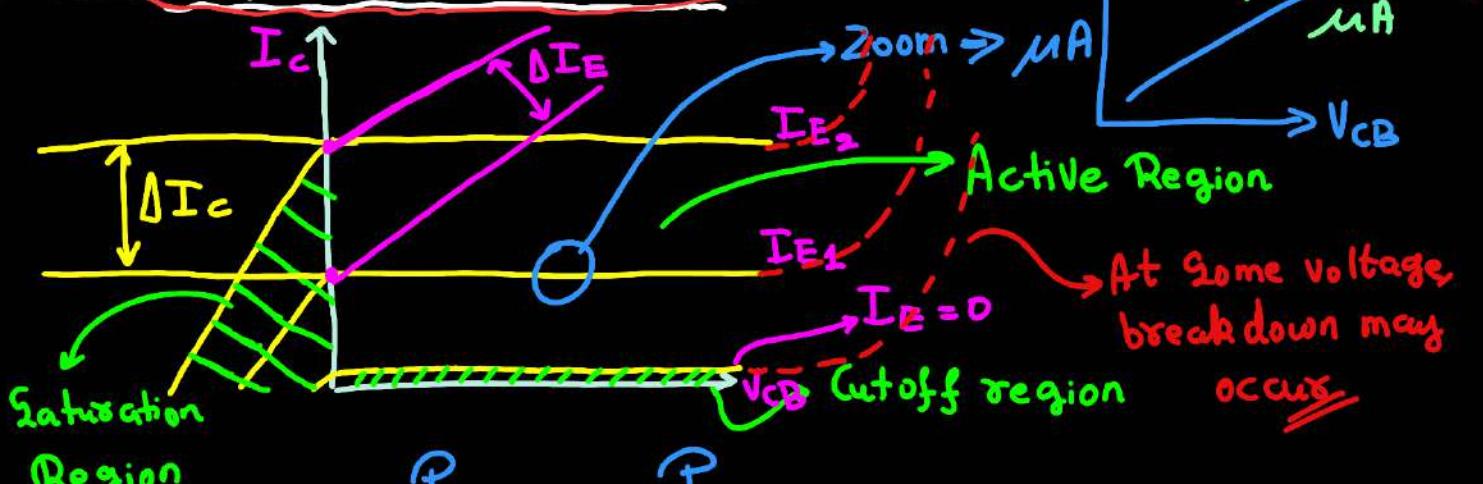
But here  
∴ reverse ratio

$$\frac{I/P}{O/P}$$

$$h_{\sigma b} = \frac{\Delta V_{EB}}{\Delta V_{CB}} \quad \left|_{I_E} \right.$$



## # Output characteristics:-



① O/P impedance

$$R_o = \left. \frac{V_{CB}}{I_C} \right|_{I_E}$$

①  $h_{ob} = \left. \frac{\Delta I_C}{\Delta V_{CB}} \right|_{I_E}$

O/P admittance Common base configuration

In off char O/P is constant if  $I_P$  keeps on varying.

②  $h_{fb} = \left. \frac{\Delta I_C}{\Delta I_E} \right|_{V_{CB}} = \alpha \rightarrow AC$

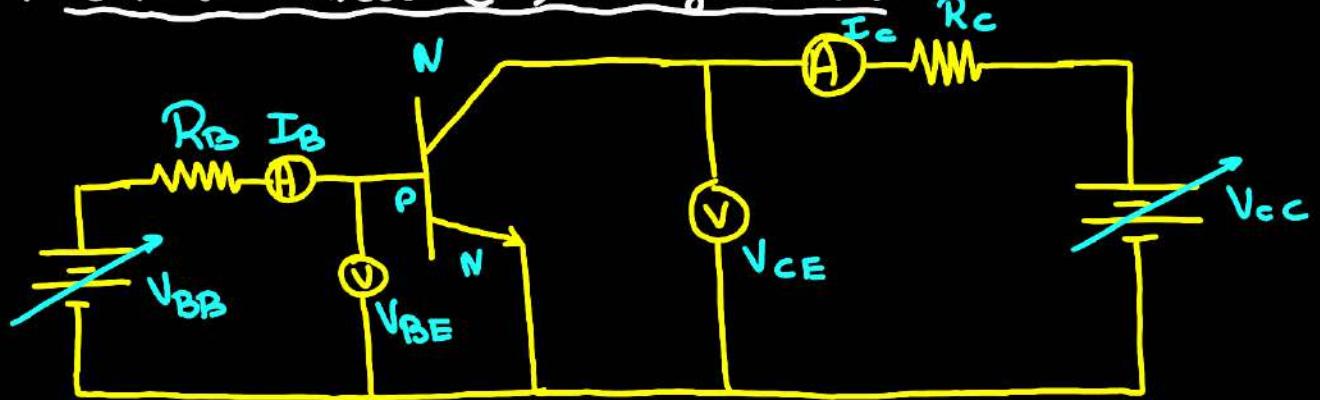
forward current gain Base config

Output current  
Input current

$$\alpha_{DC} = \frac{I_C}{I_D}$$

Output  
Input

## # Common Emitter (CE) Configuration :-

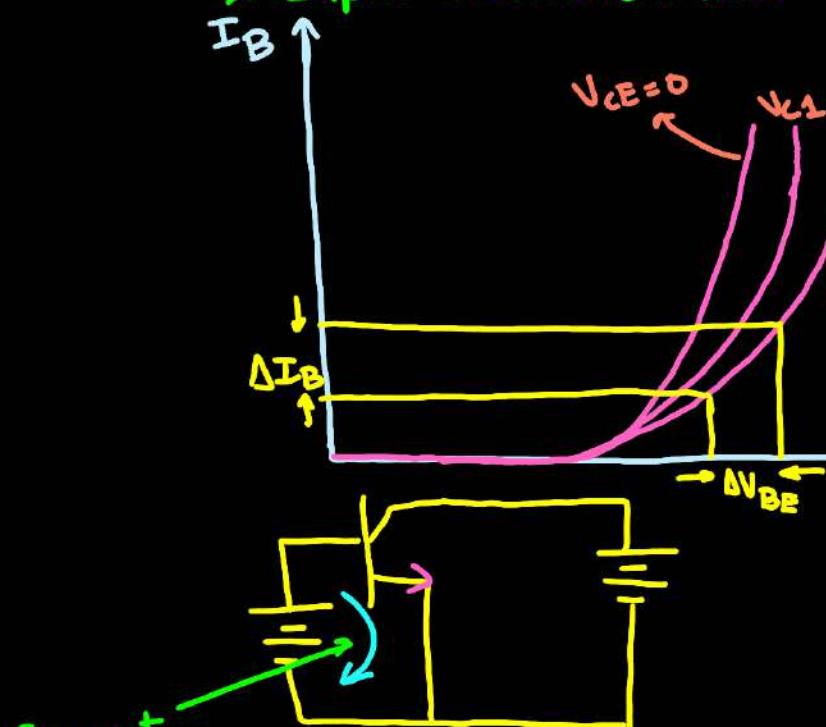


I/P ckt  
( $V_{BE}$ ,  $I_B$ )

O/P ckt  
( $V_{CE}$ ,  $I_C$ )

Emitter jn is F.B  
Collector jn is R.B

★ Input Characteristics



Current flow direction  
h-parameter

$$\textcircled{1} \quad h_{ie} = \left. \frac{\Delta V_{BE}}{\Delta I_B} \right|_{V_{CE}}$$

I/P impedance      (E Config)

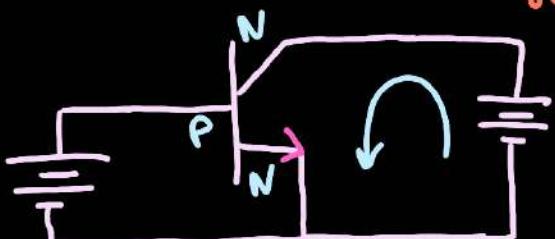
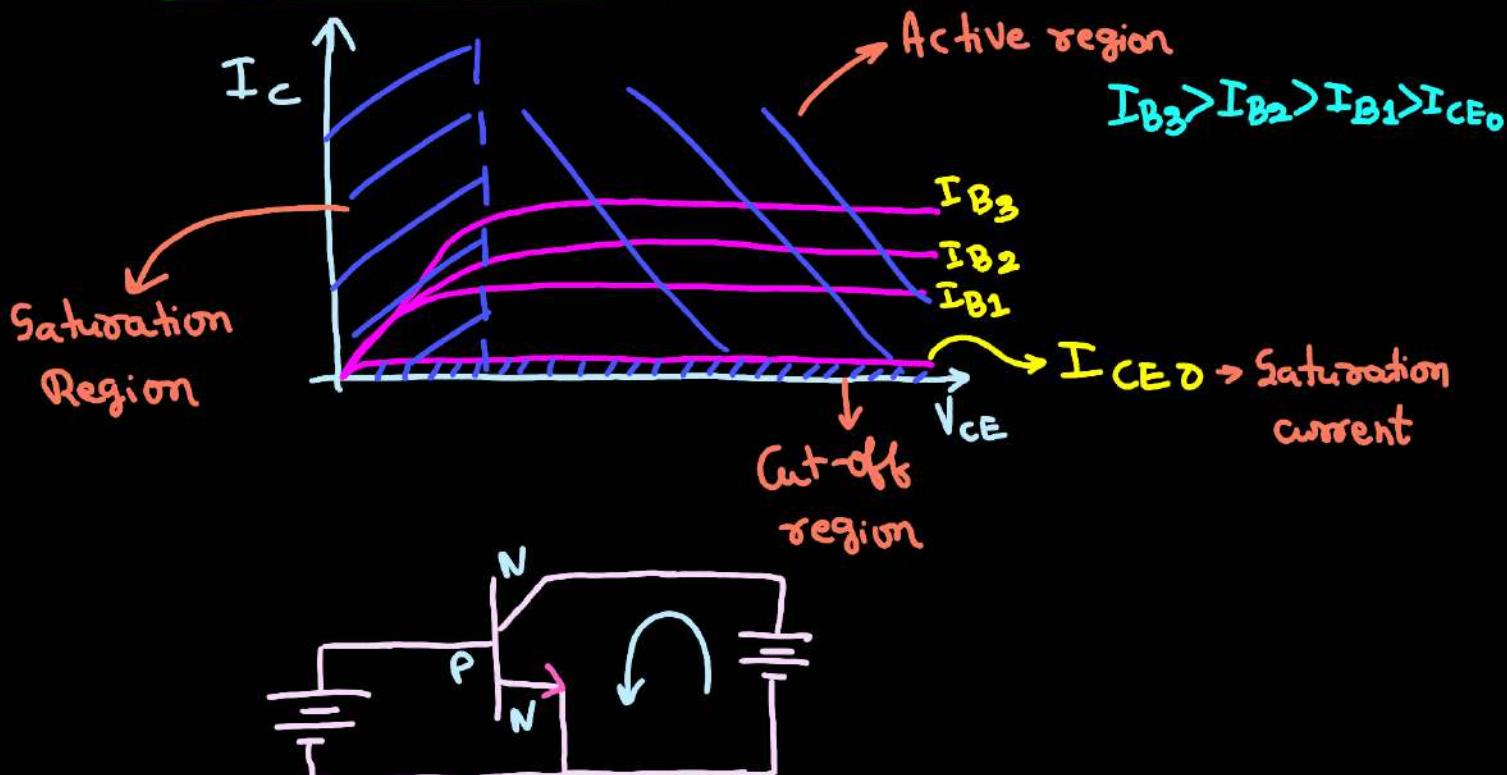
$$\textcircled{2} \quad h_{re} = \left. \frac{\Delta V_{BE}}{\Delta V_{CE}} \right|_{I_B}$$

reverse voltage ratio      (E Config)

$$\{ V_{C2} > V_{C1} > V_{CE(0)} \}$$

graph goes forward as O/P  $\uparrow$   
(Unlike CB, where graph goes backward)

## Output characteristics :-



$$\textcircled{1} \quad h_{oe} = \left. \frac{\Delta I_c}{\Delta V_{CE}} \right|_{I_B}$$

O/P admittance

$$\textcircled{2} \quad h_{fe} = \left. \frac{\Delta I_c}{\Delta I_B} \right|_{V_{CE}} = \beta$$

forward current gain

## # Relation b/w $\alpha$ & $\beta$ :-

$$\text{W.K.T : } I_E = I_B + I_C \quad \text{dividing by } I_C \text{ throughout}$$

$$\underline{I_E} = \underline{I_B} + \underline{I_C}$$

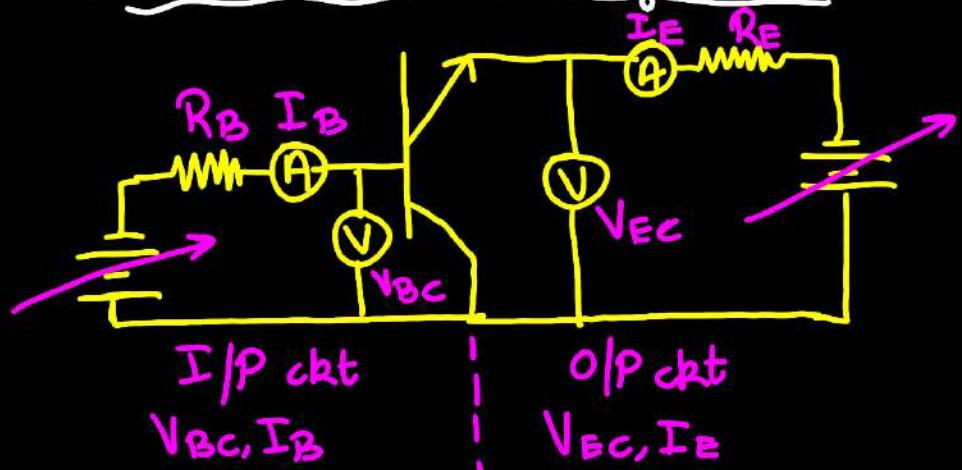
$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\Rightarrow \frac{1}{\alpha} = \frac{1}{\beta} + 1$$

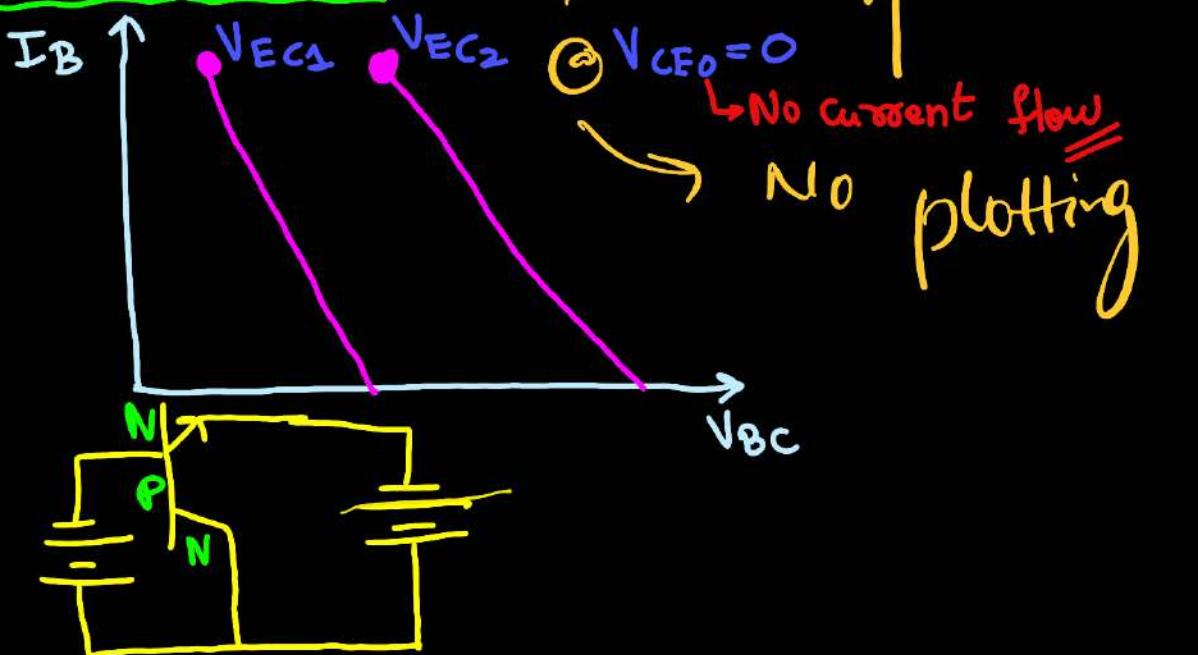
$$\alpha = \frac{I_C}{I_E} \quad \beta = \frac{I_C}{I_B}$$

Required relation

## # Common Collector Configuration :-



### # I/P characteristics :-



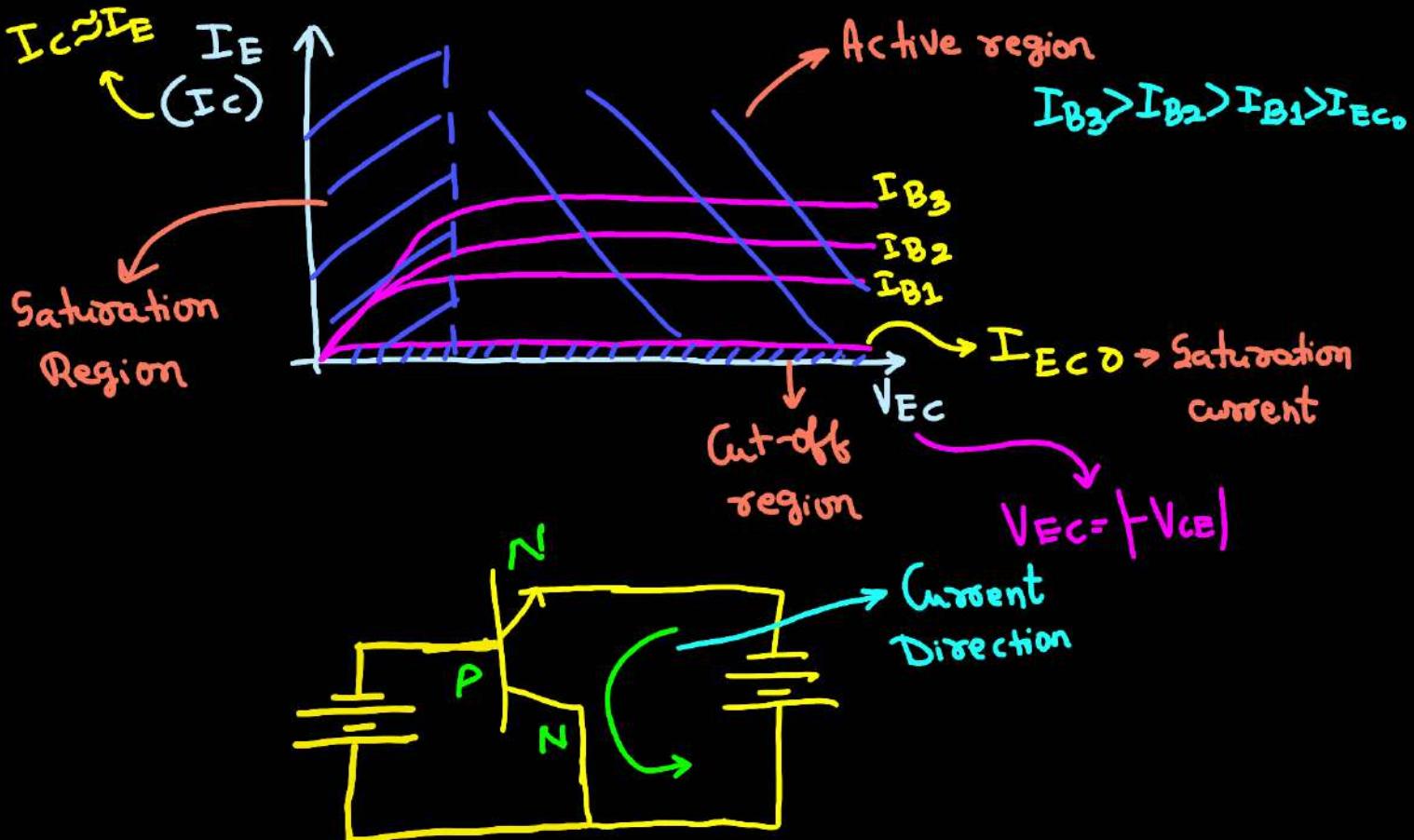
$$\textcircled{1} h_{ic} = \left. \frac{\Delta V_{Bc}}{\Delta I_B} \right|_{V_{Ec}}$$

I/P impedance

$$\textcircled{2} h_{oc} = \left. \frac{\Delta V_{Bc}}{\Delta V_{Ec}} \right|_{I_B}$$

Reverse voltage ratio

## O/P characteristics:-



$$\textcircled{1} h_{OC} = \left. \frac{\Delta I_E}{\Delta V_{EC}} \right|_{I_B}$$

O/P admittance

$$\textcircled{2} h_{fC} = \left. \frac{\Delta I_E}{\Delta I_B} \right|_{V_{EC}} = \left\{ \begin{array}{l} \text{forward} \\ \text{current gain} \end{array} \right.$$

## # Relation b/w $\alpha$ , $\beta$ , $\gamma$ :

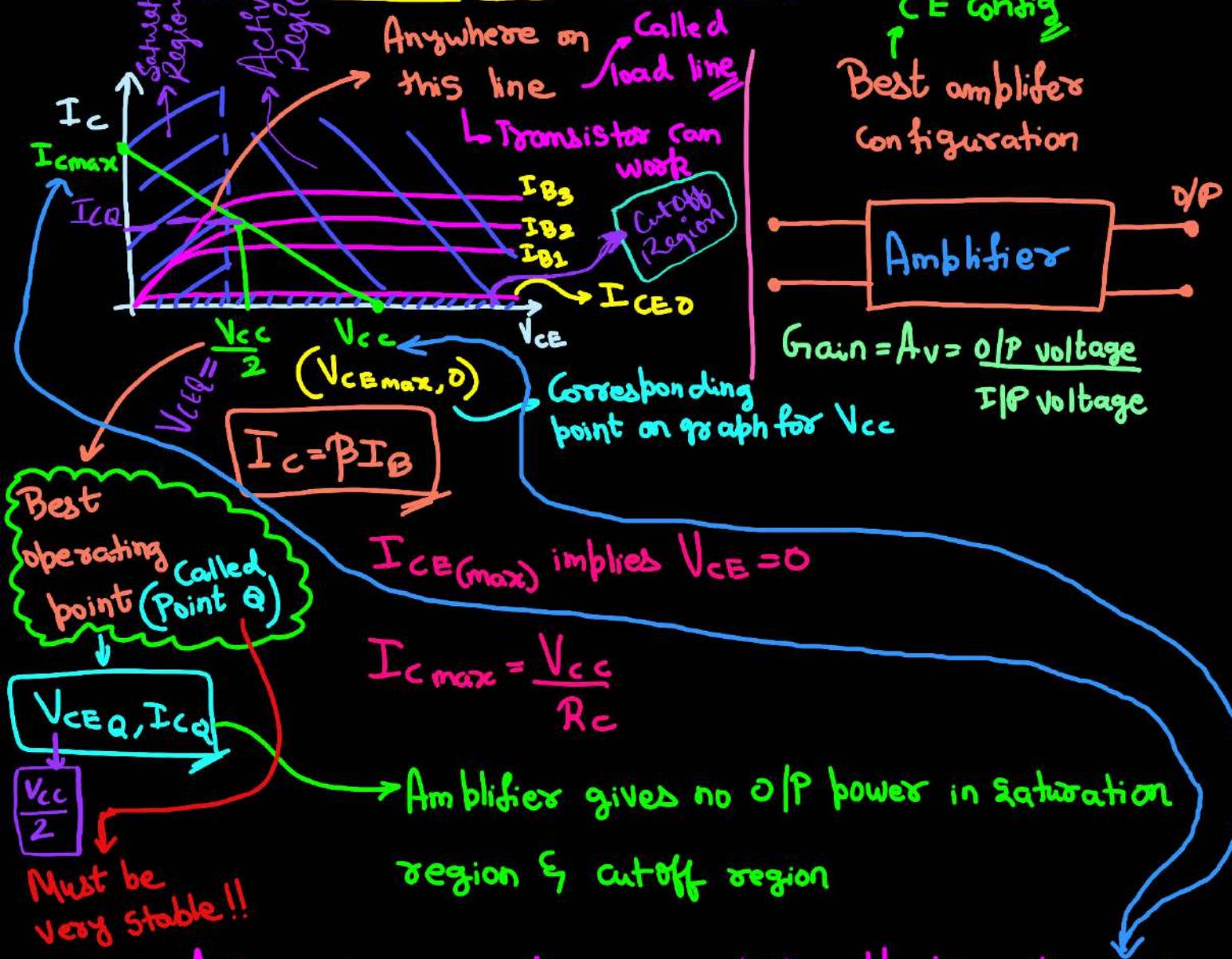
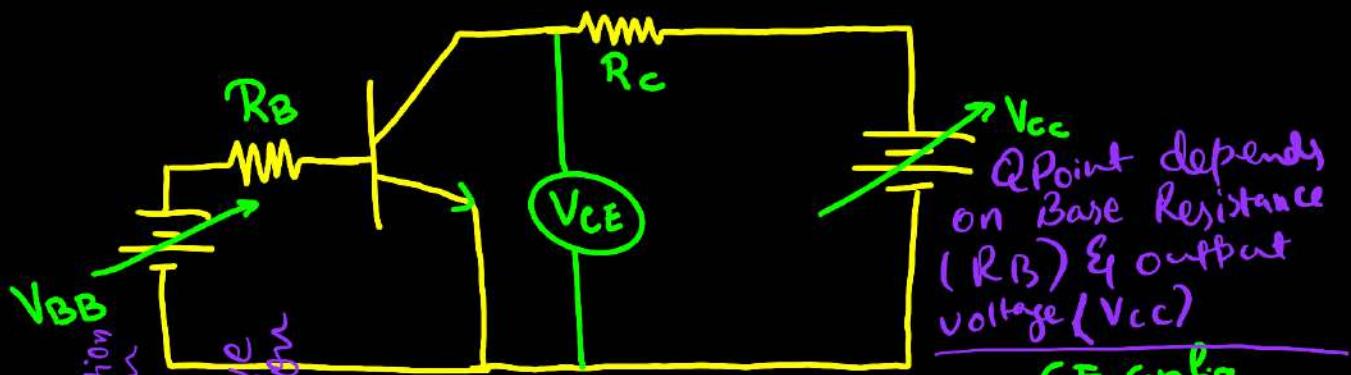
$$\gamma = \beta + 1$$

$$\gamma = \frac{1}{1-\alpha}$$

\*Derivation not necessary

# DC analysis:- This page was covered in POE

Consider CE Configuration & its O/P characteristics



★ Transistor can work as an amplifier b/w these two points ( $V_{cc}$  &  $I_{c\max}$ )

★ Load Line:- Locus of the transistor operating points

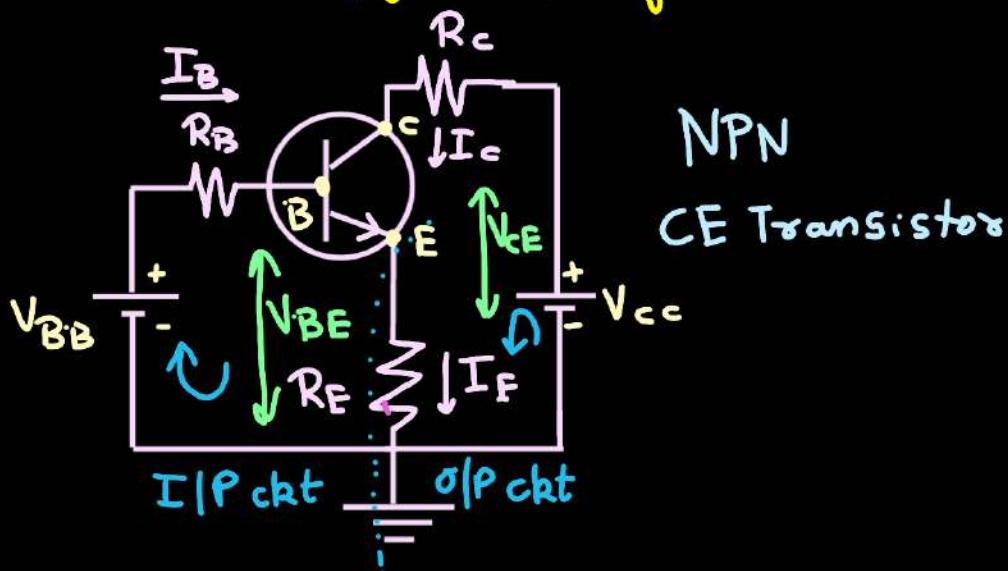
$$V_{ceQ} = \frac{V_{cc}}{2}; I_{cQ} = I_c$$

O/P operating point written again below

End of POE notes

# DC Biasing, Load line & Operating point

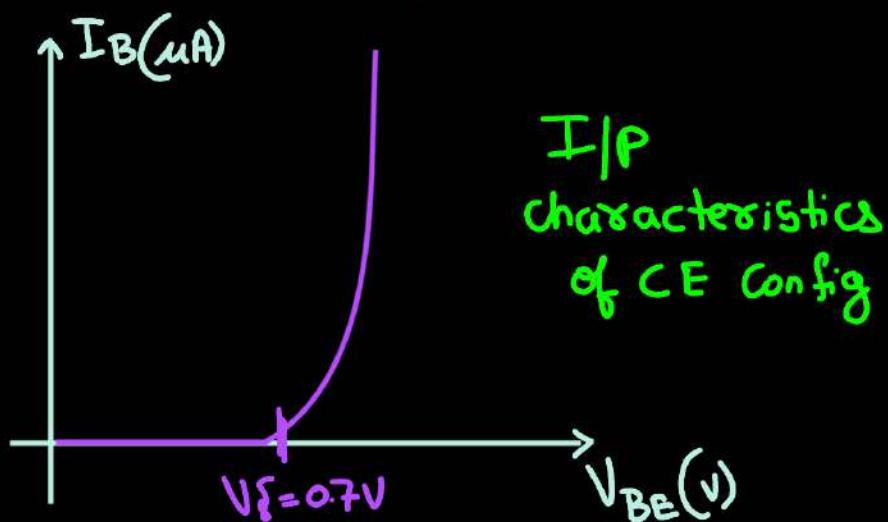
Consider the CE configuration of BJT



We need to amplify the weak I/P signal w/o any  
 distortion  
 i.e faithful amplification

# Input operating point :-

The coordinates obtained by the intersection of load line with the transistor I/P characteristics for the particular value of O/P voltage  $V_{CE}$



Applying KVL in the I/P circuit

$$\Rightarrow +V_{BB} - I_B R_B - V_{BE} = 0$$

Drawing load line using this eqn

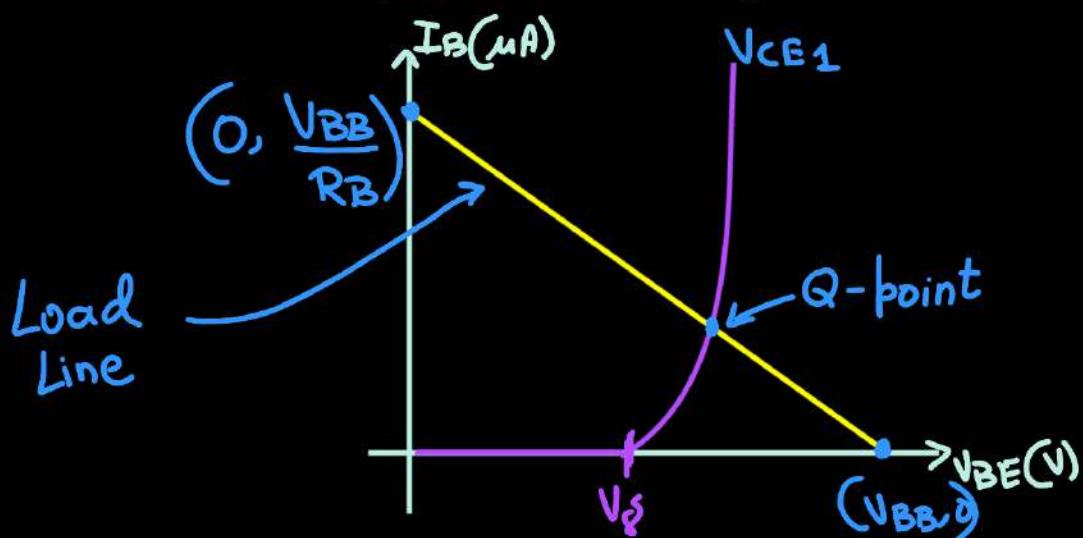
$$P_1 = (0, \infty) \quad P_2 = (-\infty, 0)$$

$$\text{When } V_{BE} = 0 \Rightarrow I_B = \frac{V_{BB}}{R_B}$$

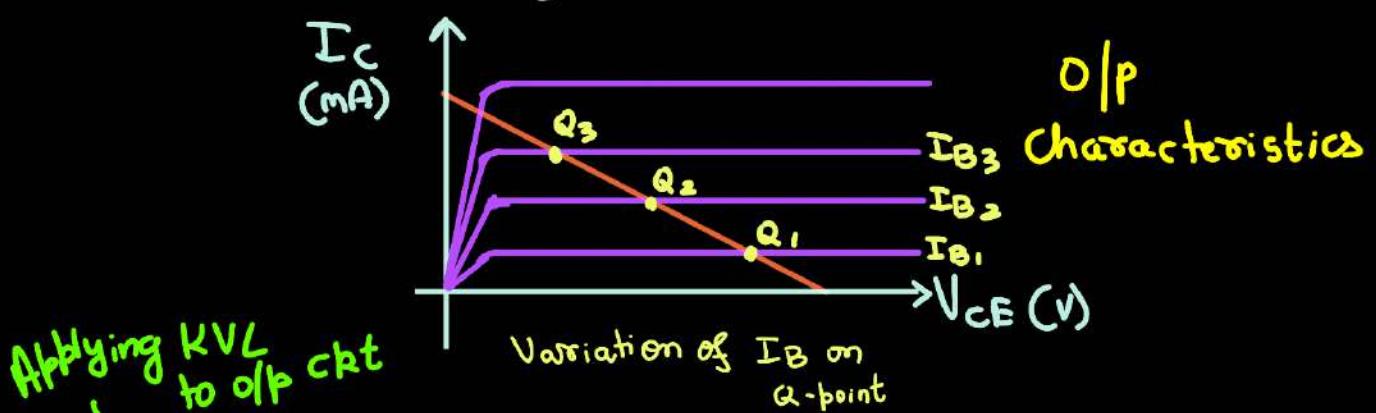
$$I_B = 0 \Rightarrow V_{BE} = V_{BB}$$

$$\Rightarrow P_1 = \left( 0, \frac{V_{BB}}{R_B} \right)$$

$$\Rightarrow P_2 = (V_{BB}, 0)$$



## # Output operating point



Applying KVL to o/p ckt

$$V_{CC} - I_C R_C - V_{CE} = 0$$

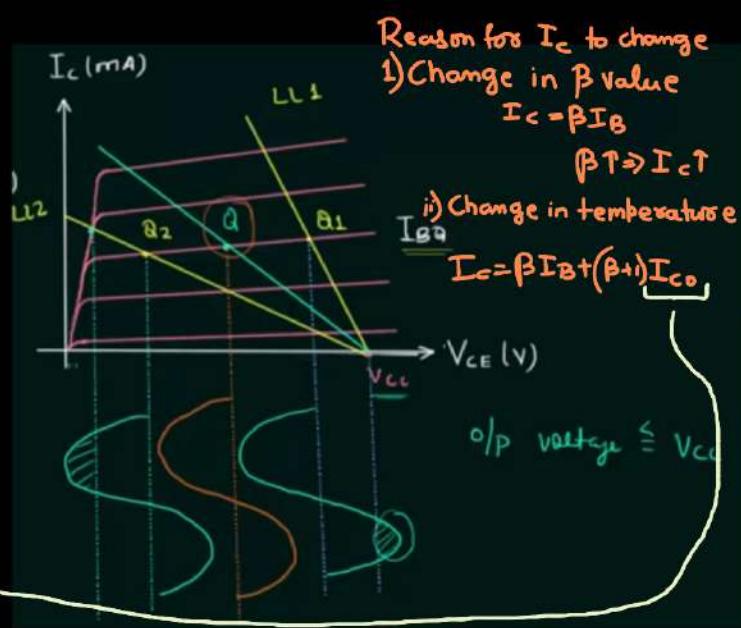
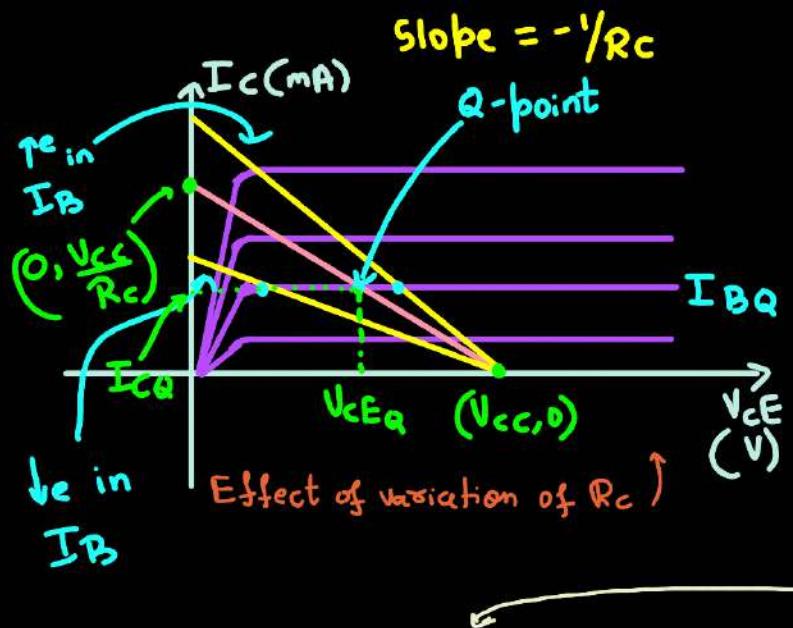
$\curvearrowleft$   $y$ -axis

By making  $V_{CE} = 0$

Variation of  $I_B$  on  $Q\text{-point}$

$\curvearrowleft$   $x$ -axis

$\hookrightarrow$  By making  $I_C = 0$



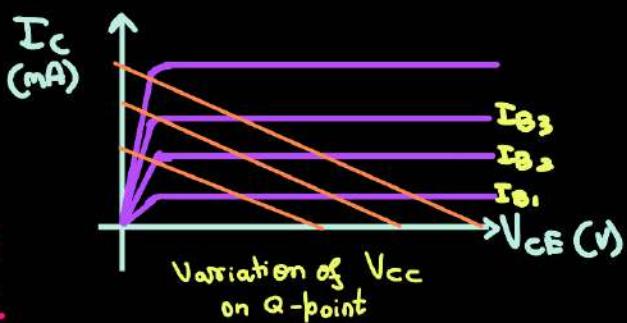
Leakage current or  
↓ rev sat curr

Depends only on  
minority charge carriers

Fig above:- Setting of probes  
Operating point

### # Types of biasing circuits :-

- 1) Fixed bias configuration
- 2) Emitter bias configuration
- 3) Collector-feedback configuration
- 4) Voltage divider configuration
- 5) Emitter follower configuration
- 6) Common Base configuration

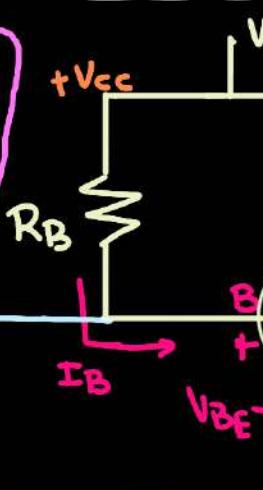


### # Fixed-Bias Configuration :- AKA Base-bias configuration

C.C's are ignored in DC analysis as  $X_C = \frac{1}{2\pi f C}$   
 $f=0$  for DC  $\Rightarrow X_C = \infty$

Thus replaced by open opt

I/P AC signal



Simplest configuration

Potential at point (not diff)

O/P AC signal

Coupling Capacitors

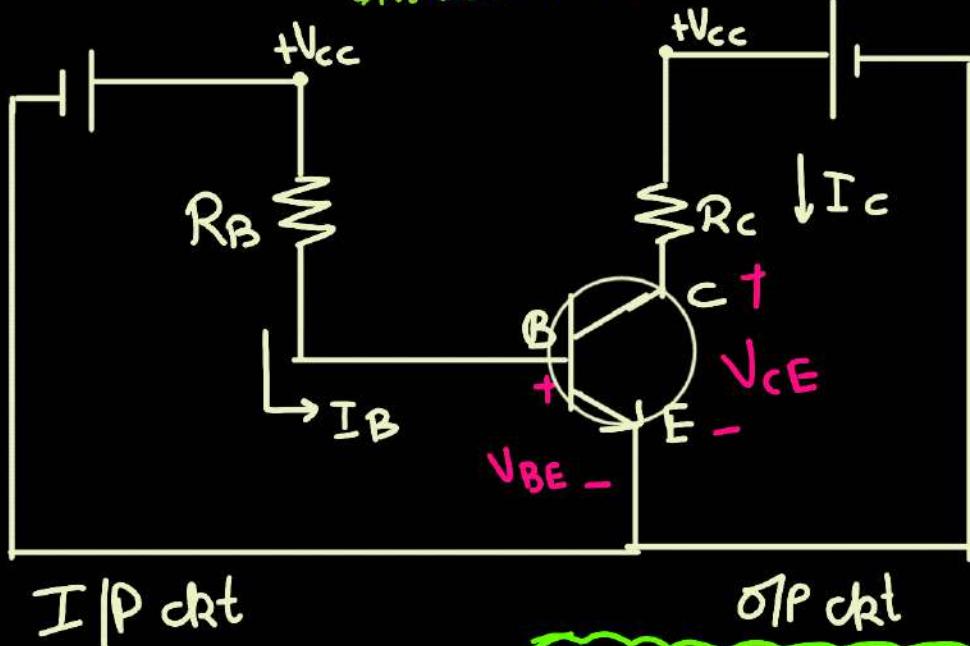
Note on Coupling capacitors

We can rewrite the ckt as

↳ For easier analysis

To obtain :-  $I_C = ?$

$V_{CE} = ?$



I/P ckt

O/P ckt

Applying KVL to i/p ckt

Emitter-Base junction is F.B by  $V_{cc}$   
Collector-Base junction is R.B by  $V_{cc}$

$$+V_{cc} - I_B R_B - V_{BE} = 0$$

WKT,

$$I_B = \frac{V_{cc} - V_{BE}}{R_B} \Rightarrow I_C = \beta I_B$$

$\therefore I_C = \frac{\beta(V_{cc} - V_{BE})}{R_B}$

$= 0.7V$  for Si  
 $= 0.3V$  for Ge

Applying KVL for O/P ckt :- ↗ i.e., the collector emitter loop

$$+V_{cc} - I_C R_c - V_{CE} = 0$$

$\Rightarrow V_{CE} = V_{cc} - I_C R_c$

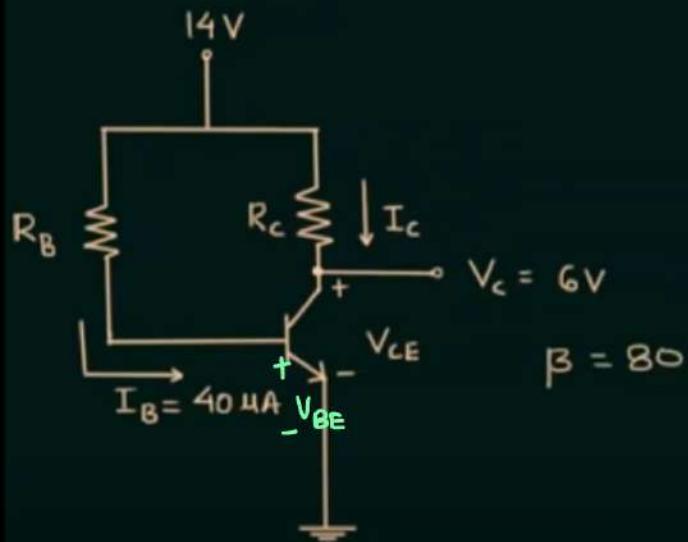
$\therefore Q\text{-point} = \left( V_{cc} - I_C R_c, \frac{\beta(V_{cc} - V_{BE})}{R_B} \right)$

Q) For the fixed bias config determine:-

- i)  $I_c$
- ii)  $R_c$
- iii)  $R_B$
- iv)  $V_{CE}$

$$\text{Soln} :- V_{CC} = 14V ; \beta = 80$$

$$I_B = 40\mu A ; V_C = 6V$$



a)  $I_c = \beta I_B$   
 $= 80(40\mu A) = 3.2mA$

b) Applying KVL to outer loop

$$14V - I_c R_c = 6$$

$$R_c = \frac{14 - 6}{I_c} = \frac{8}{3.2mA}$$

$$R_c = 2.5k\Omega$$

c) Applying KVL to IP loop:-

$$14V - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{14 - V_{BE}}{I_B} = \frac{13.3}{40\mu} = 332.5k\Omega$$

iv)  $V_{CE} = V_C - V_E$   
 $= 6V - 0$

$$V_{CE} = 6V$$

Q) For the fixed bias config determine:-

- i)  $I_C$
- ii)  $V_{CC}$
- iii)  $\beta$
- iv)  $R_B$

$$\text{Given :- } R_C = 2.7 \text{ k}\Omega \quad | \quad I_E = 4 \text{ mA}$$

$$I_B = 20 \mu\text{A} \quad | \quad V_{CE} = 7.2 \text{ V}$$

Soln:-

$$\text{a) } I_E = I_C + I_B$$

$$\Rightarrow I_C = I_E - I_B = 4 \text{ mA} - 20 \mu\text{A}$$

$$\Rightarrow \boxed{I_C = 3.98 \text{ mA}}$$

b) Applying KVL in outer loop

$$V_{CC} - I_C (2.7 \text{ k}\Omega) - 7.2 \text{ V} = 0$$

$$V_{CC} = 3.98 (2.7 \times 10^3) \times 10^{-3} + 7.2$$

$$\boxed{V_{CC} = 17.946 \text{ V}}$$

$$\text{c) } \beta = \frac{I_C}{I_B} = \frac{3.98 \text{ mA}}{20 \mu\text{A}} = 199$$

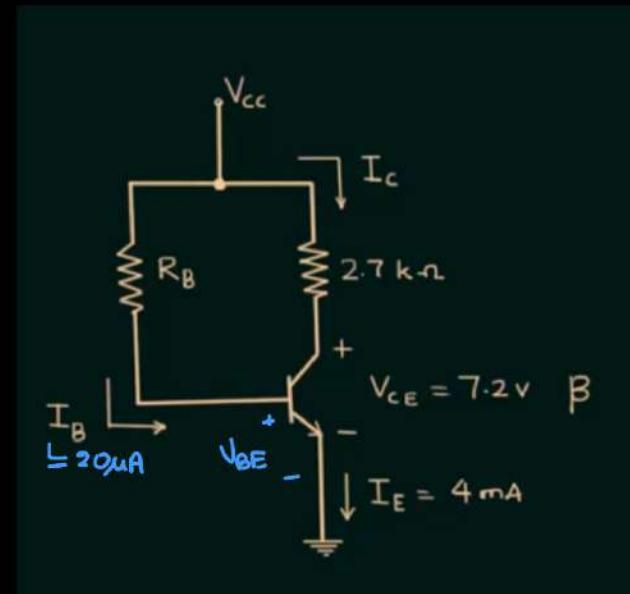
$$\boxed{\beta = 199}$$

d) Applying KVL in input loop

$$V_{CC} - I_B R_B - V_{BE} = 0$$

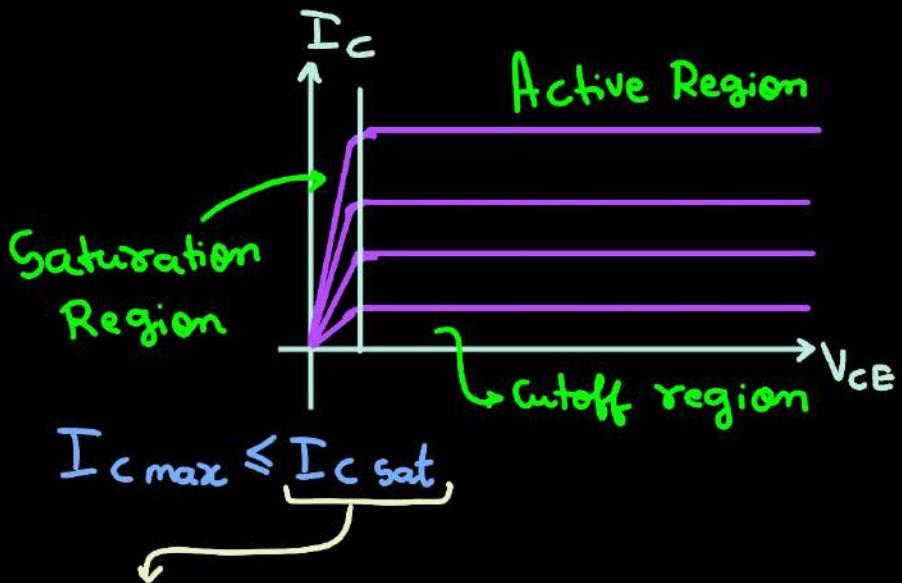
$$= 17.946 - 20 \mu(R_B) - 0.7 \text{ V} = 0$$

$$\Rightarrow R_B = \frac{17.946 - 0.7}{20 \mu} \Rightarrow \boxed{R_B = 862.3 \text{ k}\Omega}$$



## \* Transistor Saturation :-

Transistor is said to be saturated if  $I_c > (I_c)_{\max}$  for the particular design



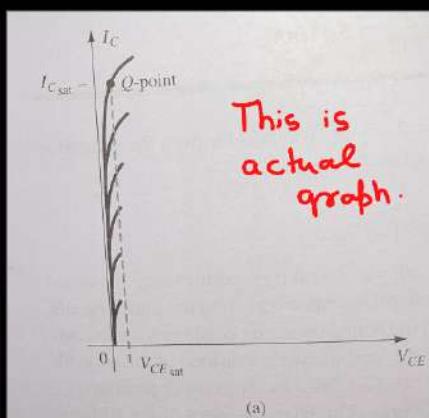
We generally avoid saturation conditions because the Collector-Base junction is forward biased & there is distortion in the amplified signal

For amplification  $\Rightarrow$  transistor must work in active region

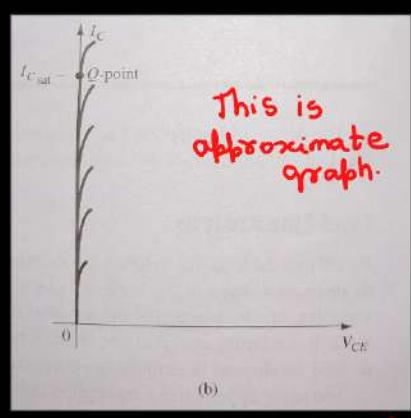
resistance offered  $\approx 0$  {  $\begin{matrix} CB J^n \\ F.B \downarrow \\ EB J^n \\ R.B \end{matrix}$  }

When  $I_{c\max} \leq I_{c\text{sat}}$   $\Rightarrow$  transistor operates in the saturation region

Graphs of saturation region  $\Rightarrow$



This is actual graph.



This is approximate graph.

observe the  
difference

$$V_{CE} = 0V$$

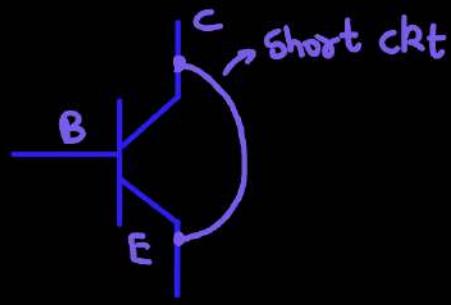
$I_{c\text{sat}} \rightarrow$  relatively high

Applying Ohm's law  $\Rightarrow I_{c\text{sat}} \cdot R_{CE} = V_{CE}$

$$R_{CB} = \frac{0}{I_{\text{sat}}} \Rightarrow R_{CE} = 0 \Omega$$

No resistance  
b/w C & E

$\Rightarrow C \& E$  can be short ckt  $\Rightarrow$



\* Saturation Cond'n for fixed-bias Configuration

$$I_{C\text{sat}} = I_{C\text{max}}$$

Applying KVL to o/p loop

$$\Rightarrow V_{CC} - I_{C\text{sat}} R_C = 0$$

$$\Rightarrow I_{C\text{sat}} = \frac{V_{CC}}{R_C}$$

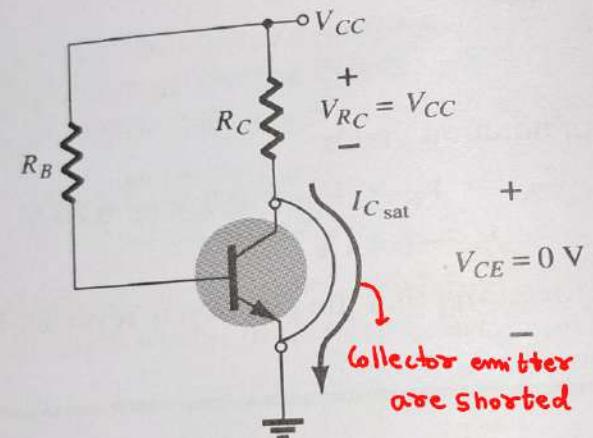


FIG. 4.10

Determining  $I_{C\text{sat}}$  for the fixed-bias configuration.

# Emitter-Bias Configuration :-  $Q\text{-Pt} = (I_{CQ}, V_{CEQ})$

Difference b/w fixed bias

Emitter bias is resistance  $R_E$

Improve the stability  
of the operating pt.

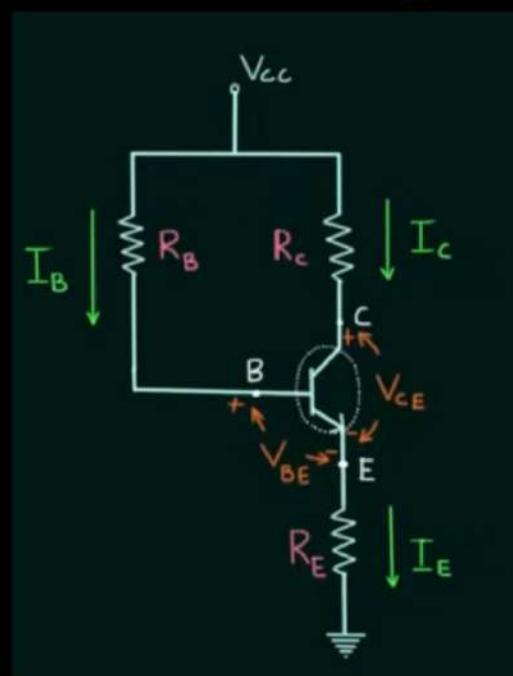
To find  $I_{CQ}$ , apply KVL to i/p loop

$$\Rightarrow V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

WKT,

$$I_E = I_C + I_B = \beta I_B + I_B \Rightarrow I_E = (\beta + 1) I_B$$

$$\Rightarrow V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$



$$V_{CC} - I_B(R_B + (\beta+1)R_E) - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_E} \rightarrow \text{Base Current}$$

$$\Rightarrow I_C = \beta I_B = \beta \left( \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_E} \right) = I_{CQ}$$

Collectors current  
 $I_C = I_{CQ}$

Applying KVL to O/P loop:-

$$\Rightarrow V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0 \quad (I_E \approx I_C)$$

$$\Rightarrow V_{CC} - I_C (R_C + R_E) - V_{CE} = 0$$

$$V_{CEQ} = V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Advantage of using  $R_E$  :-

\* When  $T \uparrow \Rightarrow I_C \uparrow \Rightarrow$  changes Q-point  $\rightarrow$  undesired

$$I_C = \left\{ \beta I_B + (\beta+1) I_{CO} \right\}$$

$\downarrow$  Leakage / Rev. Sat. current

when  $I_C \uparrow \Rightarrow I_E R_E \uparrow \quad (I_C \approx I_E)$

$$I_B \downarrow \Rightarrow I_C \downarrow \quad (I_C = \beta I_B)$$

$\therefore$  Increment in  $I_C$  due to increase in temp is equally compensated by the decrement in  $I_B \Rightarrow$  This occurs only due to introduction of  $R_E$  (Temp no longer has any effect)

$\therefore$  Adv. 1

\* When  $\beta$  changes  $I_C$  also changes

$$\Rightarrow I_C = \beta I_B$$

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B + (\beta+1)R_E} \quad \left. \begin{array}{l} \beta \gg 1 \\ \Rightarrow \beta+1 \approx \beta \end{array} \right\}$$

$$\Rightarrow I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B + \beta R_E}$$

$$\beta R_E \gg R_B \Rightarrow I_C = \frac{(V_{CC} - V_{BE})}{R_E} \quad \left. \begin{array}{l} I_C \text{ is independent of} \\ \beta \end{array} \right\}$$

∴ Change in  $\beta$  does not affect  $I_C$

Possible only  
due to  $R_E$   
↓  
Adv. 2

### \* Disadvantages:-

\* To have  $I_C$  independent of  $\beta \Rightarrow$  the cond' is  $\beta R_E \gg R_B$

But we do not know  $\beta$  most of the time]

This will increase the cost  $\Leftarrow$  ∵  $R_E$  must be very high  $\Rightarrow R_B$  must be very low

The  $R_B$  of C-B j<sup>n</sup> will reduce

Q) For the emitter bias config determine:-

i)  $R_C$    iii)  $R_B$    ii)  $V_B$

ii)  $R_E$    iv)  $V_{CE}$

Soln :-  $I_C = 3\text{mA}$ ;  $\beta = 80$ ;  $V_C = 7.6\text{V}$   
 $V_E = 2.4\text{V}$ ;  $V_{CC} = 12\text{V}$

c)  $V_{BE} = 0.7\text{V}$  ( $S_1$ )

$$V_B - V_E = 0.7\text{V}$$

$$V_B - 2.4\text{V} = 0.7\text{V} \Rightarrow V_B = 3.1\text{V}$$

d)  $V_{CE} = V_C - V_E = 7.6\text{V} - 2.4\text{V} \Rightarrow V_{CE} = 5.2\text{V}$

e) Applying KVL in input loop

$$12 - I_B R_B = V_B \Rightarrow 12 - I_B R_B = 3.1\text{V}$$

WKT,  $I_B = \frac{I_C}{\beta} = \frac{3\text{mA}}{80} \Rightarrow I_B = 37.5\mu\text{A}$

$$\Rightarrow R_B = \frac{12\text{V} - 3.1\text{V}}{37.5\mu\text{A}} \Rightarrow R_B = 237.4\text{k}\Omega$$

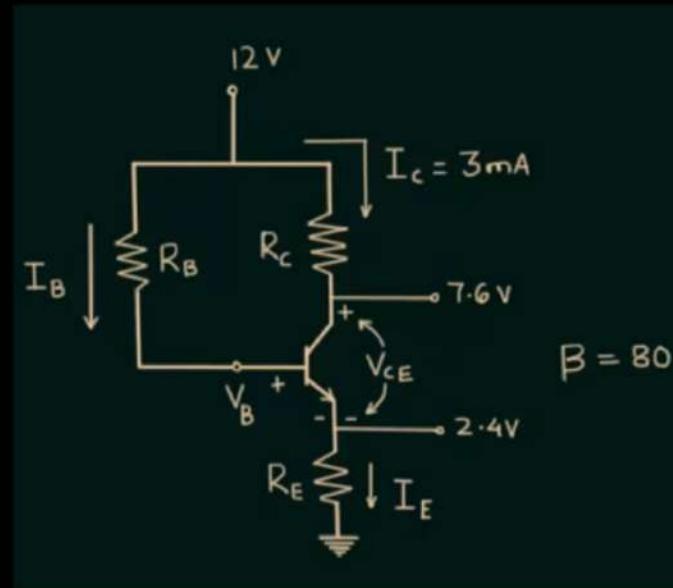
b) Applying KVL from  $2.4\text{V}$  to GND

$$\Rightarrow 2.4\text{V} - I_E R_E = 0$$

$$\Rightarrow 2.4\text{V} = I_C R_E \quad (I_E \approx I_C) \Rightarrow R_E = \frac{2.4\text{V}}{3\text{mA}} \Rightarrow R_E = 0.8\text{k}\Omega$$

a) Applying KVL from  $V_{CC}$  to  $7.6\text{V}$

$$\Rightarrow 12 - I_C R_C = 7.6 \Rightarrow \frac{12 - 7.6}{3\text{mA}} = R_C \Rightarrow R_C = 1.47\text{k}\Omega$$



## Saturation Cond' for emitter-bias configuration

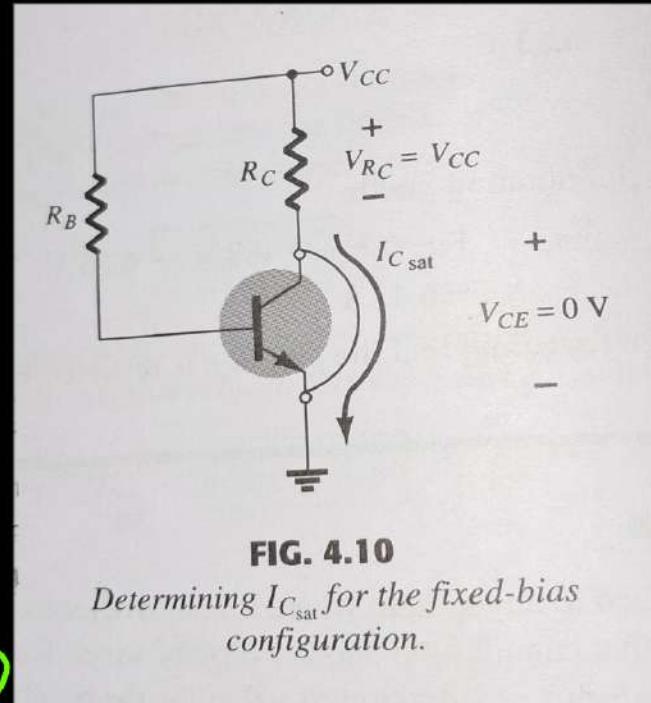
Applying KVL in the  $\delta/\beta$  loop

$$\Rightarrow V_{CC} - I_{C\text{sat}} R_C - I_E R_E = 0$$

$$I_E \approx I_{C\text{sat}}$$

$$\Rightarrow V_{CC} - I_{C\text{sat}}(R_C + R_E) = 0$$

$$\Rightarrow I_{C\text{sat}} = I_{C\text{max}} = \frac{V_{CC}}{R_C + R_E}$$



## # Collector-Feedback Bias Configuration:-

In emitter biasing,  $R_E$  was introduced which improved stability of Q-point.

This can also be achieved by introducing of feedback from collector to base.  $\rightarrow$  Achieved in this config

Applying KCL at node n

$$\Rightarrow I = I_c + I_B \quad \begin{matrix} \text{Apply KVL to find this} \\ \Downarrow \end{matrix}$$

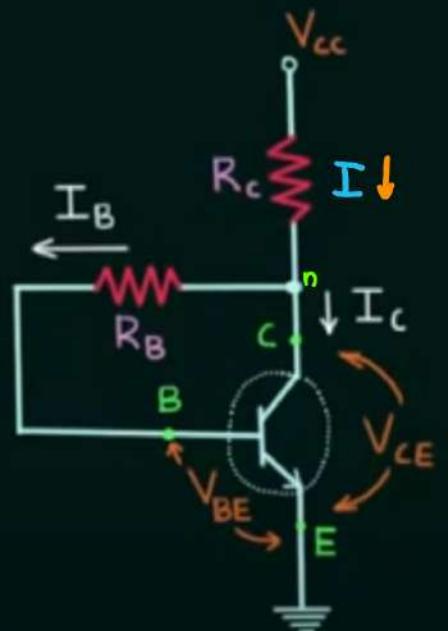
$$V_{CC} - (I_c + I_B)R_C - I_B R_B - V_{BE} = 0$$

$$\text{WKT, } I_c = \beta I_B$$

$$\Rightarrow V_{CC} - [(\beta + 1)R_C + R_B] I_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{(\beta + 1)R_C + R_B}$$

$$I_c = \frac{\beta(V_{CC} - V_{BE})}{(\beta + 1)R_C + R_B}$$



## Applying KVL in O/P loop :-

$$V_{CC} - I R_C - V_{CE} = 0$$

$$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - (I_C + I_B) R_C$$

## Advantages:-

★ Stabilises Q-pt against → i) Variation of temperature

Proof

ii) Variation of  $V_{CC}$   
iii) — " — " —  $\beta$

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B + (\beta+1)R_C}$$

$$\beta+1 \approx \beta \Rightarrow \beta R_C \gg R_B$$

$$\Rightarrow I_C = \frac{\beta(V_{CC} - V_{BE})}{\beta R_C} \Rightarrow I_C = \frac{(V_{CC} - V_{BE})}{R_B}$$

Independent of  $\beta$  //

## Disadvantages:-

★ To have  $I_C$  independent of  $\beta \Rightarrow$  the cond' is  $\boxed{\beta R_C \gg R_B}$

But we do not know  $\beta$  most of the time ↴

This will increase the cost ← ∵  $R_C$  must be very high  
⇒  $R_B$  must be very high

The  $R_B$  of C-B JFET will reduce

Q) Figure shows a silicon transistor biased by collector-feedback method. Determine operating point if  $\beta = 100$ .

Sol:-

$$Q-Point = (I_C, V_{CE})$$

Applying KVL in I/P loop

$$V_{CC} - (I_C + I_B)(1\text{ k}\Omega) - I_B(100\text{ k}\Omega) - V_{BE} = 0$$

$$0.3\text{ V}$$

$$\Rightarrow I_B = \frac{V_{CC} - 0.7\text{ V}}{(\beta + 1)(1\text{ k}\Omega) + 100\text{ k}\Omega} \Rightarrow I_B = \frac{19.3\text{ V}}{201\text{ k}\Omega}$$

$$\Rightarrow I_B = 0.096\text{ mA} \Rightarrow I_B = 96\mu\text{A}$$

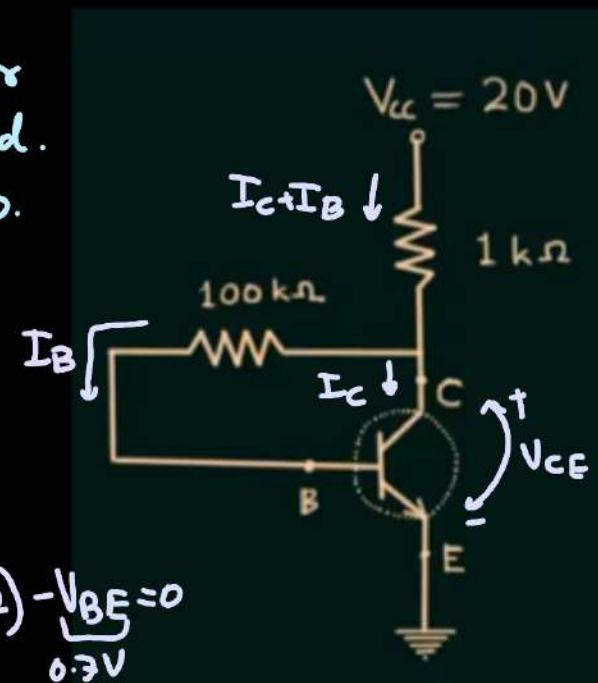
$$\therefore I_C = \beta I_B = 100 \times 96\mu\text{A} \Rightarrow I_C = 9.6\text{ mA}$$

Applying KVL in O/P loop:-

$$V_{CC} - (I_C + I_B)(1\text{ k}\Omega) - V_{CE} = 0$$

$$V_{CE} = 10.304\text{ V}$$

$$\therefore Q-Point = (9.6\text{ mA}, 10.304\text{ V})$$



## # Collector Feedback biasing with Emitter Resistor

Combination of both emitter biasing & collector feedback biasing (above)

Applying KVL in I/P loop :-

$$V_{CC} - I R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$\downarrow I = I_c + I_B$  (From KCL at node n)

$$V_{CC} - (I_c + I_B) R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = I_c + I_B = \beta I_B + I_B = (\beta + 1) I_B$$

$$\Rightarrow V_{CC} - (\beta + 1) I_B R_C - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\Rightarrow V_{CC} - I_B \left[ (\beta + 1)(R_C + R_E) + R_B \right] - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + [(\beta + 1)(R_C + R_E)]}$$

$$I_c = \frac{\beta (V_{CC} - V_{BE})}{R_B + (\beta + 1)(R_C + R_E)}$$

Will be independent of  $\beta$  if

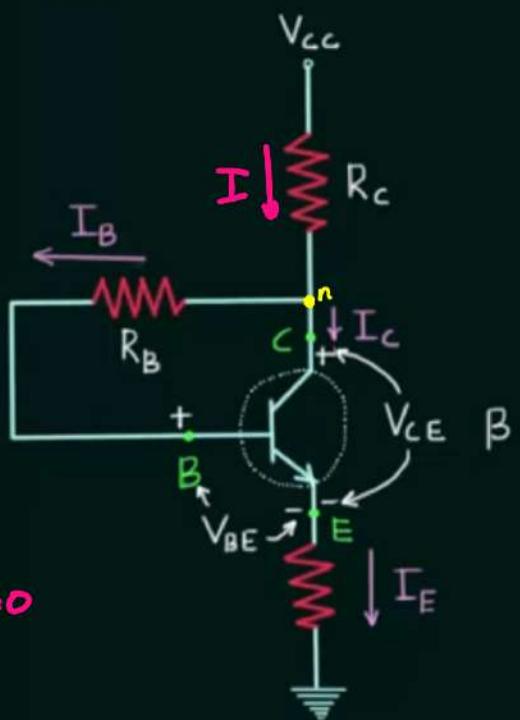
$$R_B \ll (\beta + 1)(R_C + R_E)$$

Apply KVL in O/P loop:-

$$\Rightarrow V_{CC} - (I_c + I_B) R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} - I_E R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} - I_E (R_E + R_C) - V_{CE} = 0 \quad (I_c \approx I_E)$$



$$\Rightarrow V_{CC} - I_C(R_C + R_E) - V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C(R_C + R_E) = 0$$

## \* Saturation Condition for Collector-feedback config

$I_{C\text{sat}} = I_{C\text{max}} = \frac{V_{CC}}{R_C + R_E}$

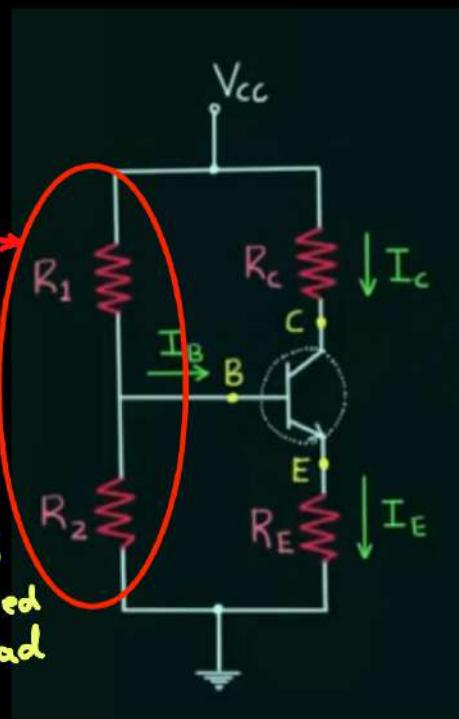
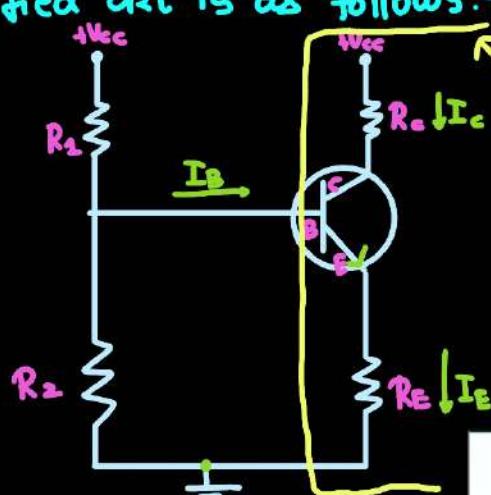
Taken from T.B  
Had only for config with  $R_E \parallel$

## # Voltage-Divider Bias Configuration

### \* Most widely used biasing scheme

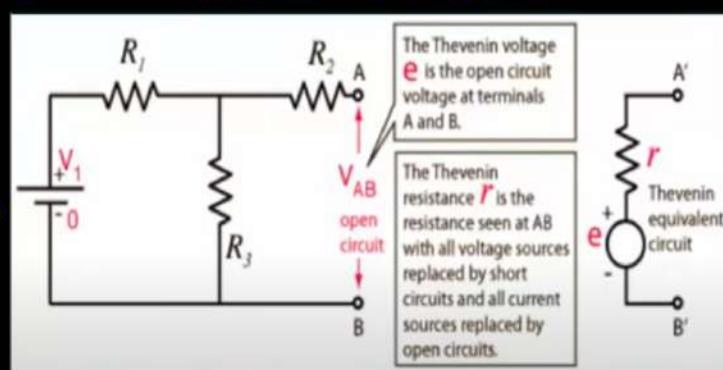
Called Voltage divider bias because voltage divider network is used to bias the transistor

The modified ckt is as follows:-

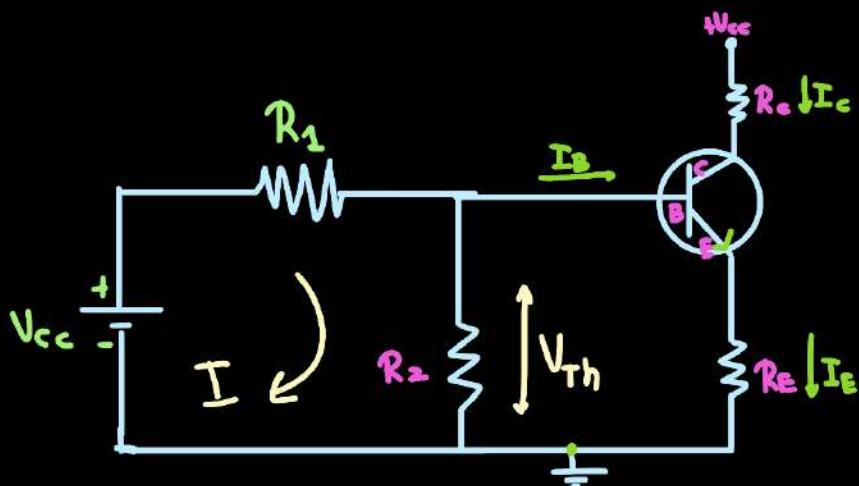


Q-point is found using Thevenin's theorem

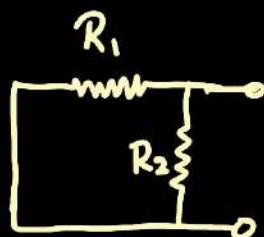
Overview / Revision of Thevenin's theorem



Finding Thevenin ckt :- The ckt can be rewritten as follows



Find  $R_{Th}$  :-



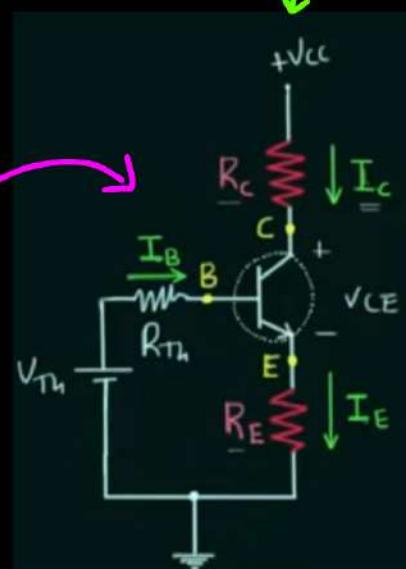
$$R_{Th} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Finding  $V_{Th}$  :-  $I = \frac{V_{cc}}{R_1 + R_2}$  (From KVL)

$$\Rightarrow V_{Th} = IR_2 = \frac{R_2 V_{cc}}{R_1 + R_2}$$

Thevenin equivalent  
ckt

Observing carefully  
this is emitter bias  
configuration



\* Saturation Condition

$$I_{C\max} = I_{Csat} = \frac{V_{cc}}{R_c + R_E}$$

## Applying KVL in I/P loop

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$V_{Th} - I_B R_{Th} - V_{BE} - (\beta + 1) I_B R_E = 0$$

Condition to make  
I<sub>c</sub> ind. of β  
 $\Rightarrow R_{Th} \ll (\beta + 1) R_E$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E} \Rightarrow \left\{ \begin{array}{l} I_c = \frac{\beta (V_{Th} - V_{BE})}{R_{Th} + (\beta + 1) R_E} \\ \qquad \qquad \qquad \end{array} \right.$$

## Applying KVL to O/P loop

$$\Rightarrow V_{cc} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{cc} - I_C (R_C + R_E) - V_{CE} = 0 \Rightarrow V_{CE} = V_{cc} - I_C (R_C + R_E)$$

### \* Advantages:-

\* R<sub>Th</sub> is parallel value of R<sub>1</sub> & R<sub>2</sub>, whereas R<sub>B</sub> is a single resistor.

$$\therefore R_{Th} < R_B$$

\* To make I<sub>c</sub> independent of β  $\Rightarrow \underbrace{R_{Th}}_{\downarrow} \ll (\beta + 1) R_E$

Reducing single resistor R<sub>B</sub> has  $\Leftrightarrow \left\{ \begin{array}{l} R_{Th} \text{ is a small value in this case} \\ \text{without reducing } R_1 \& R_2 \Rightarrow \text{Provides little flexibility in design.} \end{array} \right.$

Q) For the voltage divider bias config. determine :-

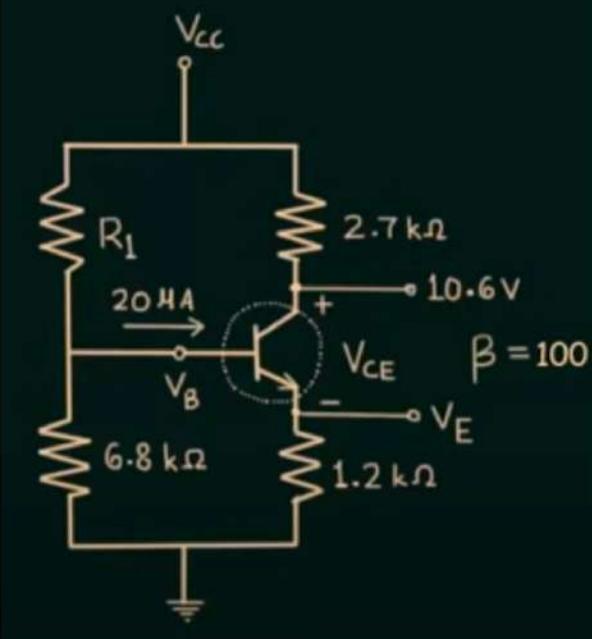
- a)  $I_C$
- b)  $V_E$
- c)  $V_{CC}$
- d)  $V_{CE}$
- e)  $V_B$
- f)  $R_1$

Soln:-

$$I_B = 20 \mu A; R_C = 2.7 k\Omega$$

$$V_C = 10.6 V; \beta = 100; R_2 = 6.8 k\Omega;$$

$$R_E = 1.2 k\Omega$$



Drawing thevenin's equivalent circuit

$$V_{Th} = \frac{V_{CC}R_2}{R_1 + R_2}; R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

a)  $I_C = \beta I_B = 100 \times 20 \mu A$   
 $\Rightarrow I_C = 2 mA$

b) Applying KVL from  $V_{CC}$  to  $10.6 V$

$$V_{CC} - I_C R_C = 10.6 V$$

$$V_{CC} = (2 mA)(2.7 k\Omega) + 10.6 V$$

$$\boxed{V_{CC} = 16 V}$$

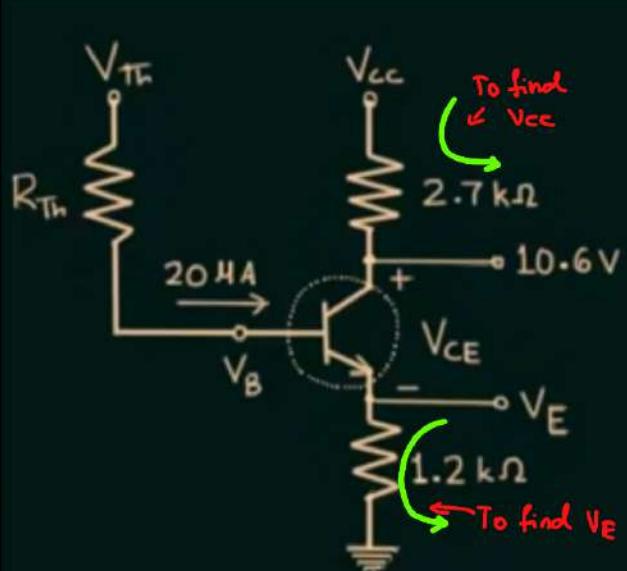
b)  $I_E = I_C + I_B$   
 $= 2 mA + 20 \mu A$   
 $\Rightarrow I_E = 2.02 mA$

Applying KVL from  $V_E$  to GND

$$V_E - I_E R_E = 0 \Rightarrow V_E = I_E R_E$$

$$= (2.02 mA)(1.2 k\Omega)$$

$$\Rightarrow \boxed{V_E = 2.424 V}$$



$$d) V_{CE} = V_C - V_E = 10.6V - 2.424V \\ \Rightarrow V_{CE} = 8.176V$$

$$e) V_{BE} = V_B - V_E$$

$$0.7V = V_B - 2.424V$$

$$\Rightarrow V_B = 3.124V$$

physically this is potential at point

$$f) V_{Th} \approx V_B \text{ (because drop across } R_{Th} \text{ is very small)}$$

$I_B$  is very small

$$\Rightarrow V_{Th} = \frac{V_{cc}R_2}{R_1 + R_2} = \frac{16 \times 6.8k\Omega}{R_1 + 6.8k\Omega}$$

$$\Rightarrow 3.124V = \frac{16 \times 6.8k\Omega}{R_1 + 6.8k\Omega} \Rightarrow R_1 = 28k\Omega$$

### # Emitter-follower configuration :-

In the previous sections we have seen off voltage typically taken off the collector terminal of the transistor. Now we will exam a config where the off is taken off the emitter terminal.

All the above configs can be used for this purpose as long as  $R_E$  is there.

Applying KVL to I/P ckt

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$\text{WKT, } I_E = (\beta + 1) I_B$$

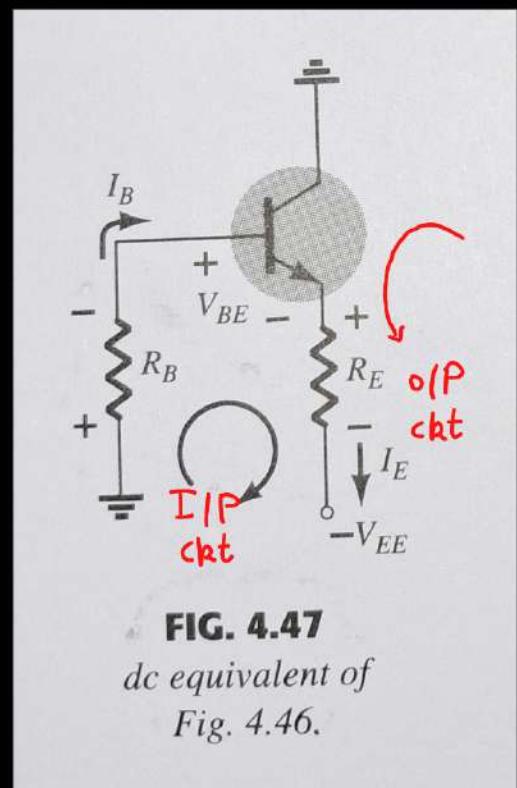


FIG. 4.47  
dc equivalent of Fig. 4.46.

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$I_B$  only  
 $\downarrow$   
 $I_C$  is grounded

Applying KVL to O/P loop:-

$$-V_{CE} - I_E R_E + V_{EE} = 0$$

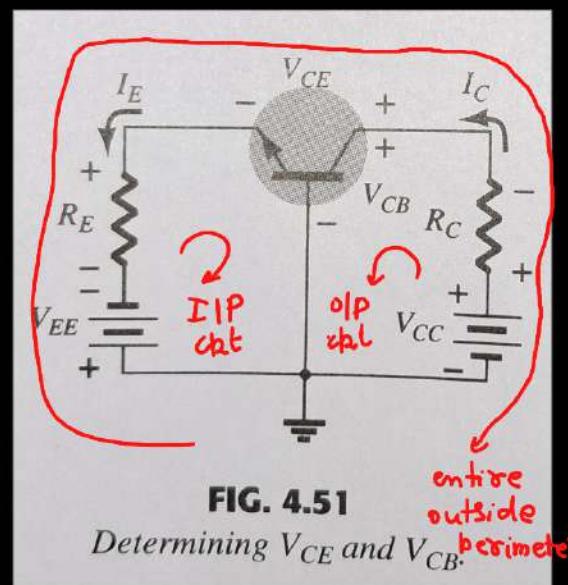
$$\{ V_{CE} = V_{EE} - I_E R_E \}$$

### # Common-Base Configuration :-

Applying KVL in I/P loop:-

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

$$\{ I_E = \frac{V_{EE} - V_{BE}}{R_E} \}$$



Applying KVL in entire outside perimeter

$$-V_{EE} + I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{EE} + V_{CC} - I_E R_E - I_C R_C$$

WKT,  $I_E \approx I_C$

$$\Rightarrow V_{CE} = V_{EE} + V_{CC} - I_E (R_C + R_E)$$

Applying KVL in O/P loop:-

$$V_{CB} + I_C R_C - V_{CC} = 0$$

$$V_{CB} = V_{CC} - I_C R_C$$

## # Thermal Runaway in Transistors :-

Consider CE config of transistor. Reverse saturation current

$$\text{Eqn of } I_c \Rightarrow I_c = \beta I_B + (\beta + 1) I_{c0}$$

$I_{c0} \Rightarrow$  Depends on minority charge carriers

P-type      N-type      } Depends on Temp  
 $e^-$                   holes

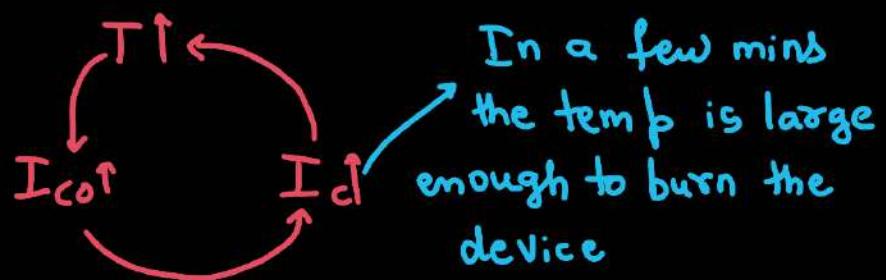
$T \uparrow \Rightarrow$  Conc. of Min. c.c.  $\uparrow \Rightarrow I_{c0} \uparrow \Rightarrow I_c \uparrow$

$T \Rightarrow I_c \uparrow (I_c \propto T)$

This causes thermal runaway  
 Not good ☹

$I_{c0}$  doubles with every  $10^\circ\text{C} \uparrow$  in Temp

$\rightarrow$  Flow of  $I_c \rightarrow$  produces heat  $\rightarrow$  Temp  $\uparrow \Rightarrow I_c \uparrow$



Def of Thermal Runaway: The self destruction of unstabilized transistor is known as thermal runaway

## \* Mitigation of Thermal Runaway :-

### 1) Introduction of negative feedback

$$\text{i) } I_c \uparrow \xrightarrow{\text{Due to } R_E} I_B \downarrow = I_c \downarrow$$

### ii) Using Heat sinks

## # Bias Stabilization:-

→ After setting Q-pt we don't want it to change.

→ Process of making Q-pt independent of temp. changes & variations in transistor parameters.

## \* Causes of Unstabilization :-

→ Q-pt shifts  $\rightarrow I_c \uparrow \downarrow$

$$\text{i) Change in } \underline{\beta} \rightarrow I_c = \underline{\beta} I_B + (\underline{\beta} + 1) I_{cB0}$$

↓  
By replacing the  
transistor,  $\beta$  changed

$$\text{ii) Change in } T \rightarrow T \uparrow \rightarrow I_{cB0} \uparrow (10^\circ C \uparrow T \rightarrow I_{cB0} \times 2)$$

↓  
 $V_{BE} (\downarrow \text{ by } 2.5 \text{ mV}/^\circ C \uparrow T)$

$$I/P_C \quad I/P_V$$

$$I_B \longrightarrow V_{BE}$$

## # Stability factors:-

There are three stability factors:-

$S(I_{CO})$ ,  $S(V_{BE})$ ,  $S(\beta)$ . Each of these are defined as follows:-

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

Networks that are quite stable & relatively insensitive to temperature variations have low stability factors.

↳ i.e. a change in  $I_{CO}$  fails to produce a significant change in  $I_C$ .

## \* Fixed Bias Configuration

→ The three stability factors are

$$S(I_{CO}) = \approx \beta ; S(V_{BE}) \approx -\frac{\beta}{R_B} ; S(\beta) = \frac{I_{C1}}{\beta_1}$$

## \* Emitter-Bias Configuration

→ The three stability factors are

$$S(I_C) \approx \frac{\beta}{\beta + R_B/R_E} \left( 1 + \frac{R_B/R_E}{R_E} \right) ; S(V_{BE}) = \frac{-\beta/R_E}{\beta + R_B/R_E} ; S(\beta) = \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(\beta_2 + R_B/R_E)}$$

The notation  $I_{C_1}$  and  $\beta_1$  is used to define their values under one set of network conditions, whereas the notation  $\beta_2$  is used to define the new value of beta as established by such causes as temperature change, variation in  $\beta$  for the same transistor, or a change in transistors.

## \* Voltage-Divider Bias

→ The three stability factors are

$$S(I_C) \approx \frac{\beta}{\beta + R_{Th}/R_E} \left( 1 + \frac{R_{Th}/R_E}{R_E} \right) ; S(V_{BE}) = \frac{-\beta/R_E}{\beta + R_{Th}/R_E} ; S(\beta) = \frac{I_{C_1}(1 + R_{Th}/R_E)}{\beta_1(\beta_2 + R_{Th}/R_E)}$$

## \* Feedback-Bias Configuration ( $R_E = 0 \Omega$ )

→ The three stability factors are

$$S(I_C) = \frac{\beta}{\beta + R_B/R_C} ; S(V_{BE}) = \frac{-\beta/R_C}{\beta + R_B/R_C} ; S(\beta) = \frac{I_{C_1}(R_B + R_C)}{\beta_1(R_B + \beta_2 R_C)}$$

## # Small Signal analysis of BJT

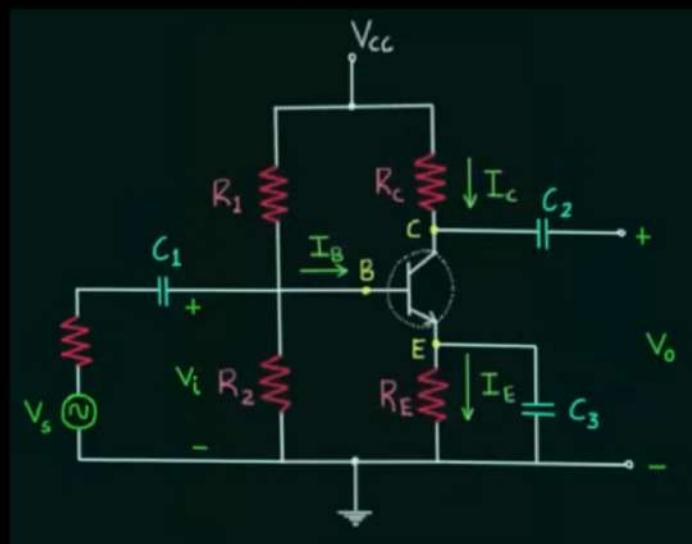
- AC response of transistors
- Transistor Models

$I_C \uparrow = \beta I_B \uparrow \Rightarrow Q - pt$  will also change  
 ↗ not desirable  
 BJT amp ckt

Def :- Signal whose mag. is sufficiently small enough to keep the transistor in active region

Active  $\rightarrow C-B \delta^n$  is R.B  
 Active  $\rightarrow E-B \delta^n$  is F.B

Total response = DC res + AC res



- i)  $R_c$  :- Limit Collector current; Act as load resistor
- ii)  $R_1 \& R_2$  :- AC biasing resistor (Voltage divider bias)
- iii)  $R_E$  :- Emitter resistor used for stabilising Q point
- iv)  $C_1, C_2 & C_3$  :- Coupling Capacitors
- v)  $C_3$  :- Bypass Capacitor

AC response :-

- i) ac equivalent ckt
- ii) replace transistor with eq model / eq ckt

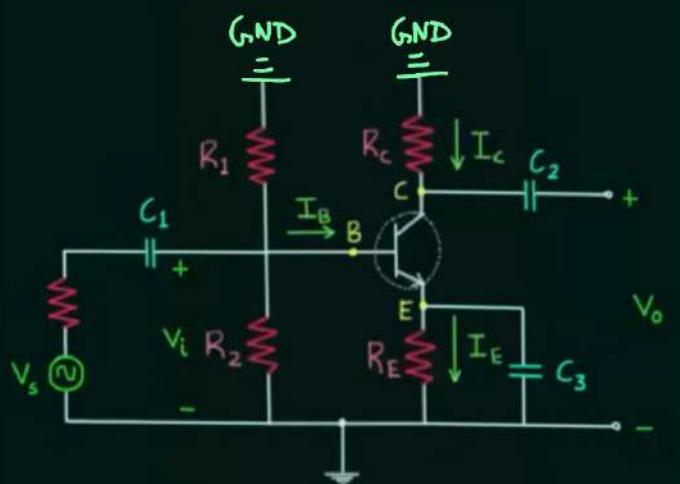
## # AC equivalent Circuit of BJT amplifier :-

Step-1 : Short ckt all the dc sources

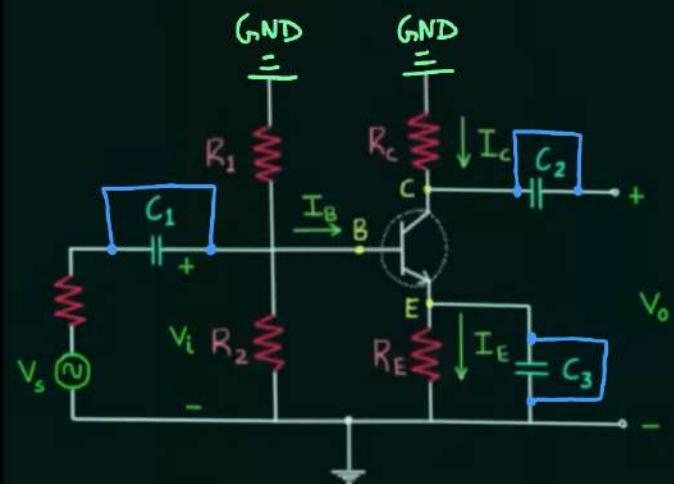
Step-2 : Short all capacitors

Step-3 : Redraw the network removing all elements which are short ckted in step 1 & step 2

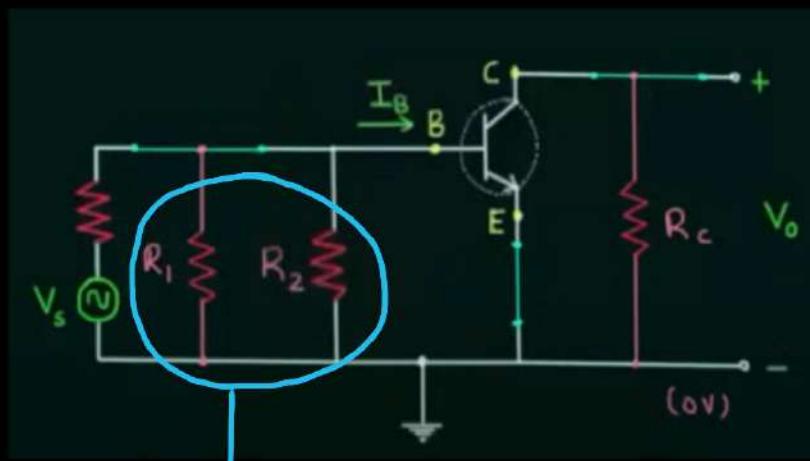
## Step-1



## Step-2



## Step-3



Final  
AC  
equivalent  
circuit for  
BJT  
amplifier

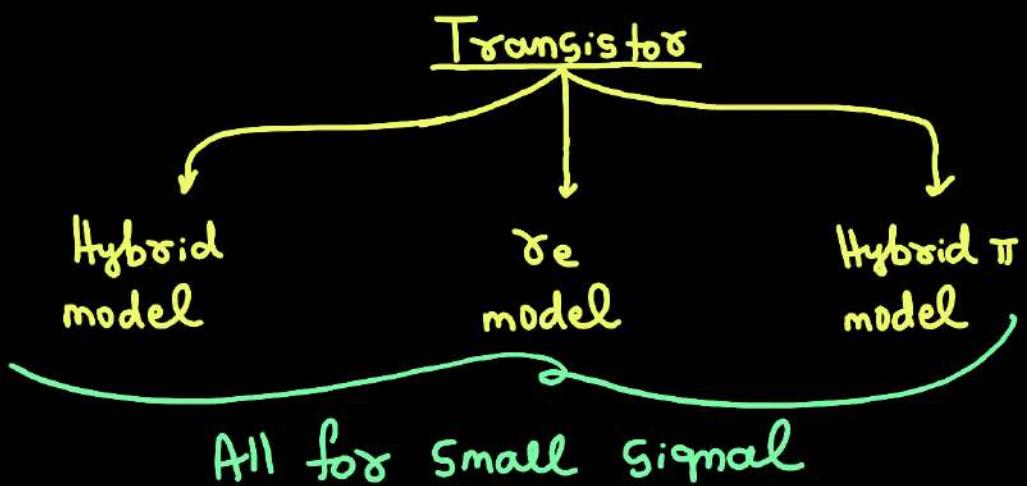
In ||el connection

∴ We can replace them with  $\text{Req} = \frac{R_1 R_2}{R_1 + R_2}$

## \* Equivalent model of the transistor

→ An equivalent model is combination of ckt elements properly chosen to best represent the actual behaviour of device under specific operating point

Network theorems cannot be used directly. Thus we need equivalent model.



# Hybrid model (calculation of h-parameters)

↳ hybrid

→ Equivalent model of transistor

→ Widely used before the popularity of <math>\delta e</math> model

h-model

→ Parameters are defined in general terms for any operating conditions.

→ Parameters are defined by the actual operating conditions.

↑  
<math>\delta e</math>-model

There are 4 Parameters in small signal analysis,

All can be found using Z-parameter or Y-parameter

↳ True only for vacuum

tubes.



We have 4 values      ↗ 2 dependent      |  $V_1 \& I_2 \rightarrow$  dependent  
 ↙ 2 independent      |  $V_2 \& I_1 \rightarrow$  independent

$$V_1 = f_1(I_1, V_2)$$

$$I_2 = f_2(I_1, V_2)$$

$$AC \text{ value } dV_1 = \frac{\partial V_1}{\partial I_1} dI_1 + \frac{\partial V_1}{\partial V_2} dV_2 \rightarrow ①$$

impedance ( $h_{11}$ ) dimensionless ( $h_{12}$ )

$$AC \text{ value } dI_2 = \frac{\partial I_2}{\partial I_1} dI_1 + \frac{\partial I_2}{\partial V_2} dV_2 \rightarrow ②$$

dimensionless ( $h_{21}$ ) admittance ( $h_{22}$ )

Some for other 3

AC current  $\rightarrow i$     AC voltage  $\rightarrow v$      $\left. \begin{array}{l} \text{eqn } ① \& ② \text{ can} \\ \text{be written as} \end{array} \right\}$

$$\begin{aligned} v_1 &= h_{11} i_1 + h_{12} v_2 \rightarrow ③ \\ i_2 &= h_{21} i_1 + h_{22} v_2 \rightarrow ④ \end{aligned} \quad \left. \begin{array}{l} \text{Applicable to all 3} \\ \text{transistor configurations} \end{array} \right\}$$

$\hookrightarrow$  making  $v_2 = 0$ , we can get  $h_{11} \& h_{21}$

from eqn ③

$$\Rightarrow h_{11} = \frac{v_1}{i_1} \Big|_{v_2=0} \quad \Rightarrow h_{11} = h_{11} = \frac{v_1}{i_1} \Big|_{v_2=0}$$

$\uparrow$   
input impedance  
when o/p is  
short ckted

Capacitor is connected in parallel to short circuit of terminal, because reactance offered by capacitor is zero in case of ac signals.

From eqn ④

$$h_f = h_{21} = \frac{i_2}{i_1} \Big|_{v_2=0} \rightarrow \text{Forward current gain when o/p is short ckted}$$

Making  $i_1 = 0$ , we get

from eq<sup>n</sup> ③

$$h_{12} = h_{21} = \left. \frac{V_1}{V_2} \right|_{i_1=0} \rightarrow \text{reverse voltage gain when } o/p \text{ is open ckted}$$

Inductor is connected in series to open circuit i/p terminal,  
because reactance offered by inductor is  $\infty$  in case of AC  
signals

From eq<sup>n</sup> ④

$$h_0 = h_{22} = \left. \frac{i_2}{V_2} \right|_{i_1=0} \rightarrow o/p \text{ admittance with } i/p \text{ open ckted}$$

### # Nomenclature of h-parameters :-

Double Subscript nomenclature

$h_{11}, h_{22}$

denotes nature of parameter      denotes the transistor configuration.

Already covered in PoE, bg

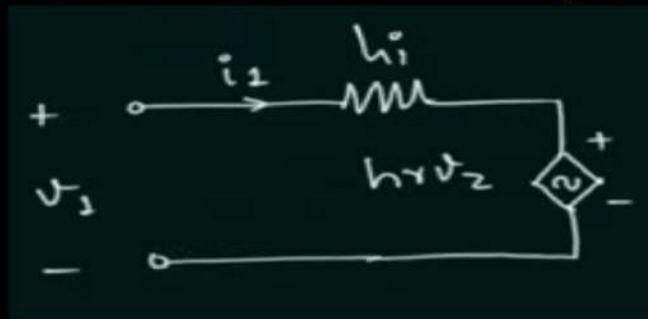
### # Equivalent ckt for hybrid model :-

$$\begin{aligned} V_1 &= h_{11}i_1 + h_{12}V_2 \rightarrow ① \Rightarrow V_1 = h_{11}i_1 + h_{12}V_2 \rightarrow ③ \quad (\text{KVL}) \\ i_2 &= h_{21}i_1 + h_{22}V_2 \rightarrow ② \Rightarrow i_2 = h_{21}i_1 + h_{22}V_2 \rightarrow ④ \quad (\text{KCL}) \end{aligned}$$

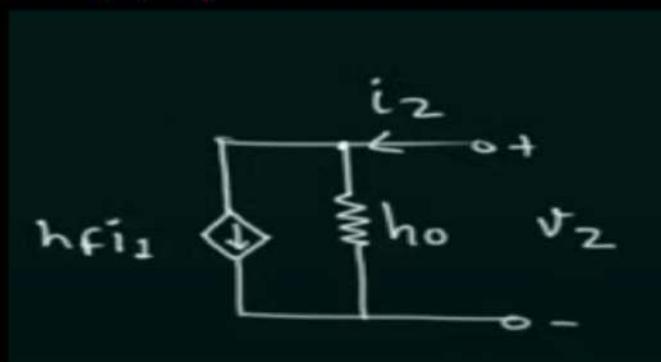
(V) (V) (V)  $\rightarrow$  units  
(A) (A) (A)  $\rightarrow$  units

For eq<sup>n</sup> ③ & ④, we draw eq<sub>1</sub>. ckt

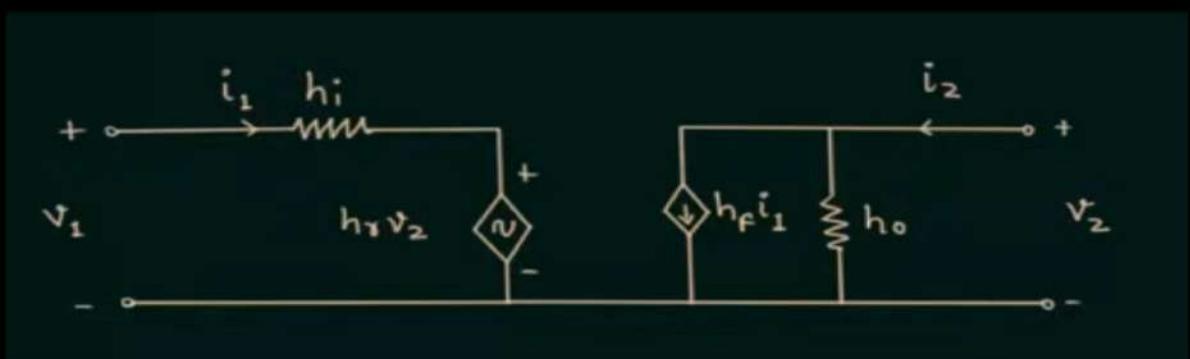
From eqn ③, we get:  $i_1 - h_{ie} i_1 - h_{ov} v_2 = 0$  (From KVL)

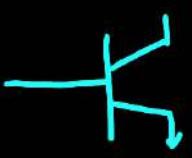


From eqn ④:- Applying KCL



Final equivalent circuit :-

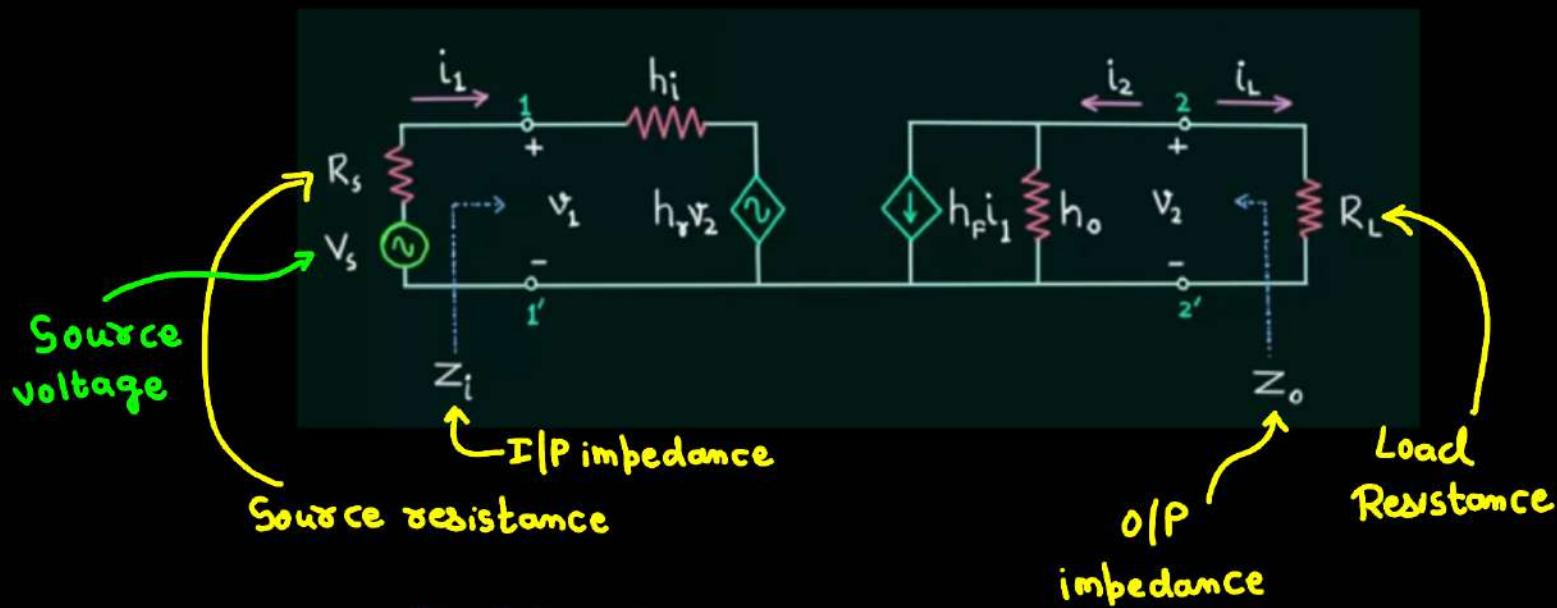


The transistor  gets replaced by the above circuit in AC analysis

The h-parameters will have to be named accordingly.

We now perform analysis of amplifier using h-parameters

## # Analysis of Transistor Amplifier using h-parameter :-



We now find the following:-

- Current Gain
- Voltage Gain
- Power Gain

\* Current Gain expression :- ( $A_i$ )

$$A_i = \frac{\text{O/P current}}{\text{I/P current}} = \frac{i_L}{i_1} = -\frac{i_2}{i_1}$$

Voltage drop  $\rightarrow V_2 = i_L R_L = -i_2 R_L$

From h-parameter eqn ④

$$\Rightarrow i_2 = h_f i_1 + h_o (-i_2 R_L)$$

$$i_2 + h_o i_2 R_L = h_f i_1$$

$$\Rightarrow i_2 = \frac{h_f i_1}{1 + h_o R_L} \Rightarrow \frac{i_2}{i_1} = \frac{h_f}{1 + h_o R_L}$$

$$A_i = \frac{-i_2}{i_1} = \frac{-h_f}{1+h_o R_L} \rightarrow \text{Current Gain}$$

\* Voltage Gain expression ( $A_v$ ) :-

$$A_v = \frac{\text{O/P voltage}}{\text{I/P voltage}} = \frac{V_2}{V_1} = \frac{-i_2 R_L}{V_1}$$

$$A_i = -i_2 / i_1 \Rightarrow -i_2 = i_2 A_i$$

$$\Rightarrow A_v = \frac{i_2 A_i R_L}{V_2} \Rightarrow A_v = \frac{A_i R_L}{Z_i} \rightarrow \textcircled{1}$$

Expression for  $Z_i = h_i - \frac{h_{\alpha} h_f}{\frac{1}{R_L} + h_o}$  →  $\textcircled{2}$  Derived later

WKT,  $A_i = \frac{-h_f}{1+h_o R_L} \rightarrow \textcircled{3}$

Put  $\textcircled{2}$  &  $\textcircled{3}$  in  $\textcircled{1}$ , we get after simplification

$$A_v = \frac{-h_f R_L}{h_i + \frac{(h_i h_o - h_{\alpha} h_f)}{\Delta h} R_L} \Rightarrow A_v = \frac{-h_f R_L}{h_i + \Delta h R_L} \rightarrow \text{True for all config}$$

\* Power Gain expression ( $A_p$ ) :-

$$A_p = A_v \times A_i = \frac{-h_f R_L}{h_i + \Delta h R_L} \times \frac{-h_f}{1+h_o R_L} =$$

$$A_p = \frac{h_f^2 R_L}{(h_i + \Delta h R_L)(1+h_o R_L)}$$

## \* Expression for I/P impedance :-

From Ohm's law:-

$$V_1 = i_2 \times Z_i \Rightarrow Z_i = \frac{V_1}{i_2}$$

We know from h-parameter eqn ③, ④ :-

$$V_1 = h_i i_2 + h_{\infty} \overbrace{(-i_2 R_L)}^{pV_2}$$

$$\Rightarrow \frac{V_1}{i_2} = h_i - \frac{h_{\infty} i_2 R_L}{i_2} \Rightarrow \frac{V_1}{i_2} = h_i + h_{\infty} A_i R_L$$

$$\frac{V_1}{i_2} = Z_i = h_i + h_{\infty} \left( \frac{-h_f}{1 + h_o R_L} \right) R_L$$

Simplifying:-

$$\Rightarrow Z_i = h_i - \frac{h_{\infty} h_f}{\frac{1}{R_L} + h_o}$$

## \* O/P Impedance expression :-

We need to short ckt source voltage & open ckt o/p terminal

$$V_s = 0$$

$$R_L = \infty$$

Redraw the ckt in exam

O/P impedance:-

$$Z_o = \frac{V_2}{i_2} \quad \left| \begin{array}{l} \text{From h-para eqn } ③ \\ i_2 = h_f i_1 + h_o V_2 \end{array} \right.$$

$$Z_o = \frac{V_2}{h_f i_1 + h_o V_2} \rightarrow ①$$

## Applying KVL in I/P loop :-

$$-i_1 R_s - i_1 h_i - h_\pi V_2 = 0$$

$$\Rightarrow i_1 (R_s + h_i) + h_\pi V_2 = 0$$

$$i_1 = \frac{-h_\pi V_2}{R_s + h_i} \rightarrow \text{Put in } ①$$

$$\Rightarrow Z_o = \frac{V_2}{h_f \left( \frac{-h_\pi V_2}{R_s + h_i} \right) + h_o V_2}$$

After simplifying

$$\Rightarrow Z_o = \frac{R_s + h_i}{\frac{(h_o h_i - h_f h_\pi) + h_o R_s}{\Delta h}} \Rightarrow Z_o = \frac{R_s + h_i}{\Delta h + h_o R_s}$$

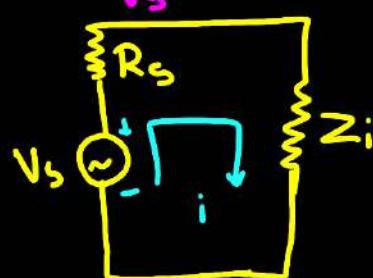
## Overall voltage gain :- ( $A_{VS}$ )

$$A_{VS} = \frac{\text{O/P voltage}}{\text{Source voltage}} = \frac{V_2}{V_s} \Rightarrow A_{VS} = \frac{V_1 \cdot V_2}{V_s}$$

$$= \frac{V_2 \cdot V_1}{V_1 \cdot V_s} \Rightarrow A_{VS} = \frac{A_V \cdot V_1}{V_s}$$

Can remember this form  $\rightarrow ①$

We now find  $\frac{V_1}{V_s}$ . Redrawing the ckt



$$\Rightarrow \text{KVL: } V_s - i R_s - i Z_i = 0$$

$$\Rightarrow i = \frac{V_s}{R_s + Z_i}$$

$$V_1 = iZ_i$$

$$V_1 = \frac{Z_i V_s}{R_s + Z_i} \Rightarrow \left\{ \frac{V_1}{V_s} = \frac{Z_i}{R_s + Z_i} \right\} \quad \textcircled{2}$$

Put  $\textcircled{2}$  in  $\textcircled{1}$

$$\Rightarrow A_{VS} = \frac{A_V \cdot Z_i}{R_s + Z_i}$$

Overall  
Voltage gain

$\Rightarrow R_s = 0 \Rightarrow \text{Ideal } V_s$

$\Rightarrow A_{VS} = A_V$  Important

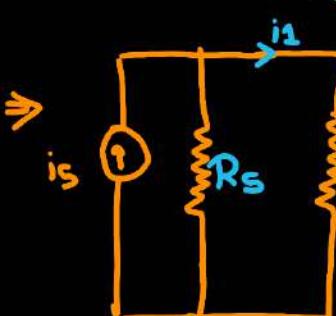
$\star$  Expression for overall current gain ( $A_{IS}$ ) :-

$$A_{IS} = \frac{i_L}{i_S} = \frac{i_L \cdot i_2}{i_S \cdot i_2} \Rightarrow A_{IS} = \frac{i_L \times i_2}{i_2 \times i_S}$$

Load current  
 $i_L$   
Current delivered by source  $i_S$

$$\Rightarrow A_{IS} = \frac{-i_2 \cdot i_L}{i_2 \cdot i_S} \quad \textcircled{1}$$

Can remember this form

$$\Rightarrow A_{IS} = A_i \cdot \frac{i_2}{i_S}$$


From current divider rule

$$i_1 = \frac{i_S R_s}{R_s + Z_i}$$

$$\frac{i_2}{i_S} = \frac{R_s}{R_s + Z_i} \quad \textcircled{2}$$

Put  $\textcircled{2}$  in  $\textcircled{1}$  we get :-

$$A_{IS} = A_i \left( \frac{R_s}{R_s + Z_i} \right)$$

Overall current gain

$\text{Ideal } V_s \Rightarrow R_s = \infty \Rightarrow A_{IS} = A_i$

Important

## \* Proof for $\Delta h = h_i h_o - h_f h_r$ :-

From h-parameter eqn's :-

$$\begin{bmatrix} V_1 \\ i_2 \end{bmatrix}_{2 \times 1} = \begin{bmatrix} h_i & h_r \\ h_f & h_o \end{bmatrix}_{2 \times 2} \times \begin{bmatrix} V_2 \\ i_2 \end{bmatrix}_{2 \times 1}$$

Representing the eqn's in matrix form

both are independent variables

both are dependent variables

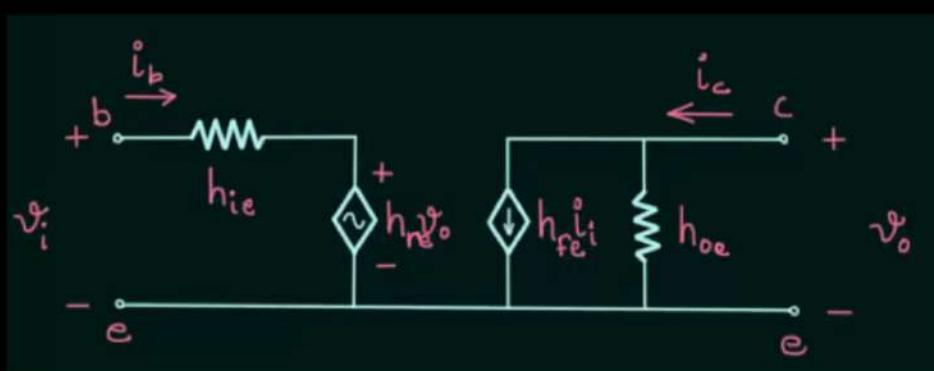
$$\Delta h = |h| = h_i h_o - h_f h_r \quad (\because \Delta h = |h|)$$

Hence proved

## # Approximate Hybrid equivalent model :-

↳ Simplified hybrid equivalent model

## Ckt modified for CE transistor :-



For CE & CB the magnitude of  $h_r$  and  $h_o$  are such that the results obtained for the parameters are slightly affected.

$\frac{1}{h_o} \rightarrow 0$  /  $\infty$  impedance  $\Rightarrow$  very large  $\Rightarrow$  can be neglected  
 Compare  $\frac{1}{h_o}$  to  $R_L \Rightarrow \frac{1}{h_o} \gg R_L$

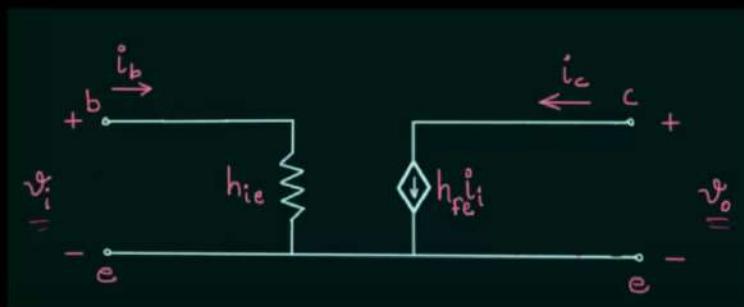


$$h_{re} = \frac{V_i}{V_o} \approx 0$$

$V_o \rightarrow$  very large } Ckt above is used for  
compared to  $V_i$  } amplification purposes

here  $V_o$  is replaced by short ckt

Approximate hybrid equivalent model then becomes:-



Make it similar to CCCS CB

# Conversion of h-parameters:

CE config

$h_{ie}$   
 $h_{re}$   
 $h_{fe}$   
 $h_{oe}$ 
}  $\Rightarrow$  Convert these to parameters  
in case of CB, then later  
to CC

Why need for conversion:- Manufacturers give only for CE, but we need for CB & CC as well

CE  $\rightarrow$  CB :-

$$\star h_{ib} = \frac{h_{ie}}{1 + h_{fe}} \quad \star h_{eb} = \frac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}$$

$$\star h_{fb} = \frac{-h_{fe}}{1 + h_{fe}} \quad \star h_{ob} = \frac{h_{oe}}{1 + h_{fe}}$$

### CE $\rightarrow$ CC :-

$$\star h_{ie} = h_{re} \quad \star h_{rc} = 1 - h_{re}$$

$$\star h_{fe} = - (1/h_{re}) \quad \star h_{oc} = h_{re}$$

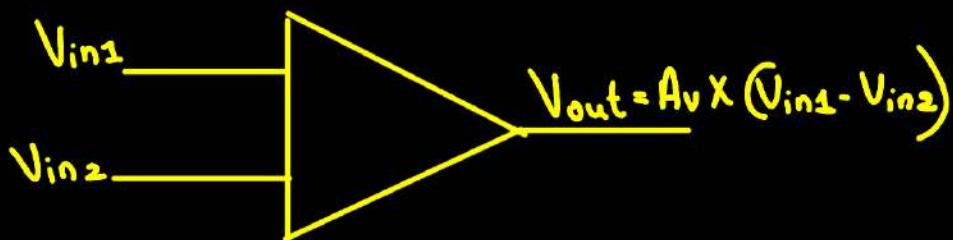
### CB $\rightarrow$ CC :-

$$\star h_{ie} = \frac{h_{ib}}{1 + h_{fb}} \quad \star h_{re} = \frac{h_{ib} h_{fb}}{1 + h_{fb}} - h_{re}$$

$$\star h_{fe} = \frac{-h_{fb}}{1 + h_{fb}} \quad \star h_{oc} = \frac{h_{fb}}{1 + h_{fb}}$$

### # Differential Amplifiers :-

- Amplifies the difference b/w the i/p signals
- Widely used in ICs
- First stage of Op-Amp



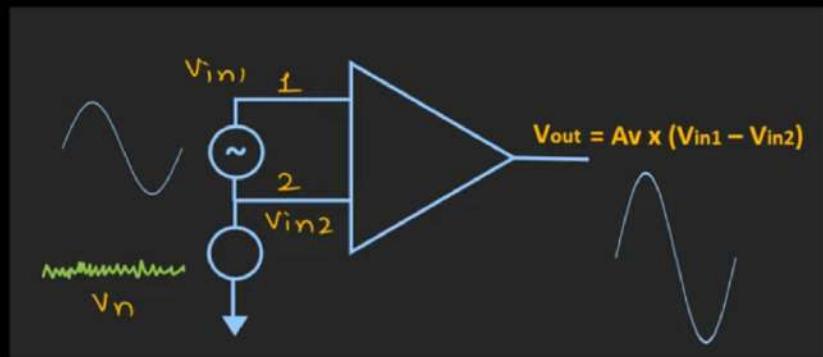
### \* Difference b/w the single ended & differential input :-

→ All BJT amplifiers are single ended amplifiers

↳ Single ended amplifier → the i/p & o/p is measured w.r.t ground

→ When noise gets coupled with i/p → it will also get amplified

→ Common Mode noise can be removed in diff amplifiers



$$\begin{aligned}V_{in1} &= V_{in1} + V_n \\V_{in2} &= V_{in2} + V_n\end{aligned}$$

$$V_d = V_{in1} - V_{in2} = V_{in1} - V_{in2}$$

Noise won't appear  
in o/p side

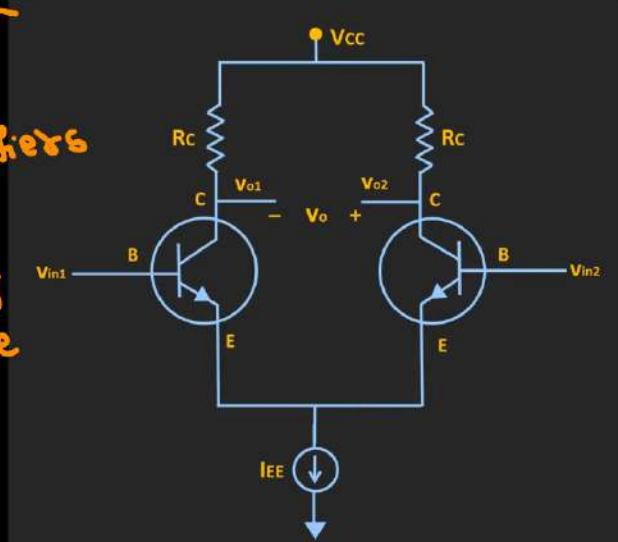
Advantage

\* Take o/p in differential configuration → possible to eliminate supply hum / any noise common to the amplifier ckt

\* When diff amplifiers are cascaded together, then the need for coupling capacitors is eliminated → which is used in single ended amplifiers.

\* Ckt diagram :- Pair of BJT amplifiers

The two BJTs must be perfectly matched for full elimination of noise



## \* DC analysis :-

### KVL:-

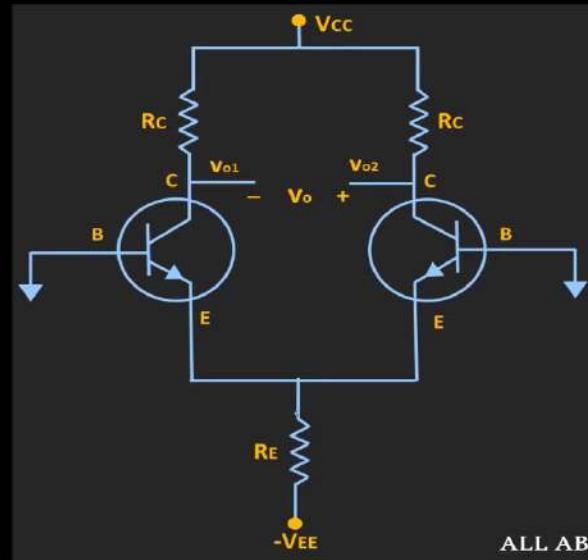
$$-V_{BE} - I_{EE} R_E + V_{EE} = 0$$

$$\Rightarrow I_{EE} = \frac{V_{EE} - V_{BE}}{R_E}$$

$$I_{E1} = I_{E2} = \frac{I_{EE}}{2}$$

$$I_C \approx I_E$$

$$\Rightarrow I_{C1} = I_{C2} = \alpha \frac{I_{EE}}{2}$$



ALL ABOUT

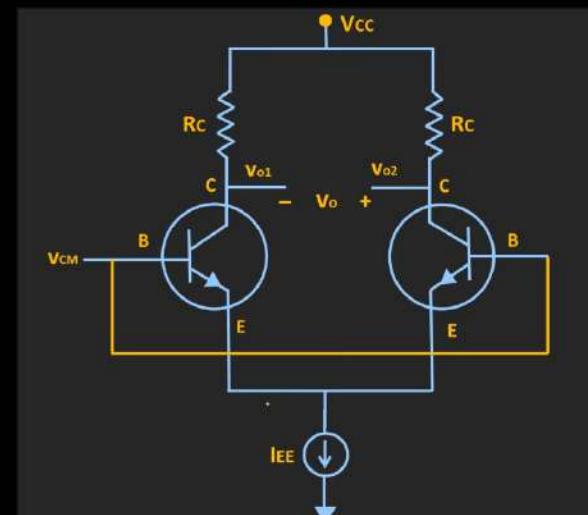
$$\begin{aligned} V_C &= V_{CC} - I_C R_C \\ &= V_{CC} - \alpha \frac{I_{EE}}{2} \cdot R_C \end{aligned}$$

## \* Response of Diff Amplifier to common mode if (Quantitative analysis) :-

Since the transistors are perfectly matched, the voltage drop across the collectors are same i.e:-

$$V_{o1} = V_{o2} = V_{CC} - \alpha \frac{I_{EE}}{2} \cdot R_C$$

$$\therefore V_{o1} - V_{o2} = 0$$



## ★ Response of Diff Amplifier to differential i/p (Quantitative analysis):

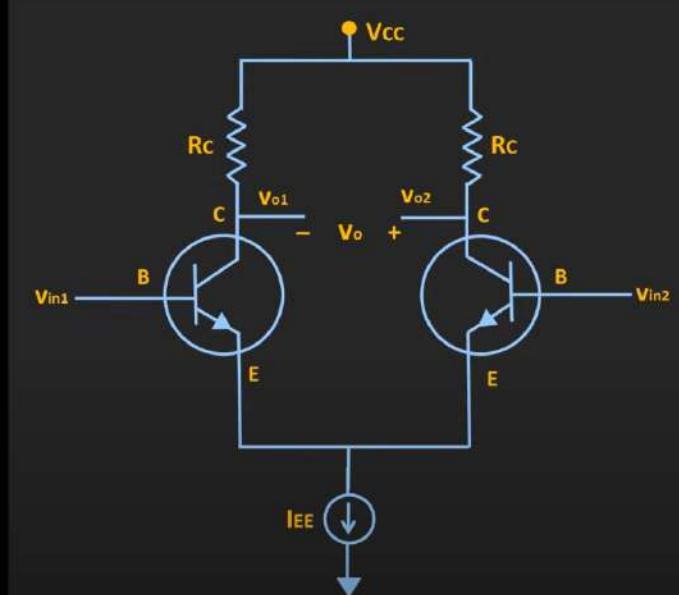
If  $V_{CM} = 1V$

If 1V is added to  $V_{in1}$

$$\Rightarrow V_{in1} = 2V$$

We can now say that, a 1V of differential i/p is present.

$\because$  1V being very large, trans  $Q_1$  draws all current  $I_E$



At that point,  $Q_2$  is off

The reverse is also true!!

$Q_1 \rightarrow ON ; Q_2 \rightarrow OFF$

$$V_{C1} = V_{CC} - \alpha I_{EE} R_C$$

$$V_{C2} = V_{CC}$$

$Q_1 \rightarrow OFF ; Q_2 \rightarrow ON$

$$V_{C1} = V_{CC}$$

$$V_{C2} = V_{CC} - \alpha I_{EE} R_E$$

★ Due to this current steering property of differential amplifier it is widely used in Emitter Coupled Logic (ECL) circuits.

→ To use this differential pair as an amplifier, the diff i/p voltage must be very small

Typically less than  $2V_T$        $\xrightarrow{\text{Thermal voltage}} \approx 25mV @ \text{room temp}$