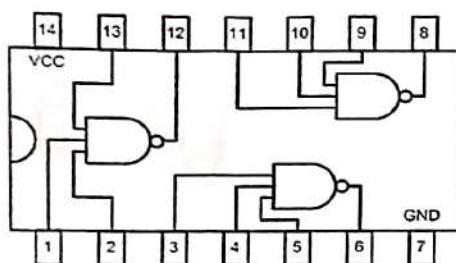
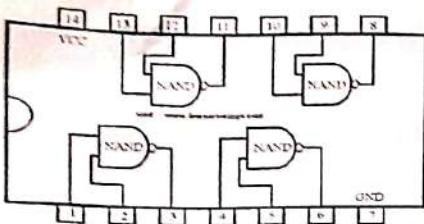
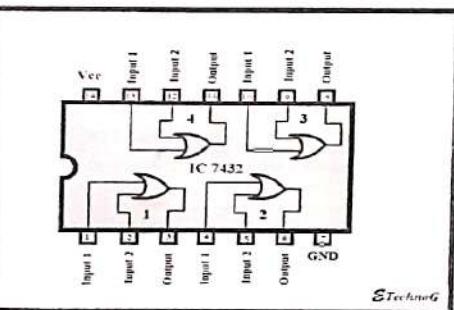


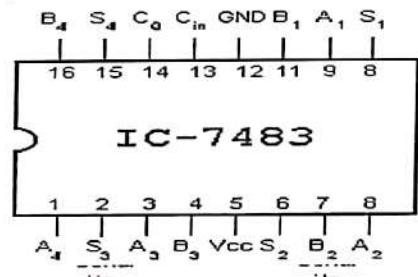
Pinout Diagram of 74HC00 / 74HCT00, Quad 2-Input TTL NAND Gate



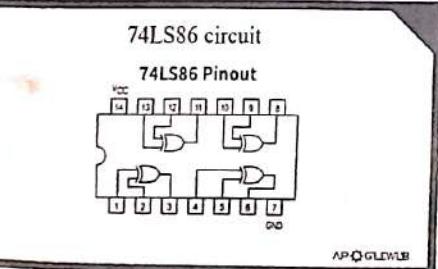
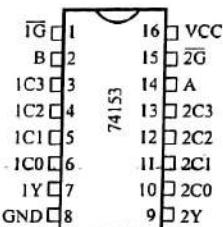
7410-Triple 3-Input-NAND



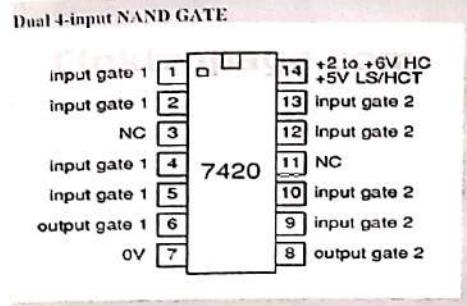
ETechnoG



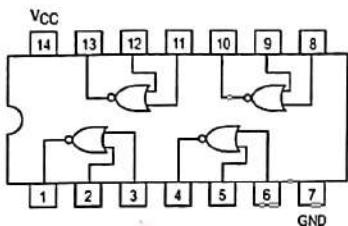
74153, 74L153, 74F153, 74ALSI53, 74LS153, 74S153, 74HC153 双 4 选 1 数据选择器



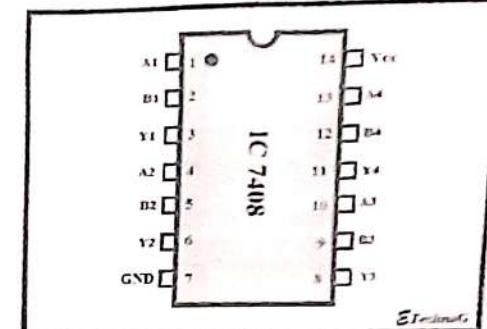
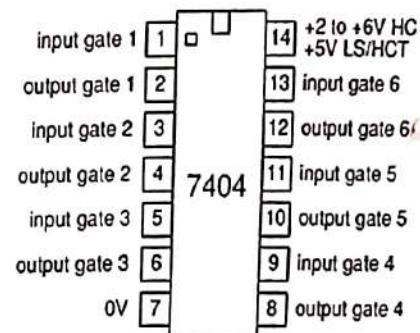
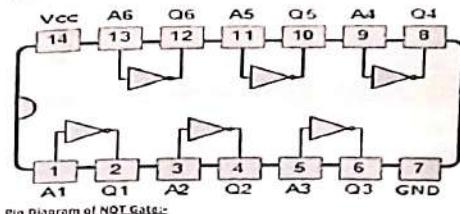
APQ GLOWIE



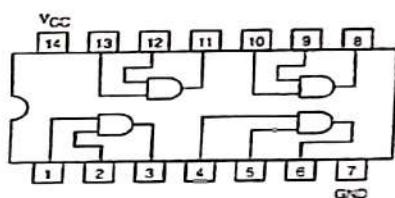
74LS02 – Quadruple Two Input NOR Gate IC



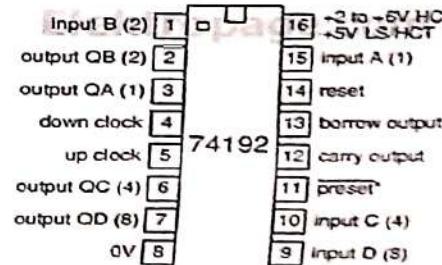
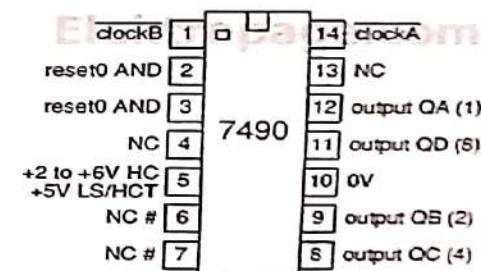
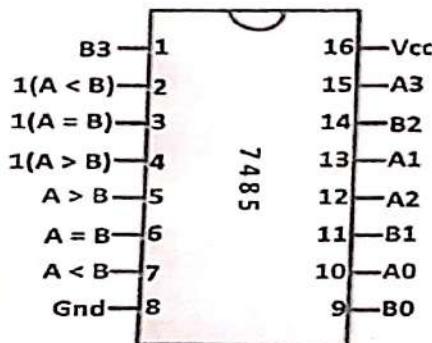
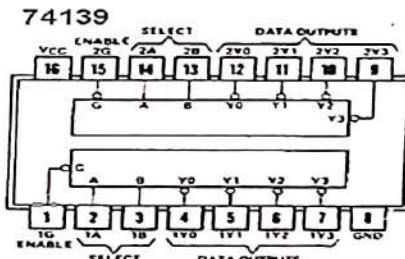
Control 7404, NOT Gate IC



7408 AND Gate IC



clock
① BN-Big former -no
②



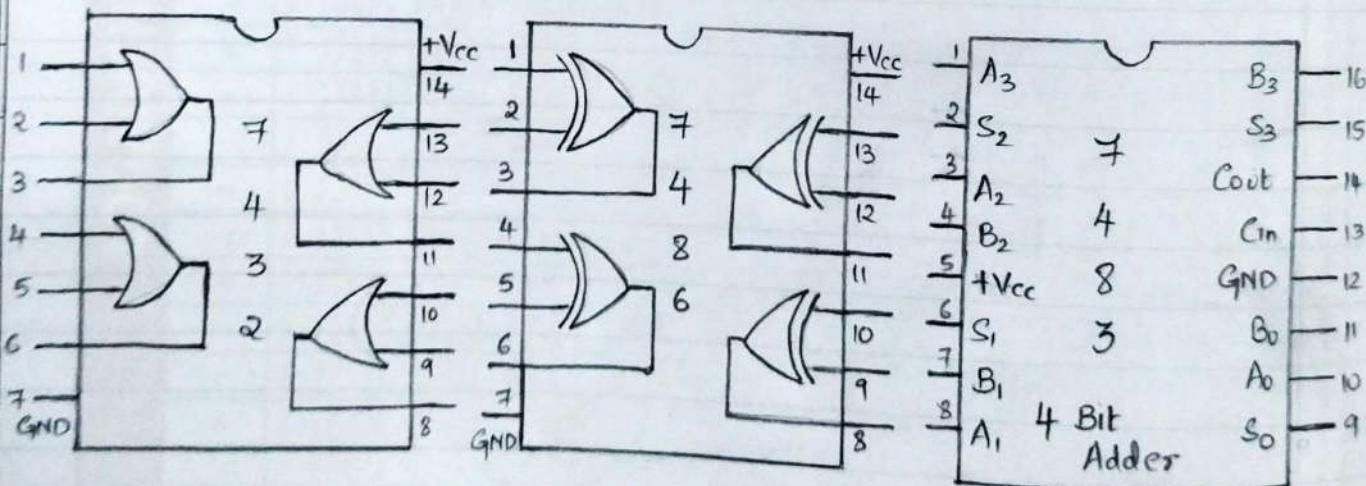
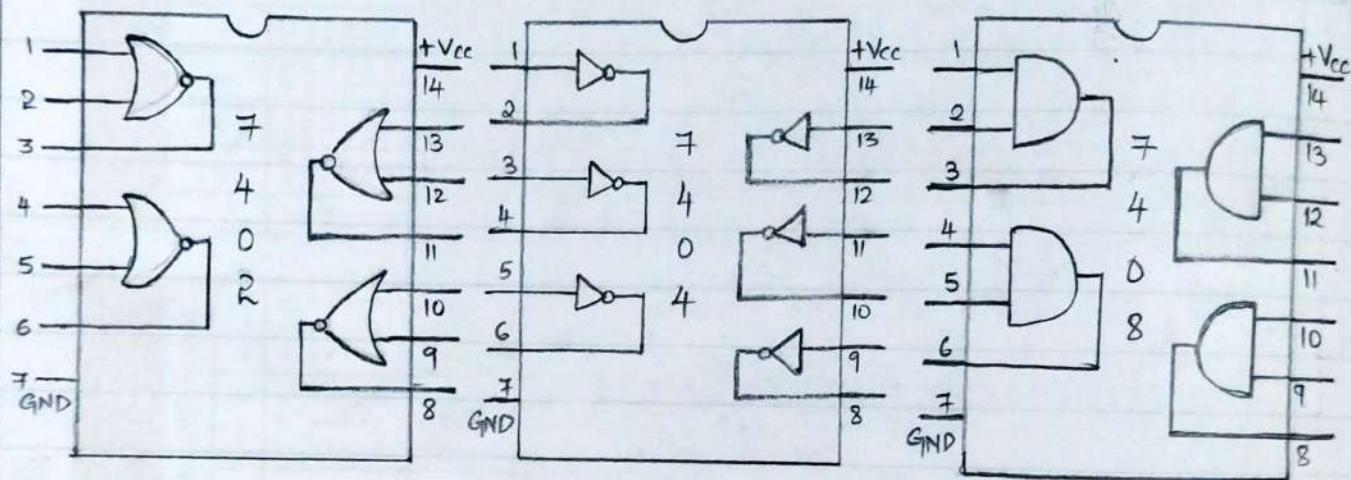
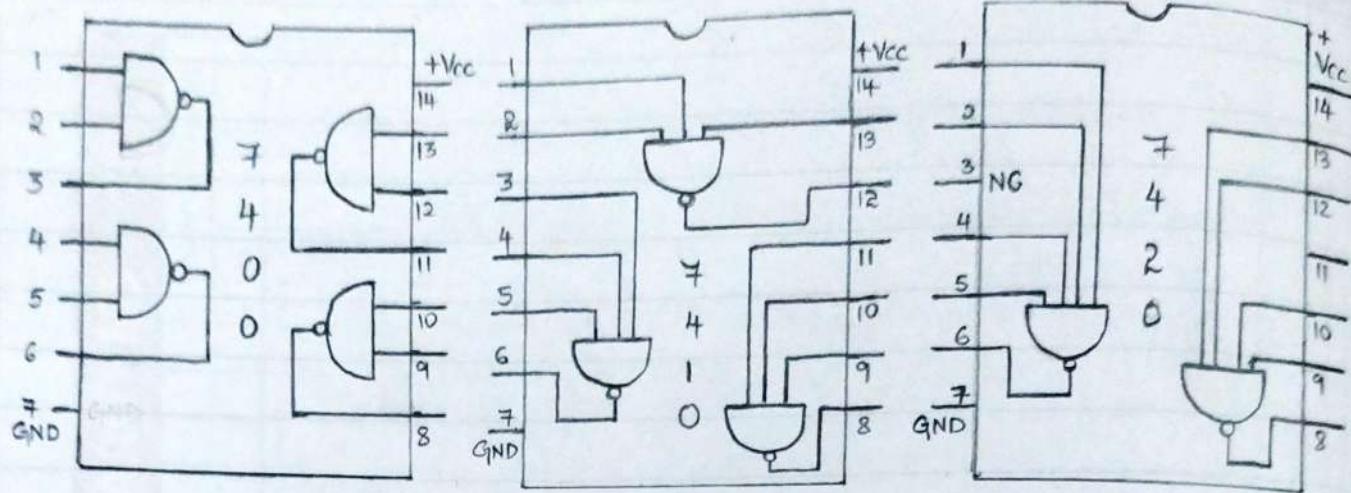
INDEX

Name Sharvari Bagade Class 2nd year Year ECE B.

Expt. No.	Date	Title of the Experiments	Page No.	Date of Submission	Remarks
1.	6/3/23	Realisation of Half Adder & Full adder. using gates	3.	13/3/23	
2.	6/3/23	Realisation of Half Subtractor & Full subtractor	4.	13/3/23	
3.	13/3/23	4 bit adder & Subtractor	5	20/3/23	
4.	13/3/23	Multiplexer.	6	20/3/23	
5.	20/3/23	Demultiplexer	7	27/3/23	
6.	20/3/23	Comparator (2 bit)	23.	27/3/23	8
7.	27/3/23	Flip Flop.	8	3/4/23	
8.	3/4/23	Counters	10	17/4/23	
9.	17/4/23	Shift Registers	12.	8/5/23	
10.	8/5/23	Inverter, Non Inverter, Follower Voltage.	15.	15/5/23	
11.	15/5/23	Astable Multivibrator using Opamp.	14.	22/5/23	

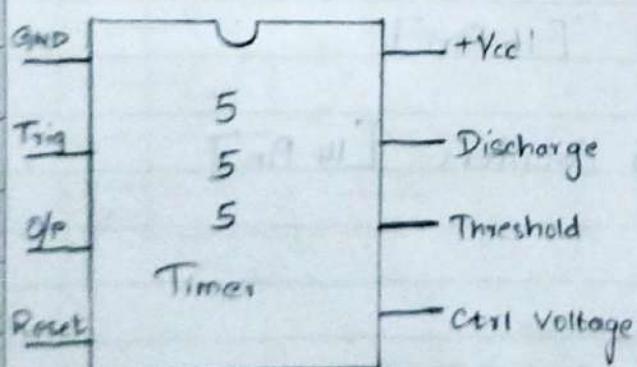
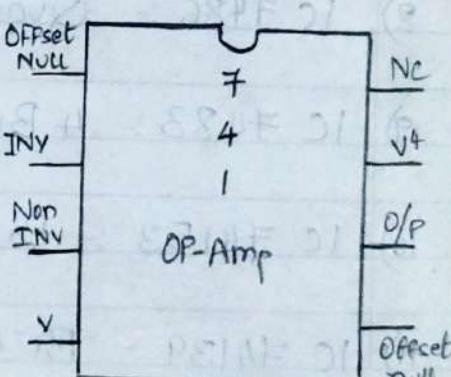
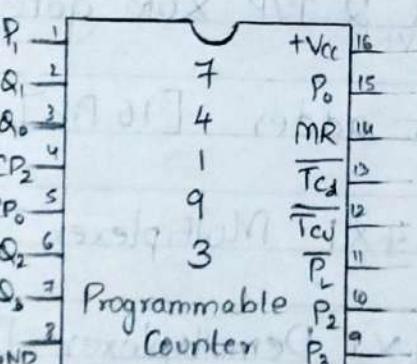
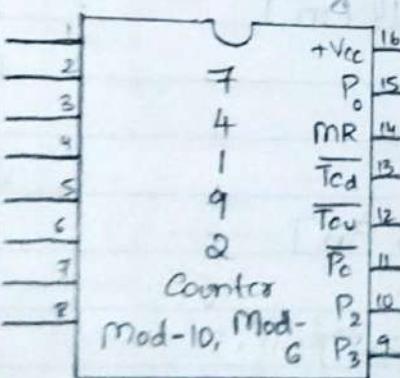
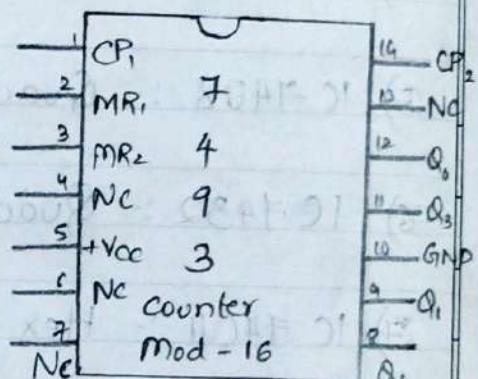
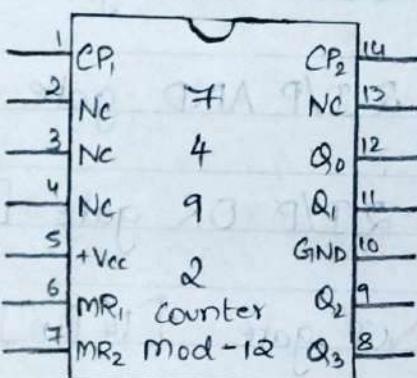
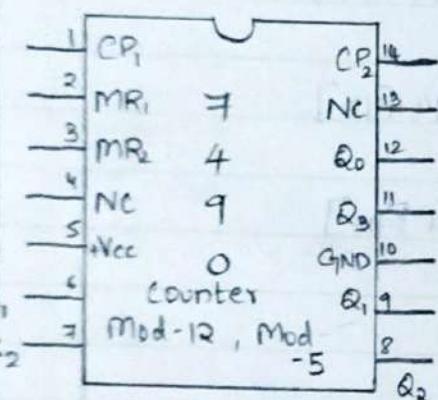
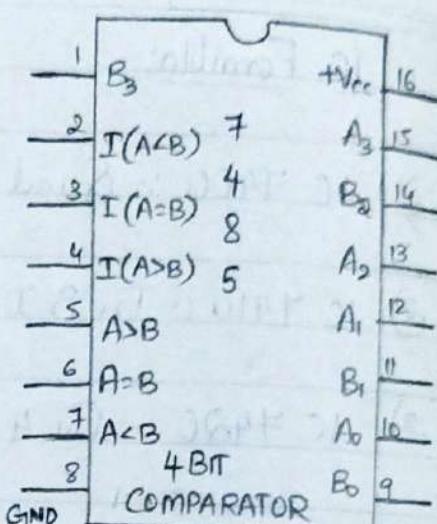
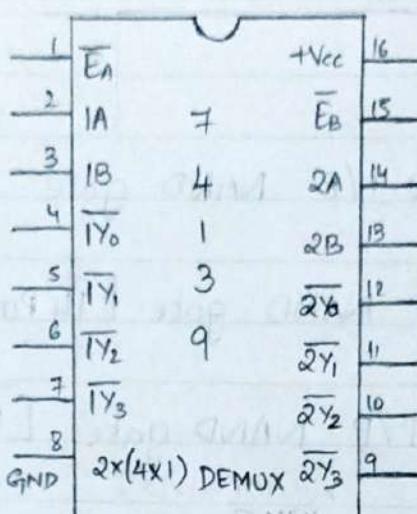
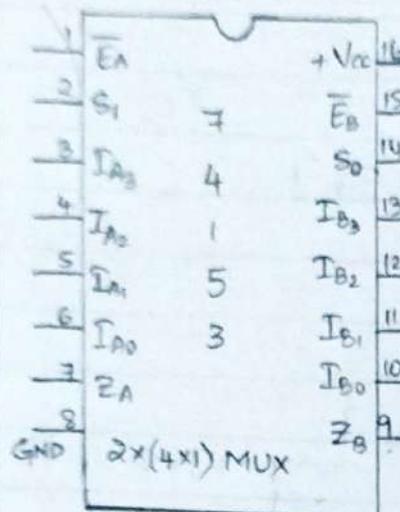
INDEX

Name Class Year



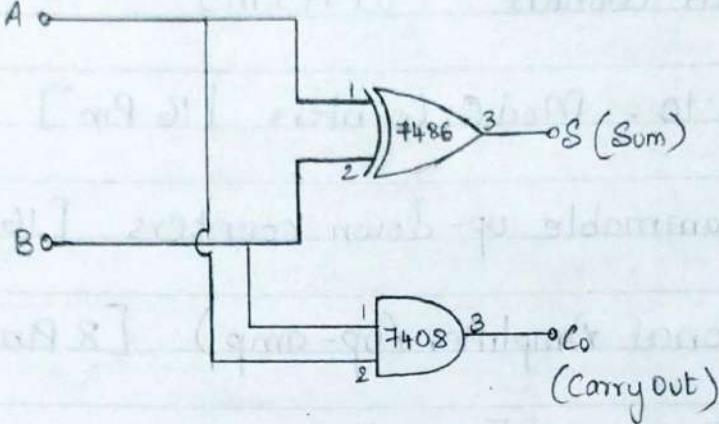
IC Families

- 1) IC 7400 :- Quad 2 I/P NAND gate [14 Pin]
- 2) IC 7410 :- Tri 3 I/P NAND gate [14 Pin]
- 3) IC 7420 :- Bi 4 I/P NAND gate [14 Pin]
- 4) IC 7402 :- Quad 2 I/P NOR gate [14 Pin]
- 5) IC 7408 :- Quad 2 I/P AND gate [14 Pin]
- 6) IC 7432 :- Quad 2 I/P OR gate [14 Pin]
- 7) IC 7404 :- Hex NOT gate [14 Pin]
- 8) IC 7486 :- Quad 2 I/P XOR gate [14 Pin]
- 9) IC 7483 :- 4 Bit adder [16 Pin]
- 10) IC 74153 :- Bi 4x1 Multiplexer [16 Pin]
- 11) IC 74139 :- Bi 4x1 Demultiplexer [16 Pin]
- 12) IC 7485 :- 4 Bit Comparator [16 Pin]
- 13) ~~IC 7490 :- Mod-10, Mod-5 counters [14 Pin]~~



- | | | |
|-----|---|----------|
| 14) | IC 7492 :- Mod 12 Counters | [14 Pin] |
| 15) | IC 7493 :- Mod 16 Counters | [14 Pin] |
| 16) | IC 74192 :- Mod 10, Mod 6 Counters | [16 Pin] |
| 17) | IC 74193 :- Programmable up-down counters | [16 Pin] |
| 18) | IC 741 :- Operational Amplifier (op-amp) | [8 Pin] |
| 19) | IC 555 :- 555 Timer | [8 Pin]. |

HALF ADDER



$$S = A \oplus B$$

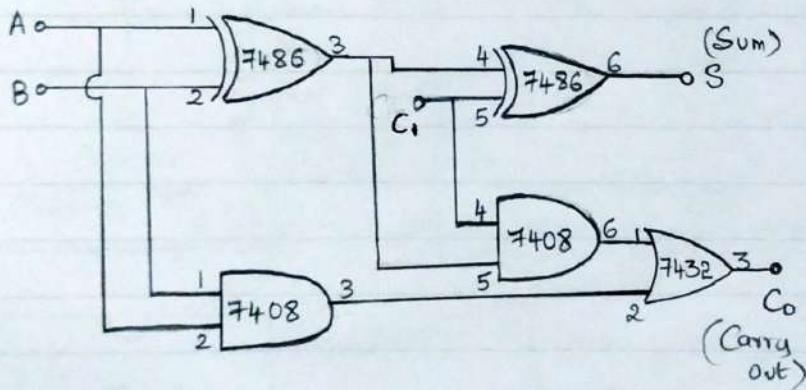
$$C_0 = A \cdot B$$

A	B	S	C ₀
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

FULL ADDER

$$S = A \oplus B \oplus C_i$$

$$C_o = A \cdot B + B \cdot C_i + A \cdot C_i$$



A	B	C _i	S	C _o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

EXPERIMENT-1 :- Realisation of Half Adder and Full Adder Using Basic Gates

AIM:- To design & implement half adder and full adder using basic gates.

APPARATUS :- IC 7486, IC 7408, IC 7432, Trainer kit, Patch cards.

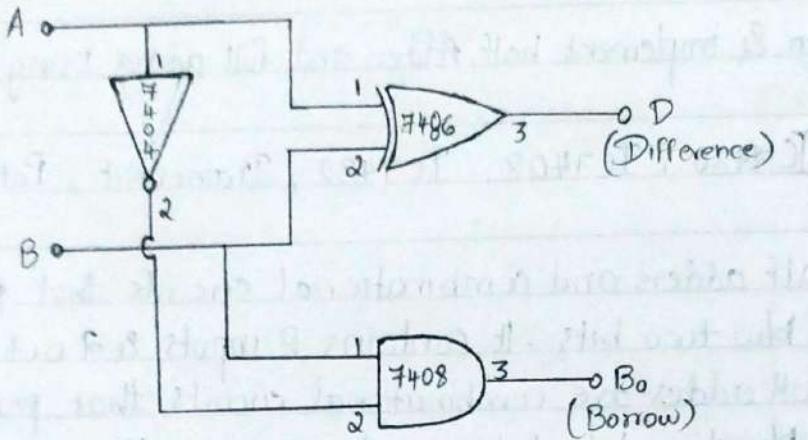
THEORY :- Half adders are combinational circuits that performs addition b/w two bits. It contains 2 inputs & 2 output.
Full adder are combinational circuits that performs addition b/w two bits taking into account the carry of the lower significant stage. It contains 3 inputs & 2 o/p.

PROCEDURE :-

- 1) Truth Tables for half adder and full adder is to be written.
- 2) Insert the IC's into the slots provided in the trainer kit.
- 3) Using patch cards, connects & arrive at the circuit diagram shown at the left (both half & full adder).
- 4) +5V DC Supply is given to the IC's
- 5) Switch 'ON' the kit after ensuring that all connections are made properly.
- 6) Give different inputs and check for the outputs by referring to the respective truth table

RESULT :- Half adder & Full adder realised using basic gates.

HALF SUBTRACTOR

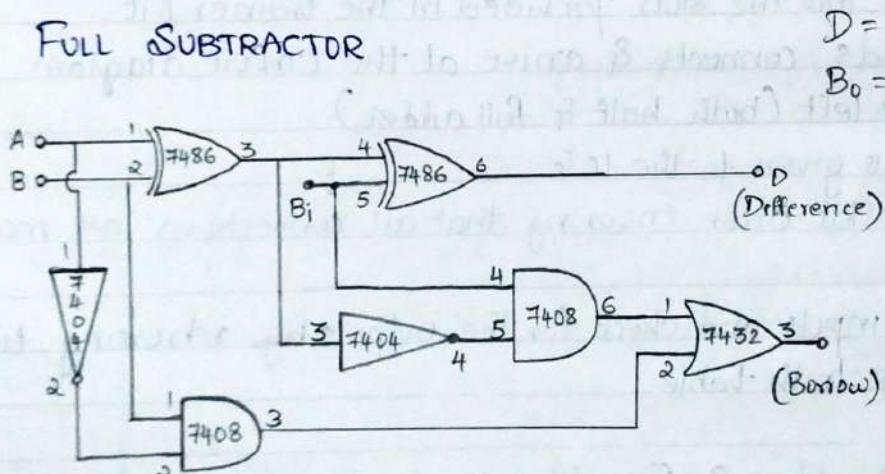


$$D = A \oplus B$$

$$B_0 = \overline{A} \cdot B$$

A	B	D	B ₀
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

FULL SUBTRACTOR



$$D = A \oplus B \oplus C$$

$$B_i = \overline{A} \cdot B_i + \overline{A} \cdot B + B \cdot B_i$$

A	B	B _i	D	B ₀
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

EXPERIMENT No - 2 : Realisation of Half Subtractor & Full Subtractor using Basic gates.

Aim:- To design & implement half Subtractor & full Subtractor using basic gates.

APPARATUS :- IC 7486, IC 7408, IC 7432, IC 7404, Trainer kit, Patch cards.

THEORY :- Half Subtractors are combinational circuits that performs subtraction b/w two bits. It contains 2 inputs & 2 outputs.

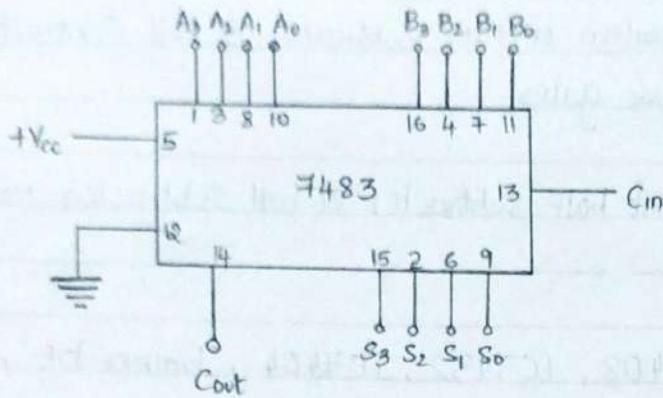
Full Subtractors are combinational circuits that performs addition b/w two bits taking into account the borrow of the lower significant stage. It contains 3 inputs & 2 outputs.

PROCEDURE :-

- 1) Truth Tables for half subtractor & full subtractor is to be written.
- 2) Insert the IC's into the slots provided in the trainer kit.
- 3) Using patch cards, connect & arrive at the circuit diagram shown at the left (both for half subtractor & full subtractor).
- 4) +5V DC Supply is given to the IC's.
- 5) Switch 'ON' the trainer kit after ensuring all connections are made properly.
- 6) Give different inputs & check for the output by referring to the respective truth tables.

~~RESULT:-~~ Half Subtractor & Full Subtractor realised using basic Gates.

4 BIT ADDER



PIN DIAGRAM IC 7483

A ₃	1	B ₃	16
S ₂	2	S ₃	15
A ₂	3	Cout	14
B ₂	4		13
+V _{cc}	5	Cin	12
S ₁	6		11
B ₁	7	B ₀	10
A ₁	8	A ₀	9
		S ₀	

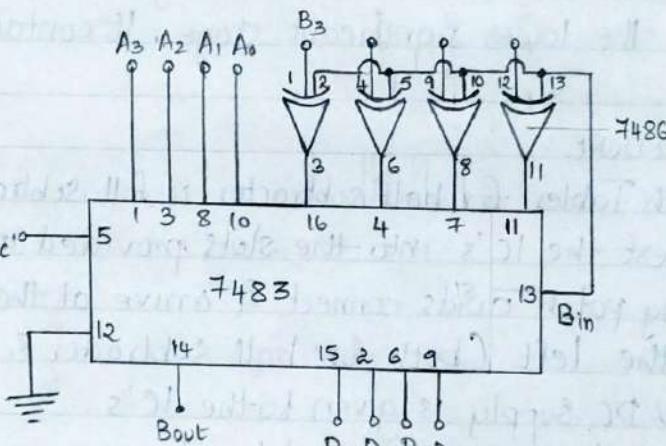
Example : 7+2=9

$$7 \rightarrow A_3, A_2, A_1, A_0 \rightarrow 0111$$

$$2 \rightarrow B_3, B_2, B_1, B_0 \rightarrow 0010$$

$$\underline{9} \rightarrow S_3, S_2, S_1, S_0 \rightarrow \underline{1001}$$

4 BIT SUBTRACTOR



Example : 13-5=8

$$13 \rightarrow A_3, A_2, A_1, A_0 \rightarrow 1101$$

$$5 \rightarrow B_3, B_2, B_1, B_0 \rightarrow 0101$$

$$\underline{8} \rightarrow D_3, D_2, D_1, D_0 \rightarrow \underline{1000}$$

EXPERIMENT NO - 3 :- Realisation of 4-bit Adder & Subtractor using a 7483 IC.

Aim:- To design & implement a 4 bit adder & subtractor using a 7483 IC.

APPARATUS :- IC 7483, IC 7486, Trainer kit, Patch cards

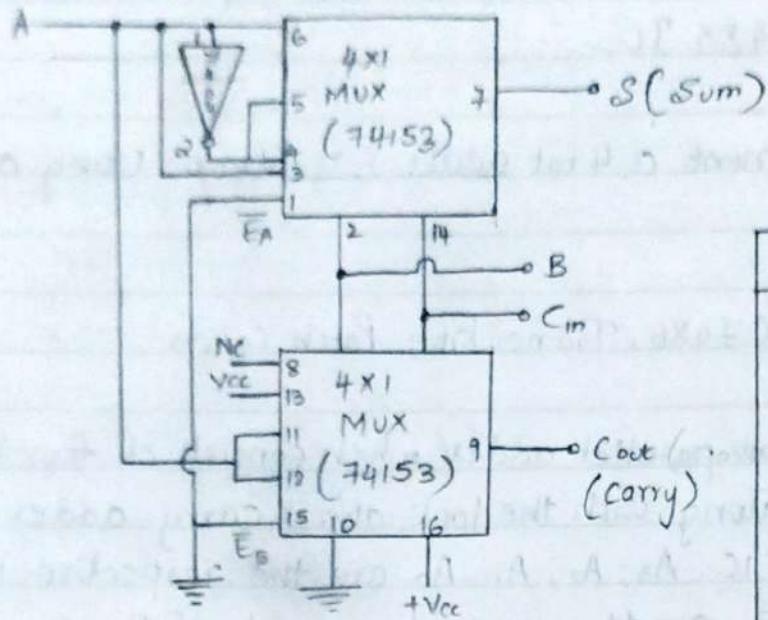
THEORY :- IC 7483 is a 4 bit parallel adder which consists of four interconnected full adder along with the look ahead carry adder circuit. It is a 16 pin IC. A_3, A_2, A_1, A_0 are the respective inputs of A & B_3, B_2, B_1, B_0 are the respective inputs of B. C_{in} is the carry input and C_{out} is the carry output & the sum output is S_3, S_2, S_1, S_0 denoting the respective output of S.

PROCEDURE :-

- 1) Truth Table for 4-bit adder & subtractor is to be written.
- 2) Insert the IC's into the slots provided in the trainer kit.
- 3) Using patch cards, connect & arrive at the circuit diagram shown at the left (both for parallel adder and parallel subtractor)
- 4) +5V DC Supply is given to the IC's
- 5) Switch 'ON' the trainer kit after ensuring all connections are made properly.
- 6) Give different inputs & check the outputs by referring to the respective truth table.

RESULT :- 4 bit parallel adder & parallel subtractor realised using 7483 IC

Full ADDER USING Mux



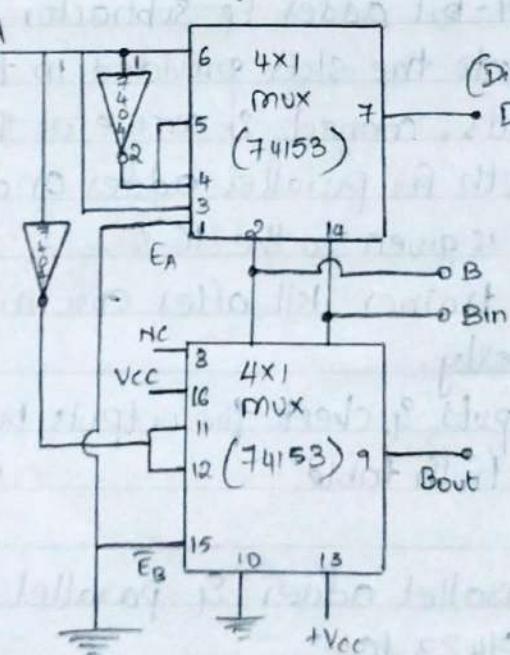
A	B	C _i	S	C _o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

PIN DIAGRAM

IC 74153

\bar{E}_A	1	16	+V _{cc}
S _i	2	15	\bar{E}_B
I _{3A}	4	14	S _o
I _{2A}	5	13	I _{3B}
I _{1A}	3	12	I _{2B}
I _{0A}	6	11	I _{1B}
Z _A	7	10	I _{0B}
GND	8	9	Z _B

Full SUBTRACTOR USING Mux



A	B	B _i	D	B _o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

**EXPERIMENT No: 4 - Realisation of a full adder & full Subtractor
Using a multiplexer (IC 74153).**

Aim: To design & implement a full adder and a full subtractor using a multiplexer (IC 74153)

APPARATUS : A multiplexer is a circuit which allows digital information from different sources to be routed onto a single line for transmission over that line for a common destination

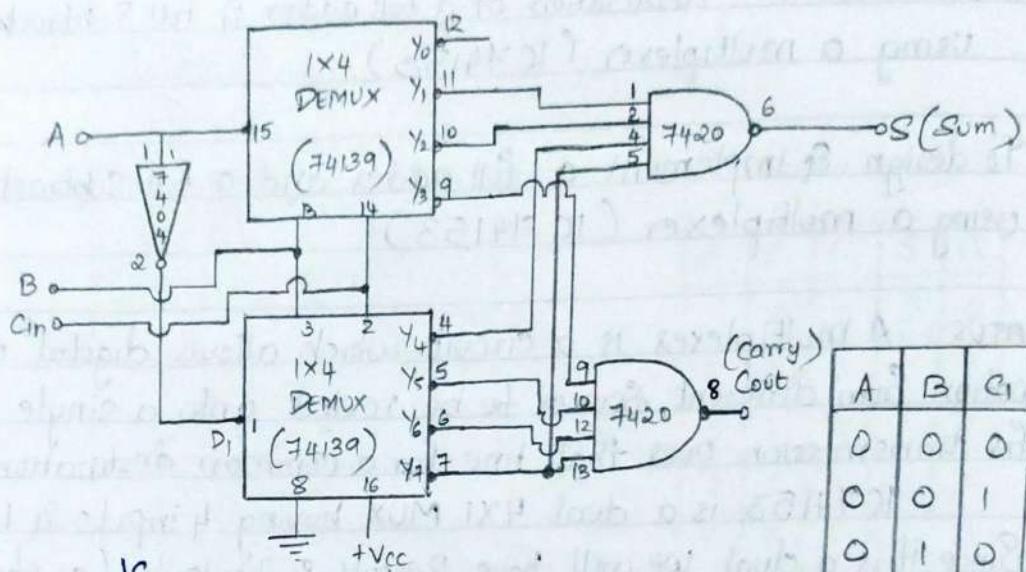
IC 74153 is a dual 4x1 MUX having 4 inputs & 1 o/p.
Since it is a dual we will have 8 inputs & 2 outputs (as shown).
So. S₁ & S₀ are the common select input & E_a & E_b are the active Low (or) Enable input.

PROCEDURE :

- 1) Truth Table for full adder and full subtractor is to be written.
- 2) Insert the IC's into the slots provided in the trainer kit.
- 3) Using patch cards, connect & arrive at the circuit diagram show at the left (both for full adder & full subtractor).
- 4) +5V DC supply is given to the IC's
- 5) Switch 'ON' the trainer kit after ensuring all connections are made properly.
- 6) Give different inputs & check for the outputs by referring to the respective truth table.

RESULT:- Full adder & Full subtractor realised using a multiplexers (IC 74153).

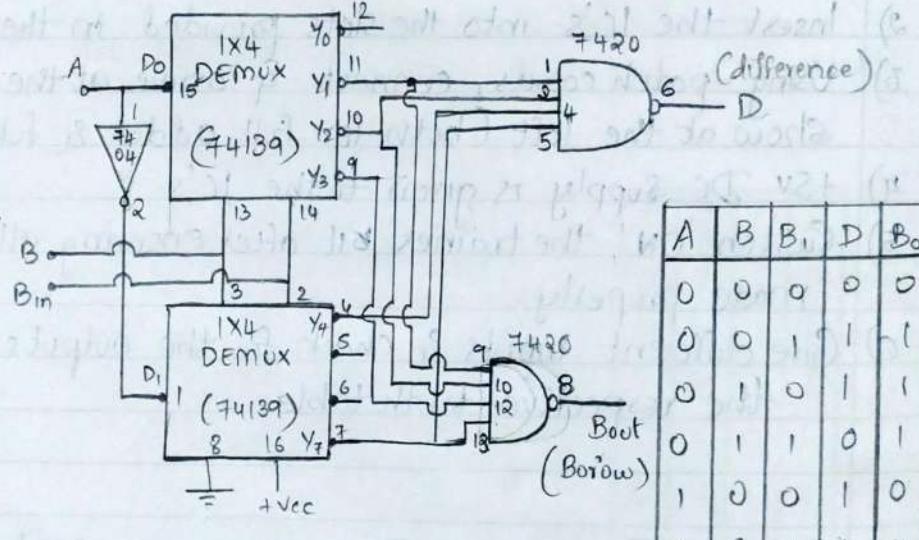
FULL ADDER USING DEMUX



PIN DIAGRAM IC 74139

E _A	1	16	+V _{cc}
I _A	2	7	E _B
I _B	3	4	2A
IY ₀	4	1	2B
IY ₁	5	3	2Y ₀
IY ₂	6	9	2Y ₁
IY ₃	7	11	2Y ₂
GND	8	9	2Y ₃

FULL SUBTRACTOR USING DEMUX



A	B	B _i	D	B _o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

EXPERIMENT No. 5 Realisation of a full adder and full subtractor using a demultiplexer (IC 74139)

Aim:- To design and implement a full adder and a full subtractor using a demultiplexer (IC 74139)

APPARATUS :- IC 74139, IC 7420, IC 7404, Trainer kit, Patch-cards.

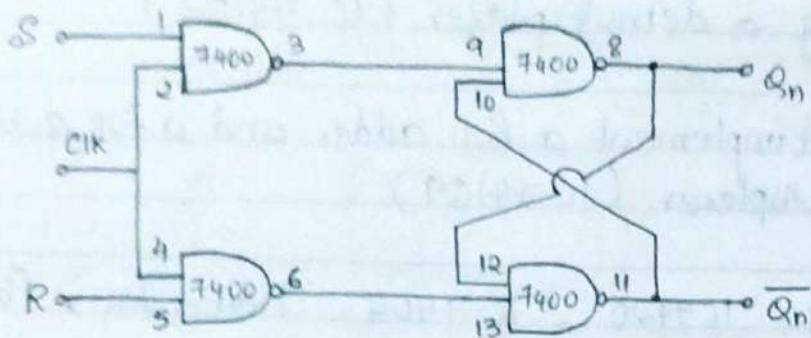
THEORY :- A demultiplexer is a circuit that takes a single input line & routes it to one of the several digital output lines. A demultiplexer of 2^n outputs will have n select lines which select the output line to send the input. IC 74139 is a dual 4x1 DEMUX having A, B, C_0/B_0 as inputs & S/D. & C_0/B_0 as outputs.

PROCEDURE :-

- 1) Truth Table for full adder and full subtractor is to be written
- 2) Insert the IC's into the slots provided in the trainer kit.
- 3) Using patch cards, connect & arrive at the circuit diagram shown at the left (both for full adder & full subtractor).
- 4) +5V DC supply is given to the IC's. Switch ON the trainer kit after ensuring all connections are made properly.
- 5) Give different inputs & check for the outputs by referring to the respective truth tables.

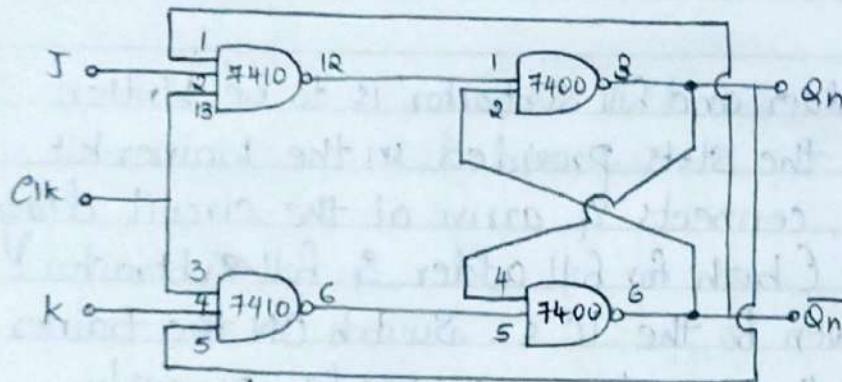
RESULTS :- Full adder and full subtractor realised using a demultiplexer (IC 74139).

SR FLIP FLOP



Clk	S	R	Q_{n+1}
↑	0	0	No Change
↑	0	1	Reset
↑	1	0	Set
↑	1	1	Invalid

JK FLIP FLOP



Clk	J	K	Q_{n+1}
↑	0	0	No change
↑	0	1	Reset
↑	1	0	Set
↑	1	1	Toggle

EXPERIMENT NO: 6 Study of Flip Flops [SR, JK and JK Master Slave].

Aim: To study the flip flops and verify their truth Tables using NAND gate IC's (7400 IC & 7410 IC)

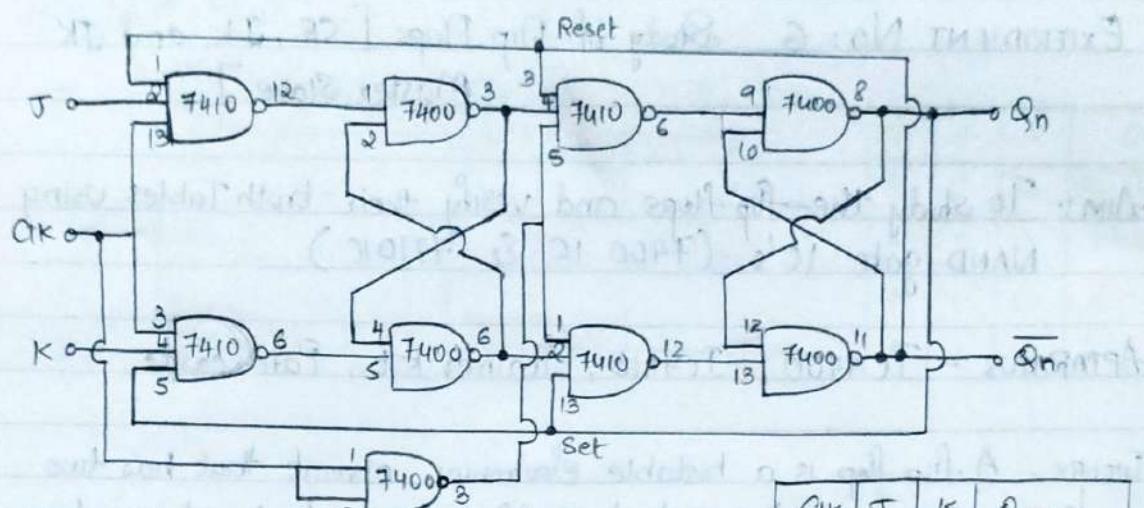
APPARATUS: IC 7400, IC 7410, Trainer kit, Patch cards.

THEORY: A flip flop is a bistable electronics circuit that has two stable states i.e. the output is either low or high. These two stable states are called as reset & set respectively. The output will remain at set which some changes is performed. Flip Flop are also regarded as memory devices.

SR Flip Flop: An SR flip flop is constructed using NAND gates as shown in the left. It has 2 inputs i.e. S & R. When both S & R is 0 (during transition of clock pulse), the output remains in previous state. When S=0 & R=1, output reset & similar. When S=1 & R=0, the output sets. When S & R are high the output is ambiguous.

JK Flip Flop: The functioning of a JK flip flop is same as that of SR flip flop except for one major difference. When J & K are high, the output of the flip flop goes to its opposite stable states upon the transition of clock pulse. It gives a toggling output instead of ambiguous output & this mode is called toggle mode of operation.

JK MASTER SLAVE FLIP FLOP.



CK	J	K	Q_{n+1}
1	0	0	No change
↑	0	1	Reset
↑	1	0	Set
1	1	1	Toggle

JK Master Slave Flip Flop :- The construction for their flip flop is done by a master & a slave section in series. The positive clock is given to the master & negative clock is given to the master & slave. Hence the master responds first to J & K inputs & then the slave. If $J=1$ & $K=0$, the master sets with positive clock. The high output of master goes to slave & when negative clock is applied, the slave copies the action of the master & gives high output. If $J=0$, $K=1$ master & resets with positive clock. The high output of master drives K input & slave is also driven by the master at K input. Slave reacts as the high output is given by K. So the slave has the gain behaved in the same way as the master.

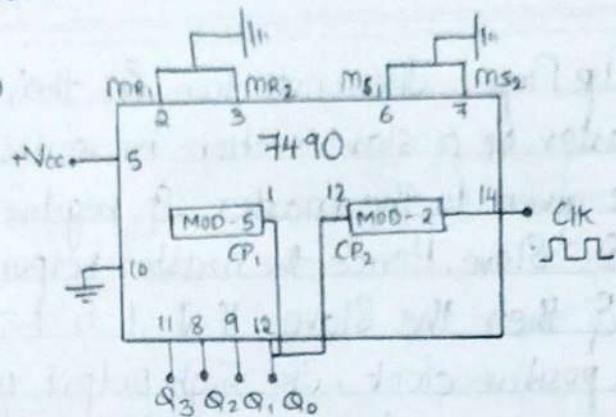
PROCEDURE :-

- 1) Truth Table for the flip flop is written down.
- 2) Insert the IC's into the slot provided in the kit.
- 3) Using patch cards connect & arrive at the ckt diagram
- 4) +5V DC Supply is given to all IC's. Switch ON the kit after ensuring all connections are made.
- 5) By giving clock pulse & the respective high/low values for SR or JK check for the outputs by referring to the respective Truth Table.

RESULT :- All Types of flip flop [SR, JK, JK Slave Master] have been studied & implemented.

IC 7490 COUNTER

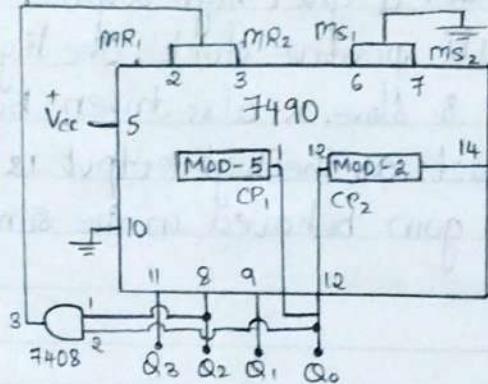
MOD-10



Truth Table (5)

$\textcircled{1}$	Q ₃	Q ₂	Q ₁	Q ₀
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0

MOD-5



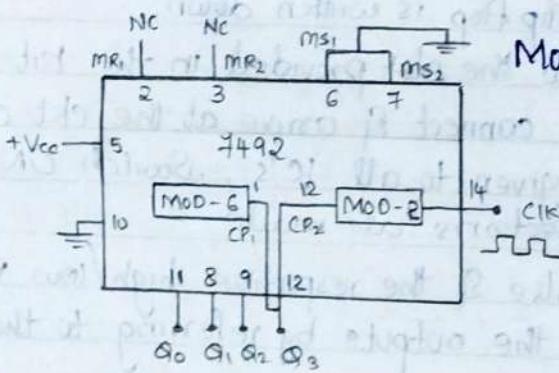
Truth Table (10)

$\textcircled{1}$	Q ₃	Q ₂	Q ₁	Q ₀
0	0	0	0	0
1	0	0	0	0
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Truth Table (16)

$\textcircled{1}$	Q ₃	Q ₂	Q ₁	Q ₀
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

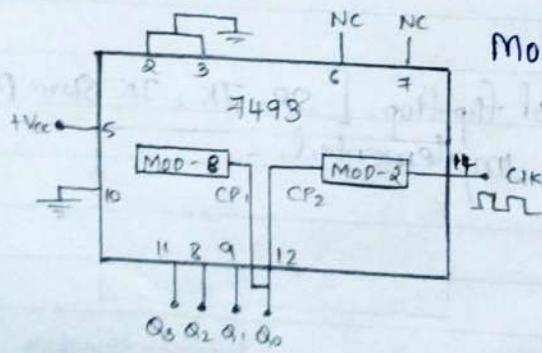
MOD-12



Truth Table (12)

$\textcircled{1}$	Q ₃	Q ₂	Q ₁	Q ₀
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

MOD-16



EXPERIMENT NO: 7 STUDY OF COUNTERS

AIM: To study the counter's IC's using 7490, 7492, 7493, 74192, and 74193.

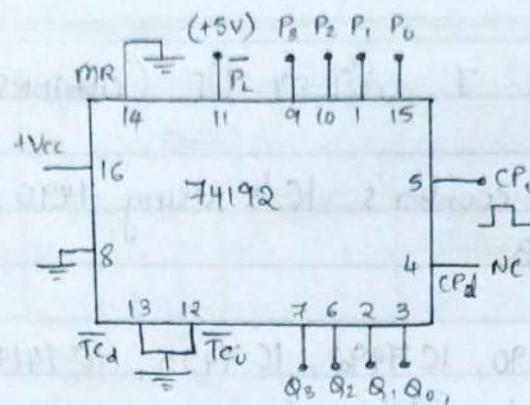
APPARATUS: - IC 7490, IC 7492, IC 7493, IC 74192, IC 74193, Trainer kit, Patch cards.

THEORY:-

- 1) IC 7490 - It is a synchronous decade counter which counts from 0[0000] to 9[1001]. It consists of 2 stages Mod-2 & Mod-5. Two clock pulses are used where one is used to count for each step & the other to reset the output to 0000. If we want to use the IC for different modes, give corresponding high values from output to an AND gate & short the o/p to an AND gate & short the output at MR₁ & MR₂.
- 2) IC 7492 - It is a divide by 12 counter where it's generally used to decide the i/p frequency by 12 i.e. output frequency is $(1/12)^{th}$ of input frequency. This IC also consists of a Mod-2 & MOD-6 stage.
- 3) IC 7493 - It is an asynchronous MOD-16 counter which counts from 0[0000] to 15[1111] on application of clock pulse. It has 4 stages, MOD-2 & MOD-8. If we want to use the IC for different modes, gives corresponding high values from o/p to an AND gate & short the o/p at MR₁ & MR₂.
- 4) IC 74192 & IC 74193 :- These IC's are synchronous up-down MOD-16 & MOD-10 binary counters. Here separate clock

IC COUNTER 74192

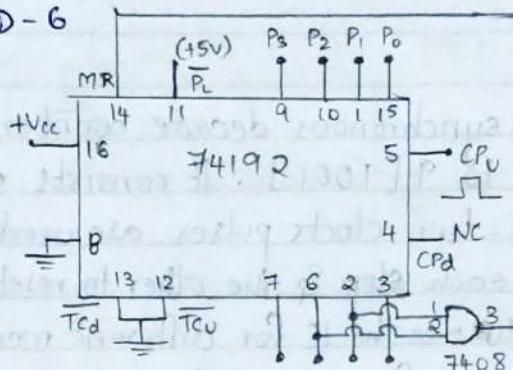
MOD-10



Truth Table (6)				
Q	Q ₃	Q ₂	Q ₁	Q ₀
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1

Truth Table (10)				
Q	Q ₃	Q ₂	Q ₁	Q ₀
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

MOD-6



Truth Table UP				
Q	Q ₃	Q ₂	Q ₁	Q ₀
0	0	0	1	1
1	0	1	0	0
2	0	1	0	1
3	0	1	1	0
4	0	1	1	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1

Programmable UP Counter

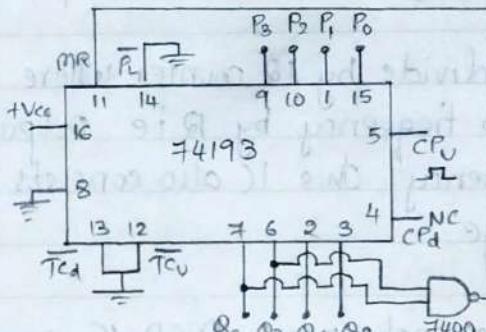
3 [0011] to 11 [1011]

MR = 0, P₃ = P₂ = 0
P₁ = P₀ = 1

Connect 5 to clk.

4 = High

DOWN



Truth Table				
Q	Q ₃	Q ₂	Q ₁	Q ₀
0	1	1	0	0
1	1	0	1	1
2	1	0	1	0
3	1	0	0	1
4	1	0	0	0
5	0	1	1	1
6	0	1	1	0
7	0	1	0	1
8	0	1	0	0

Programmable Down Counter

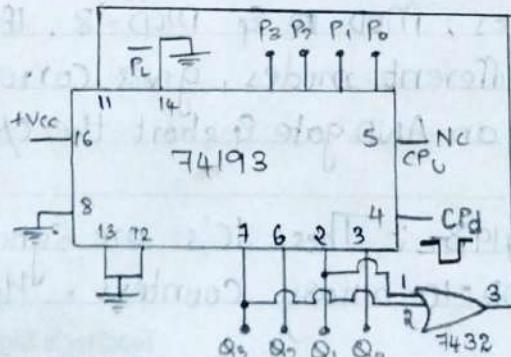
12 [1100] to 4 [0100]

P₃ = P₂ = 1

P₁ = P₀ = 0

Connect 5 to High

4 to CLK



up & clock down, is used. Depending on the type of count, we give to count up or count down. This IC contains 4JK master slave flip flop with external gating & steering logic to provide master reset & individual preset count up & count down operation.

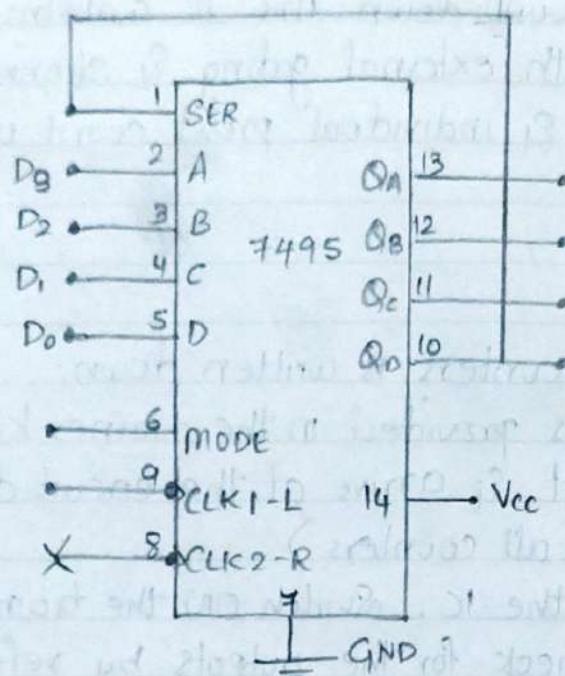
PROCEDURES :-

- 1) Truth tables for all the counters is written down.
- 2) Insert the IC into the slots provided in the trainer kit.
- 3) Using patch cards connect & arrive at the circuit diagram shown at the left (for all counters).
- 4) +5V DC supply is given to the IC. Switch ON the trainer.
- 5) By giving clock pulse, check for the outputs by referring to the respective truth tables.

RESULT:- All types of counter have been studied & implemented

SHIFT REGISTER

INVERTING AMPLIFIER



NON INVERTING AMPLIFIER

SIPO :-

CLOCK	TIME	SERIAL INPUT	OUTPUT			
			Q ₃	Q ₂	Q ₁	Q ₀
1	T ₀	1	1			
2	T ₁	0	0	1		
3	T ₂	1	1	0	1	
4	T ₃	1	1	1	0	1

Parallel data
output after 4
clk pulse

EXPERIMENT NO: 8 STUDY OF SHIFT REGISTER

Aim: Study of shift register IC 7495 for SISO, SIPO, PISO, PIPO Shift right & shift left operation.

APPARATUS :- IC 7495, Trainer kit, Patch cards

THEORY :- Study of Shift Register IC 7495.

- D_s series input data to be right shift.
- D₃, D₂, D₁, D₀ parallel data inputs to be loaded into the shift register.
- M - Mode control
- If M=1 for loading parallel data & to enable Clock 2 (pin 8)
- If M=0 for enabling clock 1 (pin 9)
- Clock 2 for loading parallel input data & for shift left of data.
- Clock 1 for right shift of data.
- Q₃, Q₂, Q₁, & Q₀ parallel output of the shift register.

Shift Right Operation

Serial input parallel output (SIPO) operation

Ex:- To perform SIPO operation, consider a 4 bit data 1101

- Mode control is made 0
- Clock 1 (pin 9) of 7495 is connected to the (monoshot) Pulser.

- The serial input to be converted to parallel output is given to series input D_s. (pin 1).

- After 4 clock pulses the serial input data appears in parallel form as Q₃, Q₂, Q₁ & Q₀ as shown.

VOLTAGE FOLLOWER

SISO:-

CLOCK	TIME	SERIAL INPUT	OUTPUT			
			Q_3	Q_2	Q_1	Q_0
1	T_0	1(LSB)	1			
2	T_1	0	0	1		
3	T_2	1	1	0	1	
4	T_3	1	1	1	0	1
5	T_4		1	1	0	
6	T_5			1	1	
7	T_6				1	

Serial data output
after 7 clk pulses at Q_0

PISO:-

CLOCK	TIME	OUTPUT			
		Q_3	Q_2	Q_1	Q_0
CLK 2	T_0	1	1	0	1
CLK 1	T_1		1	1	0
	T_2			1	1
	T_3				1

Shift register loaded with parallel data
Serial data output
after 4 pulses at Q

PIPO:-

CLOCK	TIME	SERIAL INPUT	OUTPUT			
			Q_3	Q_2	Q_1	Q_0
Clk 2	T_0	1				1
	T_1	0			1	0
	T_2	1		1	0	1
	T_3	1	1	0	1	1

Series input Series output (SISO) Operation

- Mode control is made LOW.
- Clock 1 (pin 9) of 7495 is connected to the Pulser (Mono shot)
- The serial input to be converted to serial output is given to Serial input D_s (pin 1)
- After 4 clock pulses the serial input data appears in parallel form as Q₃, Q₂, Q₁, Q₀ as shown.
- The next 4 clock pulses move the data out of shift register serially at Q₀.

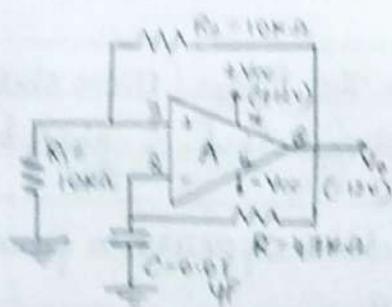
Parallel input parallel output (PIPO) operation.

- Mode control is made HIGH.
- The parallel inputs to be loaded into the shift register are given to D₃, D₂, D₁, D₀ inputs
- Clock 2 (pin 8) is pulsed once. Now D₃, D₂, D₁, D₀ parallel inputs appear on Q₃, Q₂, Q₁, Q₀ lines.

Parallel input Serial output (PISO) operation

- Mode control is made 1
- The parallel inputs to be loaded in to the shift register are given to D₃, D₂, D₁, D₀ inputs
- Clock 2 (pin 8) is pulsed once. Now D₃, D₂, D₁, D₀ parallel inputs appear on Q₃, Q₂, Q₁, Q₀ lines
- C1K 1 (pin 9) is connected to the pulses.
- Mode control is made 0.

Astable Multivibrator [50% Duty Cycle]



Given $\frac{T_{ON}}{T} = 0.5 \quad \text{&} \quad f = 1\text{kHz} \quad \therefore T = 1\text{ms}$

$$T_{ON} = T_{OFF} = RC \log e \left(\frac{1+\beta}{1-\beta} \right)$$

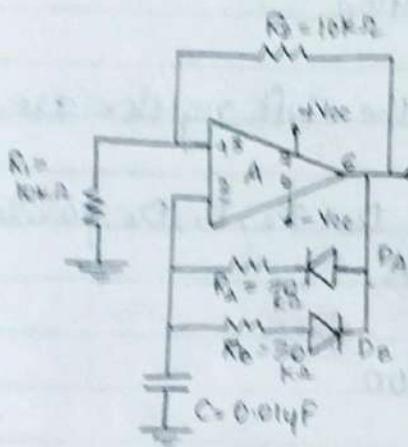
$$\text{where } \beta = \frac{R_2}{R_1 + R_2} = \frac{10}{10+10} = 0.5$$

[Assuming $R_1 = R_2 = 10\text{k}\Omega$]

$$T_{ON} = T_{OFF} = 4 \times 10^{-3} \times 0.01 \times 10^{-6} \log e \left(\frac{0.5+1}{1-0.5} \right) \\ = 0.516\text{ms} \quad (\text{assuming } R = 47\text{k}\Omega)$$

$$T = T_{ON} + T_{OFF} = 1.032\text{ms} \quad (\text{assuming } C = 0.01\mu\text{F})$$

Astable Multivibrator [70% Duty Cycle]



Given $\frac{T_{ON}}{T} = 0.7 \quad \text{&} \quad f = 1\text{kHz}, \quad T = 1\text{ms}$

$$T_{ON} = 0.7\text{ms} \quad \& \quad T_{OFF} = 0.3\text{ms}$$

$$T_{ON} = RC \log e \left(\frac{1+\beta}{1-\beta} \right)$$

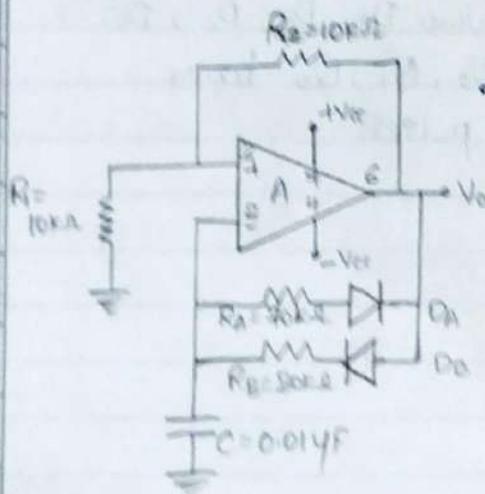
$$T_{ON} = RC \log e (3) \approx RC$$

$$T_{ON} = RAC \quad T_{OFF} = RBC$$

$$\therefore R_A = \frac{0.7\text{ms}}{0.01\mu\text{F}} = 70\text{k}\Omega \quad \text{assume } C = 0.01\mu\text{F}$$

$$\therefore R_B = \frac{0.3\text{ms}}{0.01\mu\text{F}} = 30\text{k}\Omega \quad R_1 = R_2 = 10\text{k}\Omega$$

Astable Multivibrator [30% Duty Cycle]



Given $\frac{T_{ON}}{T} = 0.3 \quad \& \quad f = 1\text{kHz}, \quad T = 1\text{ms}$

$$T_{ON} = 0.3\text{ms} \quad \& \quad T_{OFF} = 0.7\text{ms}$$

$$T_{ON} = RC \log e \left(\frac{1+\beta}{1-\beta} \right)$$

$$T_{ON} = RC \log e (3) \approx RC$$

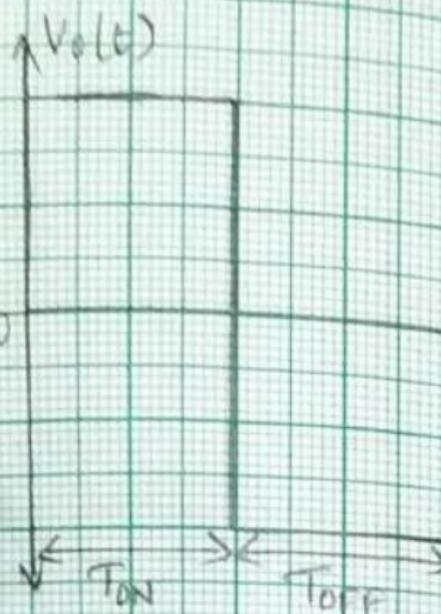
$$T_{ON} = RAC \quad T_{OFF} = RBC$$

$$\therefore R_A = \frac{0.3}{0.7} = 30\text{k}\Omega \quad \text{assuming } C = 0.01\mu\text{F}$$

$$R_1 = R_2 = 10\text{k}\Omega$$

$$\therefore R_B = \frac{0.7}{0.3} = 70\text{k}\Omega$$

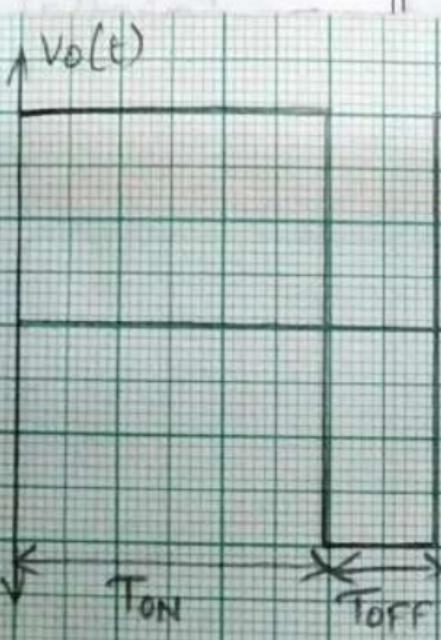
Expt. No.:



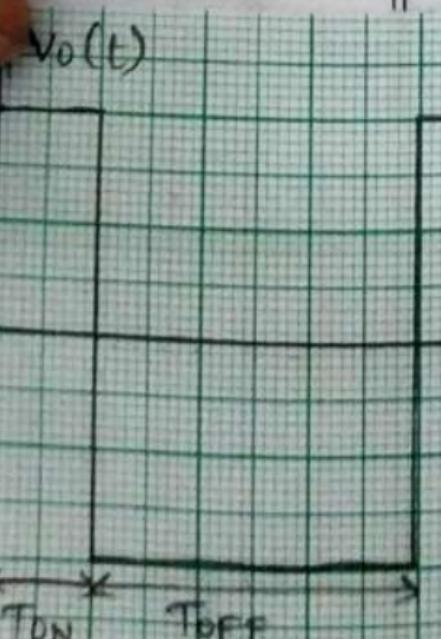
$$C = 0.01 \mu F$$

THEORY

+V



a) Insert



$$\begin{aligned} C &= 0.01 \mu F \\ R &= 10 k\Omega \end{aligned}$$

RESULT

EXPERIMENT NO.- 9 STUDY OF ASTABLE MULTIVIBRATOR USING OP-AMP.

Aim: To design an astable multivibrator using op-amp for different duty cycles [30%, 50% & 70%].

APPARATUS:- IC 741 op-amp, resistor, Capacitor, regulated power, Signal generator, CRO, CRO Probe, breadboard, wires.

THEORY :- If the op-amp is operated such that it switches between $+V$ & $-V$ rapidly & repeatedly, then it generates square wave output & functions like a square wave generator. In this mode of operation it is also called as astable multivibrator as it does not have any stable (both its states are quasi-stable).

PROCEDURE :-

- 1) Check the 741 op-amp & draw the expected output waveform.
- 2) Insert the IC on the breadboard & make the connections, as shown using connecting wires.
- 3) Give the probes at the output to CRO. Observe the output waveform in the CRO.
- 4) Note the output & repeat them for all the different duty cycles (i.e 30%, 50% & 70%).
- 5) Plot the output graphs in a suitable graph sheet & compare them with the theoretical graphs.

RESULT: The output of astable multivibrator for the different duty cycles, using op-amp has been studied & verified.

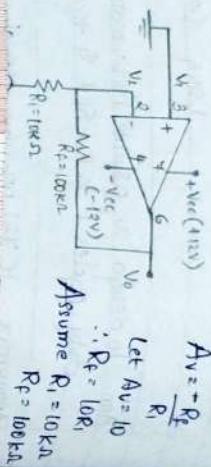
Teacher's Signature _____

Inverting Amplifier

Expt. No.:

Page No.: ...15...

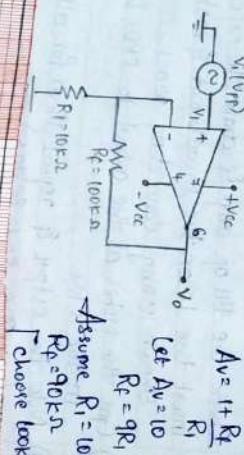
f	T_p	O_p	A_v
100	2V	19.4	9.7
500	2V	19.4	9.7
1K	2V	19.4	9.7
5K	2V	19.4	9.7
10K	2V	19.2	9.6
12K	2V	19.0	9.5
15K	2V	17.8	8.9
17K	2V	16.4	8.2
20K	2V	14.6	7.3
50K	2V	4.0	3.5
100K	2V	3.8	1.9
150K	2V	3.0	1.5
200K	2V	2.4	1.2
250K	2V	2.0	1.0
300K	2V	1.8	0.9
500K	2V	1.8	0.8
1M	2V	1.0	0.5



APPARATUS: IC741 op-amp, resistors, regulated power supply, scope, breadboard, wires.

AIM: To conduct an op-amp circuit for inverting, non-inverting amplifiers & voltage followers.

NON INVERTING AMPLIFIER



$$A_v = \frac{1 + R_f}{R_1}$$

Non Inverting Amplifiers - These amplifiers provides 180° phase shift between input & output. For these circuit, voltage gain is independent of loop gain. Voltage gain primarily depends on R_f/R_1 ratio. If $R_f > R_1$, gain is > 1 . If $R_f = R_1$, gain is $= 1$. If $R_f < R_1$, gain is < 1 . R_f forms feedback network. The polarity of output voltage is opposite to that of input. Hence feedback is considered to be negative in nature.

Non Inverting Amplifiers - These amplifiers do not give any output. In this type, voltage gain is positive indicating inphase. Voltage gain is independent on R_f & R_1 . The input of amp like is very large.

Notes

Notes

Notes

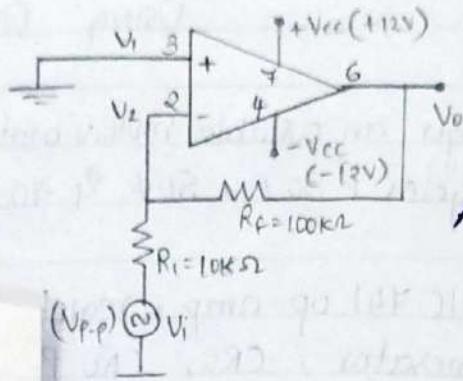
Notes

Notes

Teacher's Signature

f	I/p	O/p	Av.
100	2V	19.4	9.7
500	2V	19.4	9.7
1K	2V	19.4	9.7
5K	2V	19.4	9.7
10K	2V	19.2	9.6
12K	2V	19.0	9.5
15K	2V	17.8	8.9
17K	2V	16.4	8.2

INVERTING AMPLIFIER



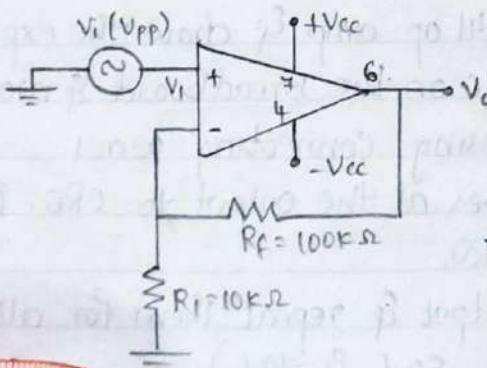
$$Av = -\frac{R_f}{R_i}$$

Let $Av = 10$
 $\therefore R_f = 10R_i$

Assume $R_i = 10k\Omega$
 $R_f = 100k\Omega$

f	I/p	O/p	Av
100	2V	19.4	9.7
500	2V	19.4	9.7
1K	2V	19.4	9.7
5K	2V	19.4	9.7
10K	2V	19.2	9.6
12K	2V	19.0	9.5
15K	2V	17.8	8.9
17K	2V	16.4	8.2
20K	2V	14.6	7.3
50K	2V	7.0	2.5

NON INVERTING AMPLIFIER



$$Av = 1 + \frac{R_f}{R_i}$$

Let $Av = 10$
 $R_f = 9R_i$

Assume $R_i = 10k\Omega$
 $R_f = 90k\Omega$
 [choose 100kΩ]

EXPERIMENT NO:10 Study of inverting, non inverting amplifiers and Voltage Followers

Aim:- To conduct an op-amp circuit for inverting, non inverting amplifiers & voltage followers.

APPARATUS:- IC741 op amp, resistors, regulated power supply, signal generator, CRO, CRO probes, breadboard, wires.

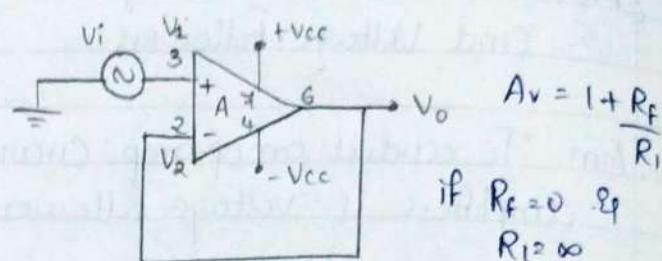
THEORY:- Opamp are high gain differential amplifiers which uses feedback to stabilises voltage gain. Opamps have high loop gain & high open impedance. They are used in analog computer operations & in oscillators & instrumentation circuit.

Inverting Amplifiers - These amplifiers provides 180° phase shift between input & output. For these circuit, voltage gain is independant of loop gain. Voltage gain primarily depends on R_f & R_i ratio. If $R_f > R_i$, gain is > 1 . If $R_f = R_i$, gain is $= 1$ & if $R_f < R_i$, gain is < 1 . R_f forms feedback network. The polarity of output voltage is opposite to that of input. Hence feedback is considered to be negative in nature.

Non Inverting Amplifiers - These amplifiers do not give any phase shift between input & output. In this type, voltage gain is always > 1 . The Voltage gain is positive indicating that output & input are inphase. Voltage gain is independent of loop gain but depends on R_f & R_i . The input impedance for non inverting amplifier is very large.

f	V _f	O/P	A _v
100	2V	2V	1
200	2V	2V	1
300	2V	2V	1
1KH	2V	2V	1
2K	2V	2V	1
3K	2V	2V	1
10K	2V	2V	1
20K	2V	2V	1
30K	2V	2V	1
100K	2V	2V	1
200K	2V	2V	1
300K	2V	2V	1
1MH	2V	2V	1

VOLTAGE FOLLOWER

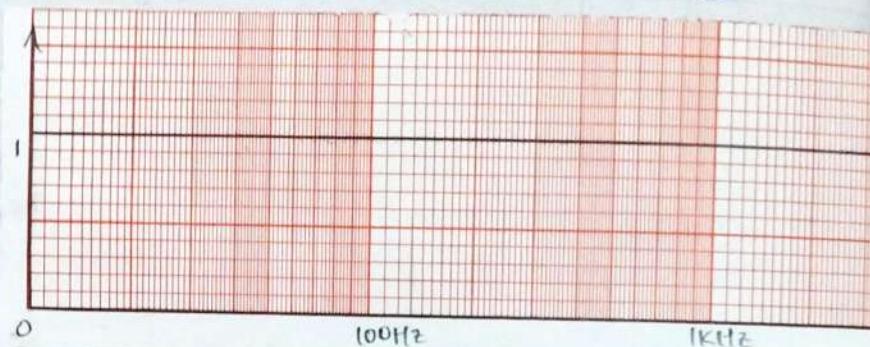


$$A_v = 1 + \frac{R_f}{R_1}$$

if $R_f = 0$ &
 $R_1 = \infty$

then $A_v = 1$

$$\underline{V_o} = \underline{V_i}$$

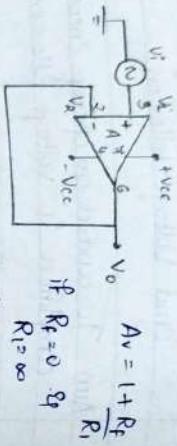


Voltage Follower

Expt. No.:

Page No.:

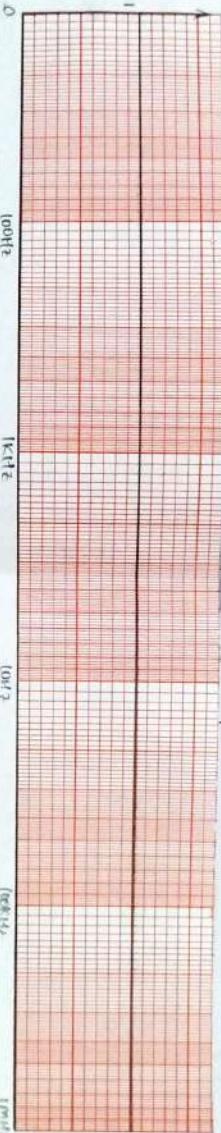
f	V _t	O _f	A _v
100	2V	2V	1
800	2V	2V	1
1MHz	2V	2V	1
2K	2V	2V	1
9K	2V	2V	1
10K	2V	2V	1
20K	2V	2V	1
30K	2V	2V	1
50K	2V	2V	1
100K	2V	2V	1



$$\text{then } A_v = \frac{V_o}{V_i}$$

$$V_o = V_i$$

Voltage follower - Here the output voltage follows the input voltage. [$V_o = V_{in}$] Also called as unit gain amplifiers, buffers, amplifiers, or isolation amplifiers. At input resistance is very large, negligible current is drawn from source. Hence, the signal source is not loaded. To avoid this in transducers we can use the voltage follower circuit between transducers & the amplifier. Such as use for impedance matching is called as buffer.



spectred graph
id 2 make the connections
wires
output to the CRO feed a

- 4) Note the output. Record your observations in a tabular form
- 5) Plot the frequency response graph for all the three cases of compare them with the theoretical graphs

Result: Inverting amplifiers, non inverting amplifiers & voltage followers circuits using IC 741 opamp have been studied & implemented.

Teacher's Signature _____

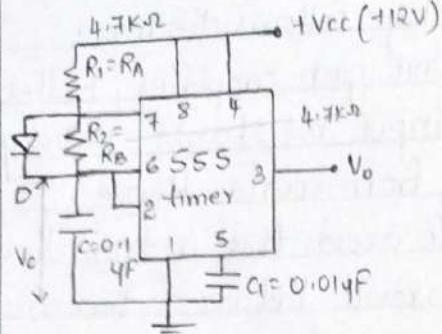
Voltage Follower - Here the output voltage follows the input voltage. [$V_o = V_{in}$]. Also called as unit gain amplifier, buffer amplifiers or isolation amplifiers. At input resistance is very large, negligible current is drawn from source. Hence, the signal source is not loaded. To avoid this in transducer we can use the voltage follower circuit between transducer & the amplifier, such as use for impedance matching is called as buffer.

PROCEDURE :-

- 1) Check the 741 opamp draw the expected graph.
- 2) Insert the IC on the bread board & make the connections as shown using connecting wires.
- 3) Give the probes at the input & output to the CRO feed a sinusoidal input at 1Vpp.
- 4) Note the output. Record your observations in a tabular form.
- 5) Plot the frequency response graph for all the these cases & compare them with the theoretical graphs.

Result : Inverting amplifier, non inverting amplifier & voltage follower circuits using IC 741 opamp have been studied & implemented.

ASTABLE MULTIVIBRATOR [50% Duty cycle]



Given $\frac{T_{ON}}{T} = 0.5 \quad \& \quad f = 1.0 \text{ kHz}$
 $T = 1.0 \text{ ms}$

$$T_{ON} = 0.693(R_A + R_B)C$$

Assume $C = 0.1\mu\text{F}$

$$\therefore R_A + R_B = \frac{0.5 \times 10^{-3} \times 1}{0.693 \times 0.1 \times 10^{-6}}$$

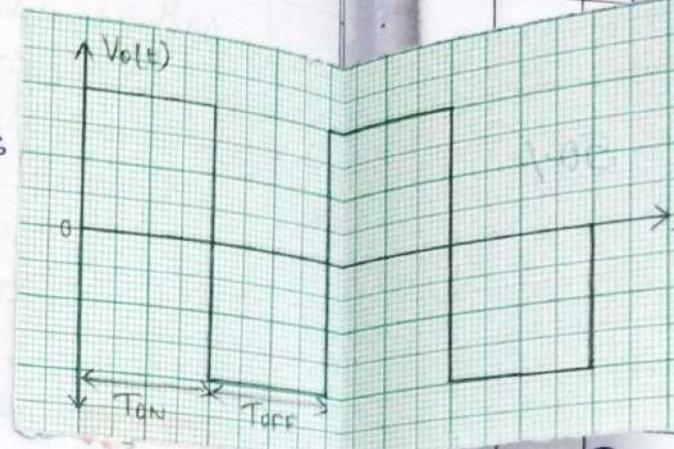
$$R_A + R_B = 7.215 \text{ k}\Omega$$

$$T_{OFF} = T_{ON} = 0.5 \quad [R_A = R_B]$$

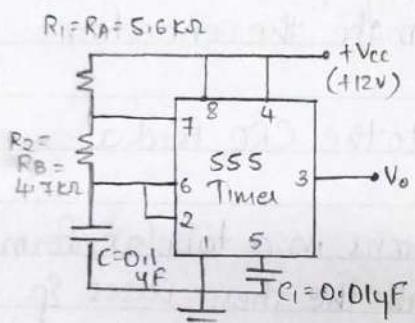
$$\text{let } C_1 = 0.01\mu\text{F}$$

$$R_A = 4.7 \text{ k}\Omega \quad \& \quad R_B = 4.7 \text{ k}\Omega$$

$$R_A + R_B \approx 7.2 \text{ k}\Omega$$



ASTABLE MULTIVIBRATOR [70% Duty cycle]



Given $\frac{T_{ON}}{T} = 0.7 \quad \& \quad f = 1 \text{ kHz}, T = 1 \text{ ms}$

$$T_{ON} = 0.693(R_A + R_B)C$$

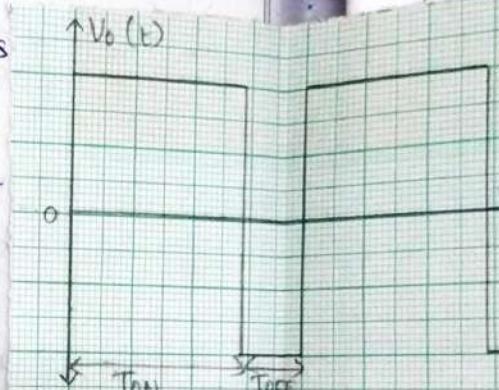
$$R_A + R_B = \frac{0.7 \times 10^{-3} \times 1}{0.693 \times 10^{-6} \times 0.1} \approx 10.1 \text{ k}\Omega$$

$$T_{OFF} = 0.693 R_B C$$

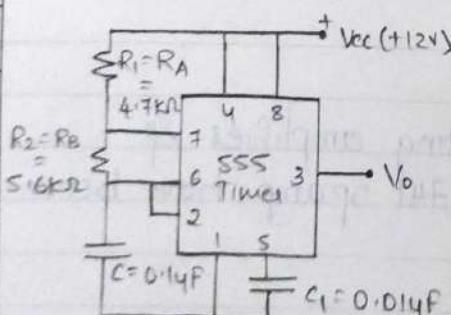
$$\therefore R_B = \frac{0.3 \times 10^{-3} \times 1}{0.693 \times 10^{-6} \times 0.1}$$

$$R_B = 4.32 \text{ k}\Omega \quad (\text{use } 4.7 \text{ k}\Omega)$$

$$R_A = (10.1 - 4.32) \text{ k}\Omega = 5.7 \text{ k}\Omega \quad (\text{use } 5.6 \text{ k}\Omega), \text{ let } C = 0.01\mu\text{F}$$



ASTABLE MULTIVIBRATOR [30% duty cycle]



Given $\frac{T_{ON}}{T} = 0.3 \quad \& \quad f = 1 \text{ kHz}, T = 1 \text{ ms}$

$$T_{ON} = 0.693(R_A + R_B)C$$

$$\therefore R_A + R_B = \frac{0.3 \times 10^{-3} \times 1}{0.693 \times 0.1 \times 10^{-6}} = 4.32 \text{ k}\Omega$$

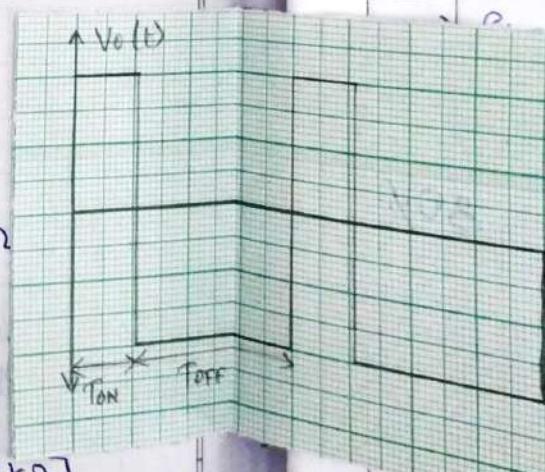
$$T_{OFF} = 0.693 R_B C$$

$$R_B = \frac{0.7 \times 10^{-3} \times 1}{0.693 \times 10^{-6} \times 0.1} = 10.1 \text{ k}\Omega$$

$$R_A = 10.1 - 4.32 = 5.7 \text{ k}\Omega \quad (\text{use } 5.6 \text{ k}\Omega)$$

$$R_B = 10.1 - 4.32 = 5.7 \text{ k}\Omega \quad (\text{use } 5.6 \text{ k}\Omega)$$

Let $C_1 = 0.01\mu\text{F}$



[50% Duty cycle]

$$\text{Given } \frac{T_{ON}}{T} = 0.5 \quad \& \quad f = 1.0 \text{ kHz}$$

$$T = 1.0 \text{ ms}$$

$$T_{ON} = 0.693(R_A + R_B)C$$

$$\text{Assume } C = 0.01 \mu\text{F}$$

$$\therefore R_A + R_B = \frac{0.5 \times 10^{-3} \times 1.0}{0.693 \times 0.1 \times 10^{-6}}$$

$$R_A + R_B = 7.215 \text{ k}\Omega$$

$$T_{OFF} = T_{ON} = 0.5 \quad [R_A = R_B]$$

$$\text{Let } C_1 = 0.01 \mu\text{F}$$

$$\& R_B = 4.7 \text{ k}\Omega$$

$$R_A + R_B \approx 7.2 \text{ k}\Omega$$

[70% Duty cycle]

$$\text{Given } \frac{T_{ON}}{T} = 0.7 \quad \& \quad f = 1 \text{ kHz}, T = 1 \text{ ms}$$

$$T_{ON} = 0.693(R_A + R_B)C$$

$$R_A + R_B = \frac{0.7 \times 10^{-3} \times 1}{0.693 \times 10^{-6} \times 0.1} \approx 10.1 \text{ k}\Omega$$

$$T_{OFF} = 0.693 R_B C$$

$$\therefore R_B = \frac{0.3 \times 10^{-3} \times 1}{0.693 \times 10^{-6} \times 0.1}$$

$$R_B = 4.32 \text{ k}\Omega \quad (\text{use } 4.7 \text{ k}\Omega)$$

$$= 5.7 \text{ k}\Omega \quad (\text{use } 5.6 \text{ k}\Omega), \text{ Let } C = 0.01 \mu\text{F}$$

[30% duty cycle]

$$\text{Given } \frac{T_{ON}}{T} = 0.3 \quad \& \quad f = 1 \text{ kHz}, T = 1 \text{ ms}$$

$$T_{ON} = 0.693(R_A + R_B)C$$

$$\therefore R_A + R_B = \frac{0.3 \times 10^{-3} \times 1}{0.693 \times 0.1 \times 10^{-6}} = 4.32 \text{ k}\Omega$$

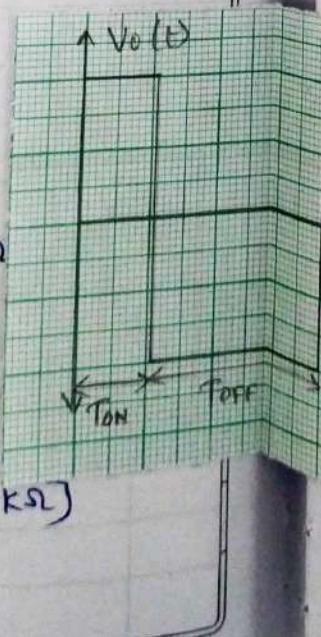
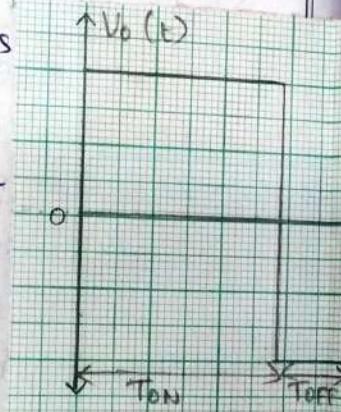
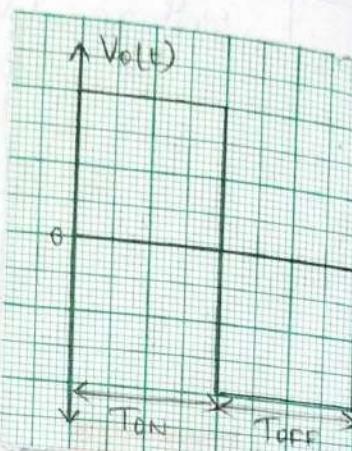
$$T_{OFF} = 0.693 R_B C$$

$$R_B = \frac{0.7 \times 10^{-3} \times 1}{0.693 \times 10^{-6} \times 0.1} = 10.1 \text{ k}\Omega$$

$$R_A = 10.1 - 4.32 = 5.7 \text{ k}\Omega \quad (\text{use } 5.6 \text{ k}\Omega)$$

$$5.7 \text{ k}\Omega \quad (\text{use } 5.6 \text{ k}\Omega)$$

(let $C_1 = 0.01 \mu\text{F}$)



Expt. No.:

EXPERIMENT NO. 11 STUDY OF USING

To design an astable multivibrator cycles [30%, 50%, 70%]

ATUS: 555 timer, resistors, display, signal generator, CRO

THEORY: If the 555 timer is operated low rapidly & separated output & functions like f operation, it is also c does not have to any stable state.

-
555 timer & draw the e i.e. LC on the breadboard

shown using connecting wires.
a) Give the probes at the output to in the CRO.

the output & see repeat th (30%, 50%, 70%).

The output graphs in a sta see them with theoretical

- The output of astable mult using 555 timer has bee

EXPERIMENT No: 11 STUDY OF ASTABLE MULTIVIBRATOR USING 555 TIMER

Aim:- To design an astable multivibrator using 555 timer for different duty cycles [30%, 50%, 70%]

APPARATUS:- 555 timer, resistors, diodes, capacitors, regulated power supply, signal generator, CRO, CRO probes, bread board, wires

THEORY:- If the 555 timer is operated such that it keeps switching high & low rapidly & separately, then it generates square wave output & functions like a square wave generator. In this mode of operation, it is also called as astable multivibrator as it does not have to any stable (both its states are quasi stable) state.

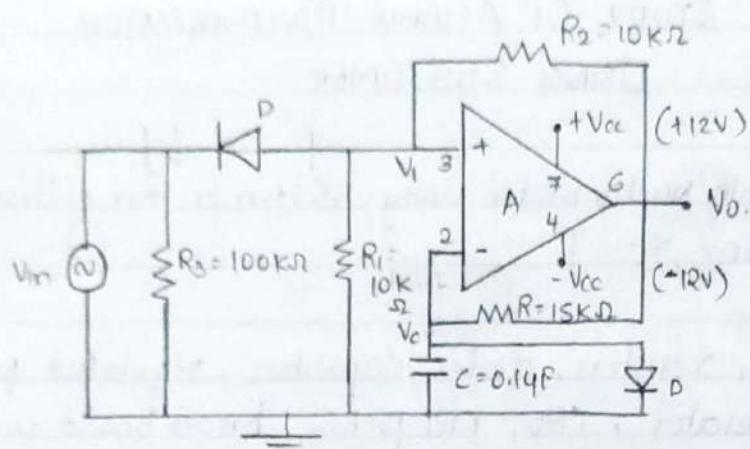
PROCEDURE:-

- 1) Check the 555 timer & draw the expected output waveforms.
- 2) Insert the IC on the breadboard & make the connections as shown using connecting wires.
- 3) Give the probes at the output to CRO. Observe the output waveforms in the CRO.
- 4) Note the output & repeat them for all the different duty cycles (30%, 50%, 70%)
- 5) Plot the output graphs in a suitable graph sheet & compare them with theoretical graphs.

Result:- The output of astable multivibrator for different duty cycles, using 555 timer has been studied & verified.

Teacher's Signature _____

MONOSTABLE MULTIVIBRATOR.



Given $f = 1\text{kHz}$, $T = 1\text{ms}$

$$T = RC \log_e \left(\frac{1}{1-\beta} \right) \text{ where } \beta = \frac{R_2}{R_1 + R_2}$$

$$\beta = 0.5 \quad [\text{assuming } R_1 = R_2 = 10\text{k}\Omega]$$

$$T = RC \log_e \left(\frac{1}{1-0.5} \right)$$

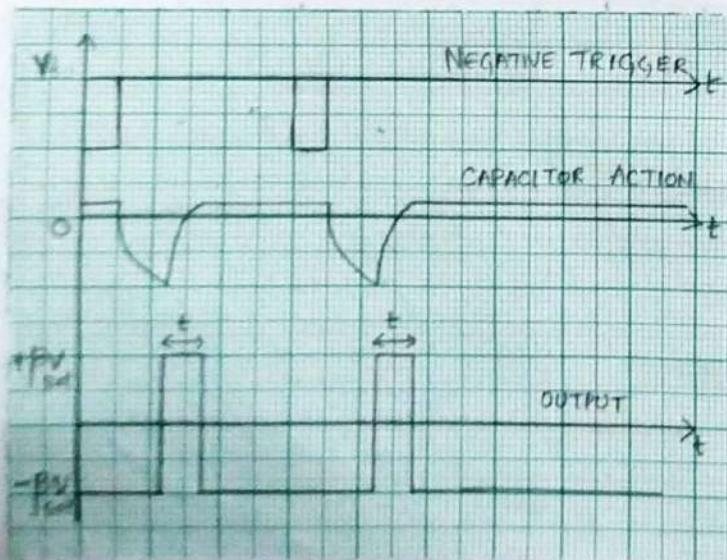
$$T = RC \log_e (2) \rightarrow T = \underline{0.7RC}$$

$$\text{Assume } C = 0.1\mu\text{F} \therefore R = \underline{15\text{k}\Omega}$$

$$\text{let } R_3 = 10R_1 \rightarrow R_3 = 10 \times 10 = 100\text{k}\Omega$$

$$\text{We have } R_3 C_3 = T = 0.1\text{ms}$$

$$\therefore C_3 = \frac{0.1 \times 10^{-3}}{100 \times 10^3} = 0.0001\mu\text{F}$$



Note:- Triggering must be done only after $T_d + T_2$ (ie)
 Input trigger $> (T_d + T_2)$

EXPERIMENT NO: 12 STUDY OF MONOSTABLE MULTIVIBRATOR USING OPAMP.

Aim:- To design a monostable multivibrator using opamp & get the expected waveform.

APPARATUS:- IC 741 opamp, resistors, diodes, capacitors, regulated power supply, signal generator, CRO, CRO probes, bread board, wires,

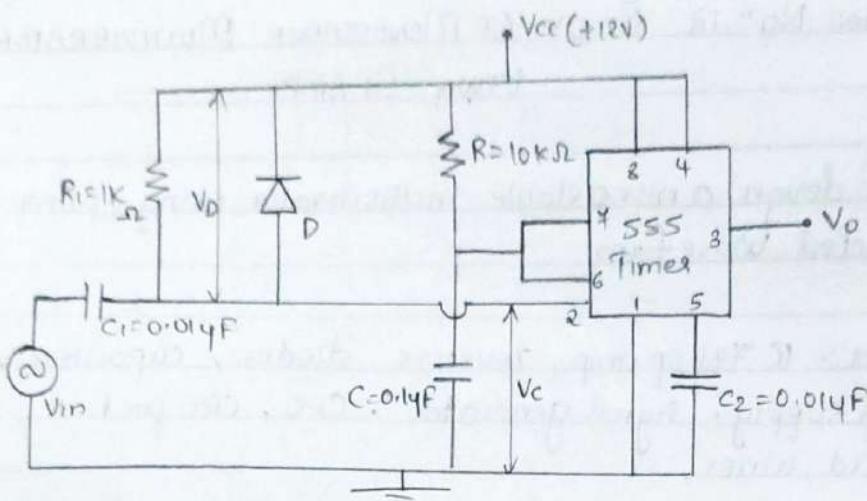
THEORY:- A monostable multivibrator produces a single pulse whose width can be controlled. It is also called 'one shot' since it produces one pulse for trigger input pulse. Monostable MV has one state stable & one quasi stable state. In the absence of trigger, the MV prefers to remain in its stable state. As a negative trigger is applied, MV switches from stable state to quasi stable

PROCEDURE:-
1) Check the 741 opamp & draw the expected output waveform.

- 2) Insert the IC on bread board & make connections as shown.
- 3) Give the probe at the output to CRO. Observe output waveform.
- 4) Give negative triggering pulse as input. Note output in CRO.
- 5) Plot the graph for the same in a suitable graph sheet & compare them with the theoretical graph.

RESULT:- The output of monostable multivibrator using opamp has been studied & verified.

MONOSTABLE MULTIVIBRATOR



Given $f = 1\text{kHz}$, $T = 1\text{ms}$

$$T = 1.1RC \quad \text{let } C = 0.014\text{F} \therefore R = 10k\Omega$$

$$f_{\max} = 10\text{kHz} \quad (\text{assume})$$

$$\therefore T_{\max} = 0.1\text{ms}$$

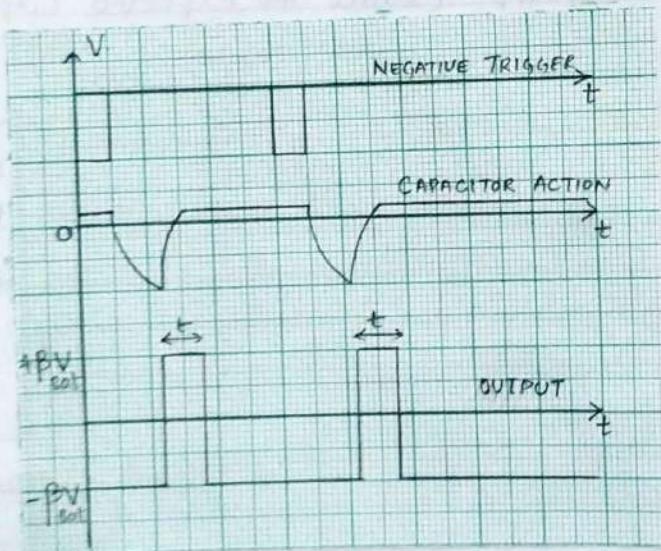
$$T_{\max} = R_1 C_1 (1.1)$$

$$\text{Assume } R_1 = 1k\Omega \therefore C_1 = 0.014\text{F}$$

$$\text{Since } C_1 = C_2 = 0.014\text{F}$$

Note:- Triggering must be done only after $(T_c + d\alpha)$

i.e
Input trigger $> (T_c + T_d)$



EXPERIMENT NO : 13 STUDY OF MONOSTABLE MULTIVIBRATOR USING 555 TIMER

Aim:- To design a monostable multivibrator using 555 timer & get the expected waveform

APPARATUS :- 555 timer, resistors, capacitors, diodes, regulated power supply, signal generator, CRO, CRO probes, breadboard, wires,

THEORY :- A monostable multivibrator produces a single pulse whose width can be controlled. It is also called 'one shot' since it produces one pulse & one for each trigger input pulse. Monostable MV has one stable state & one quasi stable state. In the absence of triggers, the MV prefers to remain in its stable state. As a negative trigger is applied the MV switches from state to quasi-stable

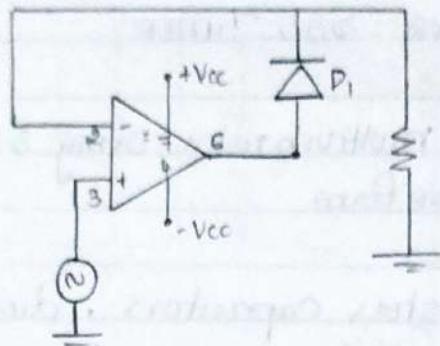
PROCEDURE:-

- 1) Check the 555 timer & draw the expected output waveform.
- 2) Insert IC on breadboard & do the connections.
- 3) Give the probe at output CRO. Observe the output.
- 4) Give negative triggering pulse as input. Note the output.
- 5) Plot the graph for the same in a suitable graph sheet & compare them with theoretical graph.

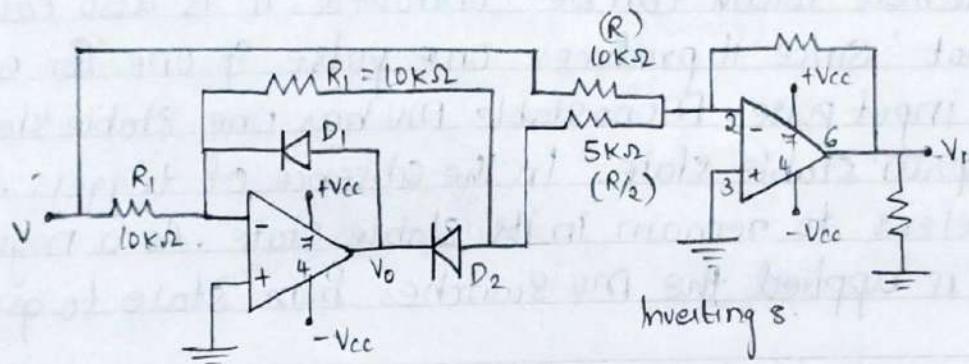
RESULT:- The output of monostable multivibrator using 555 timer has been studied & verified.

Teacher's Signature _____

HALF WAVE RECTIFIER



FULL WAVE RECTIFIER



EXPERIMENT NO.: 14 HALF WAVE AND FULL WAVE REC PRECISION RECTIFIERS

Aim:- To design & study precision rectifiers : full wave & half wave rectifiers

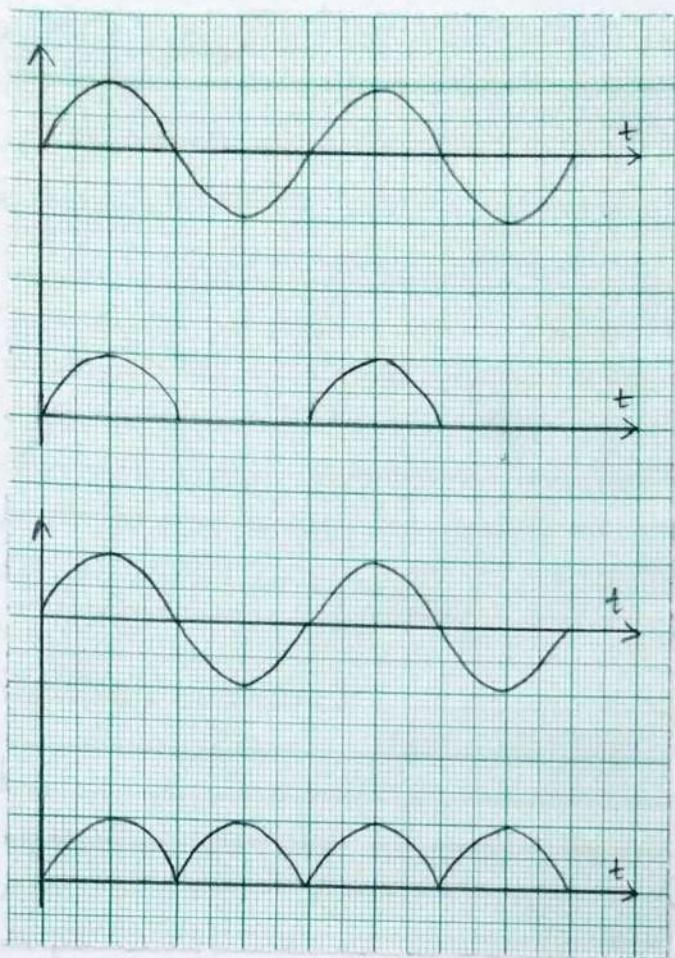
APPARATUS:- IC 741, normal diodes, resistors, signal generator, CRO, regulated power supply

THEORY :- Half Wave Rectifier.

A Half wave rectifier consists of AC signal to DC signal by passing either the -ve or +ve half cycle of waveform & blocking the other half wave. It can be easily constructed using only one diode but are less efficient than full wave rectifier.

Full Wave Rectifier.

A full wave rectifier is defined as a rectifier that converts the complete cycle of alternating current into pulsating Direct current. Unlike half wave rectifiers that utilises only the half wave of the i/p AC cycle, Full wave rectifiers utilize the full cycle.



Half Wave
Rectifier

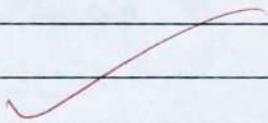
Volt - Phasor
Half A
→ primary pd
→ primary I
→ pipe flow
difference
Full Wave
Rectifier



Expt. No.:

PROCEDURE :-

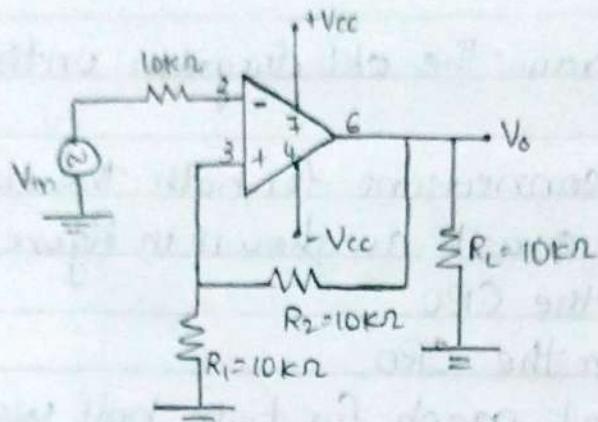
- 1) Check 741 opamp & draw the ckt diagram on the bread board.
- 2) Make the necessary connections for both the half wave & full wave rectifier circuit as shown in figure.
- 3) Connect the probes to the CRO.
- 4) Observe the output on the CRO.
- 5) Plot the input and output graph for both half wave & full wave rectifiers.



Result:- Precision Rectifier - full wave rectifier & half wave rectifiers are implemented & studied successfully.

Teacher's Signature _____

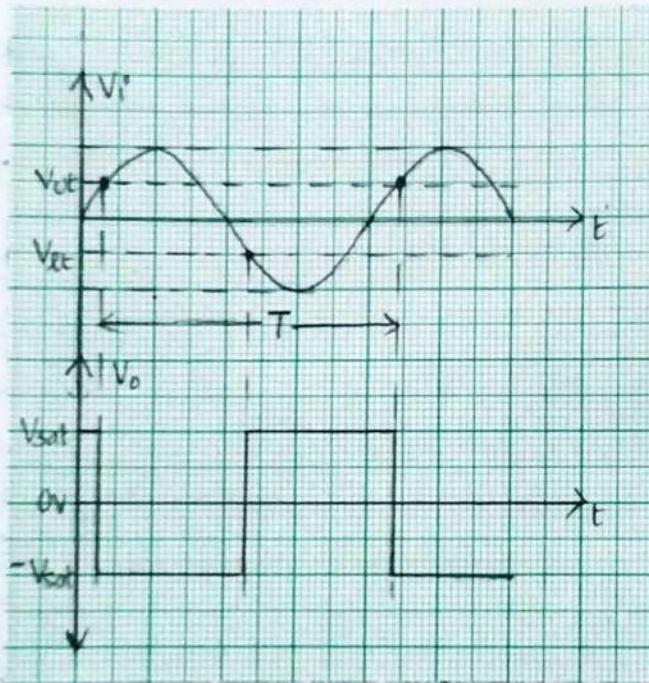
SCHMITT TRIGGER



$$V_{ce} = +15V$$

$$V_{in} = 10V$$

~~$$V_{UL} = \frac{R_1}{R_1 + R_2} V_{cc}$$~~



EXPERIMENT NO: 15 · SCHMITT TRIGGER.

Aim:- To construct an op-amp for study of Schmitt triggers for specified UTP & LTP.

APPARATUS:- IC-741, resistors, regulated power supply, signal generator, connecting wires.

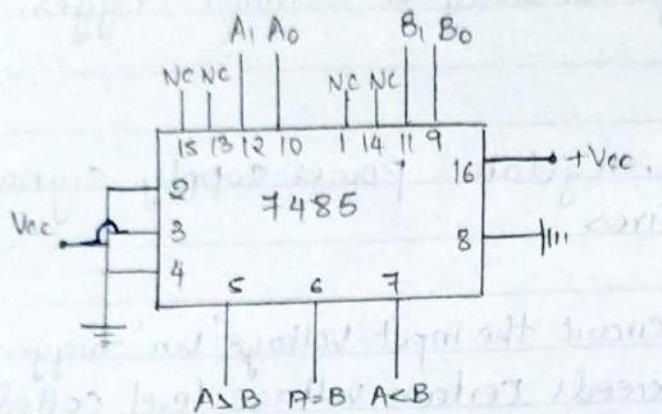
THEORY:- In the Schmitt trigger circuit the input voltage ' V_{in} ' triggers the output ' V_o ' everytime it exceeds certain voltage level called upper threshold voltage ' V_{UT} ' & lower threshold voltage ' V_{LT} '.

PROCEDURE:- i) Check 741 opamp and draw the expected o/p wave form.

- 2) Insert the IC in the breadboard & make the connections as shown in fig. using connecting wires.
- 3) Connect the probes at o/p of CRO. Observe the o/p on CRO.
- 4) Note the o/p. record your observation.

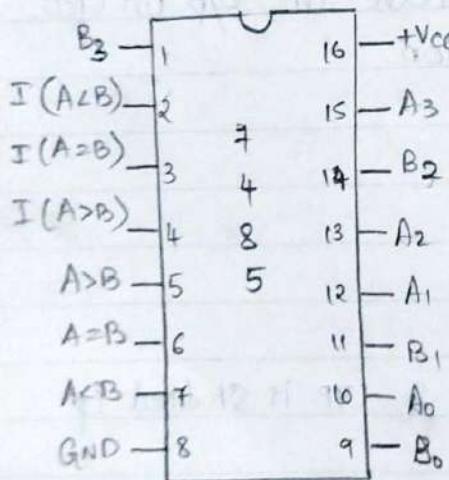
RESULT:- Schmitt Trigger for specified UTP & LTP is studied & implemented successfully.

2 BIT COMPARATOR



TRUTH TABLE						
INPUTS				OUTPUTS		
A ₁	A ₀	B ₁	B ₀	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

PIN DIAGRAM (IC 7485)



EXPERIMENT NO. 16 REALISATION OF A 2 BIT COMPARATOR USING 7485 IC

Aim: To design & implement a 2 bit comparator using a 7485 IC.

APPARATUS: IC 7485, Trainer kit, Patch Cards.

THEORY: Magnitude comparator is a logical circuit, which compares two signals $A \& B$ & generates three logical outputs whether $A > B$, $A = B$ or $A < B$. IC 7485 is a high speed 4 bit magnitude comparator, which compares 2 4 bit words. The $A = B$ input must be held high for proper compare operation.

PROCEDURE:-

- 1) Truth Table for a comparator (2-bit) is to be written.
- 2) Insert the IC into the slot provided in the kit.
- 3) Using the patch cards do the necessary connections.
- 4) +5V DC is provided to IC.
- 5) Switch ON the kit.
- 6) Give different inputs & check for the outputs by referring to the truth table.

RESULT: A 2 bit comparator using 7485 IC have designed & implemented.

Q3/10/2025

Teacher's Signature _____