

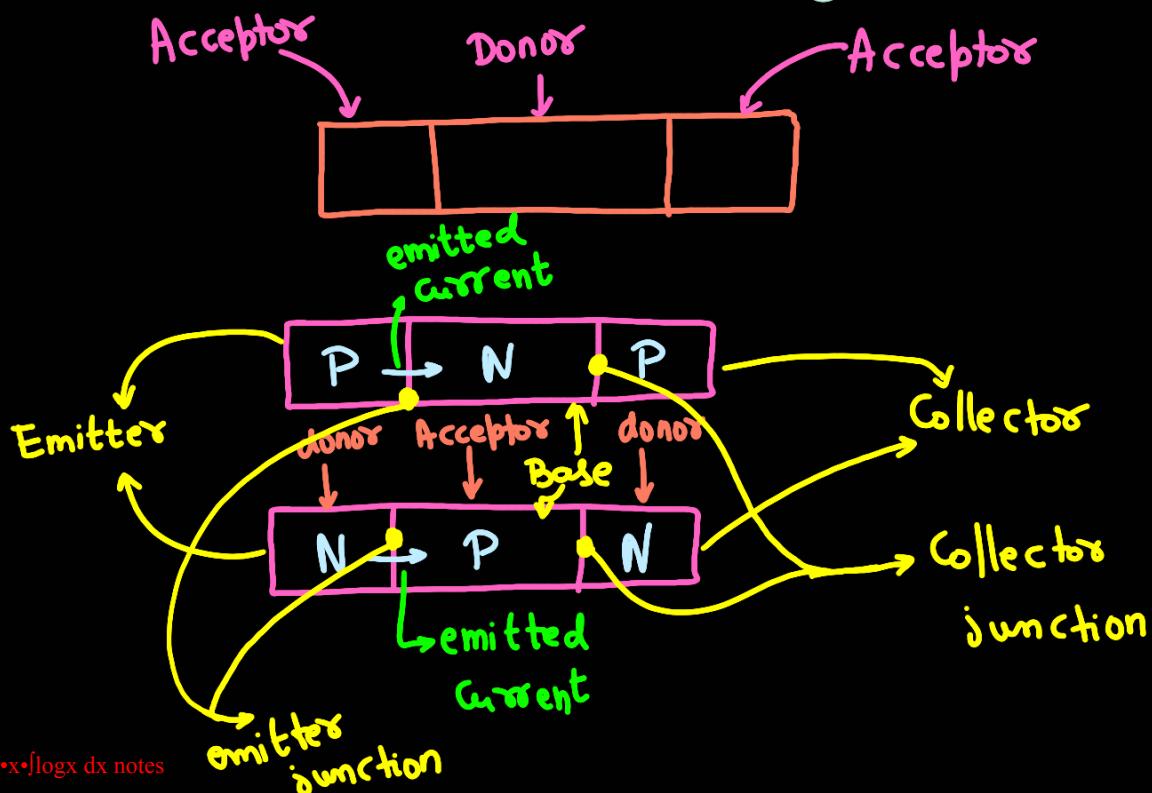
$$\text{Gain} = \frac{\text{O/P}}{\text{I/I P}}$$

★ Transistor

→ Single crystal made of Si or Ge

→ Crystal is continuous, such that 2 junctions are formed

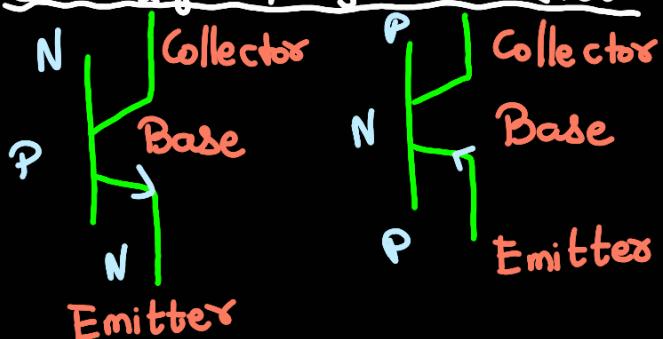
→ Can be either PNP or NPN



* There are three regions in transistor :-

- ① Emitter :- Provides large numbers of charge carriers. Heavily doped and moderately sized
- ② Base :- Very thin & lightly doped
- ③ Collector :- Large in size & moderately doped

Ckt symbol of transistor :-



N-P-N
transistor

P-N-P transistor

Note :
Arrow always
in dirn of
forward
Bias,
i.e. from
P to N

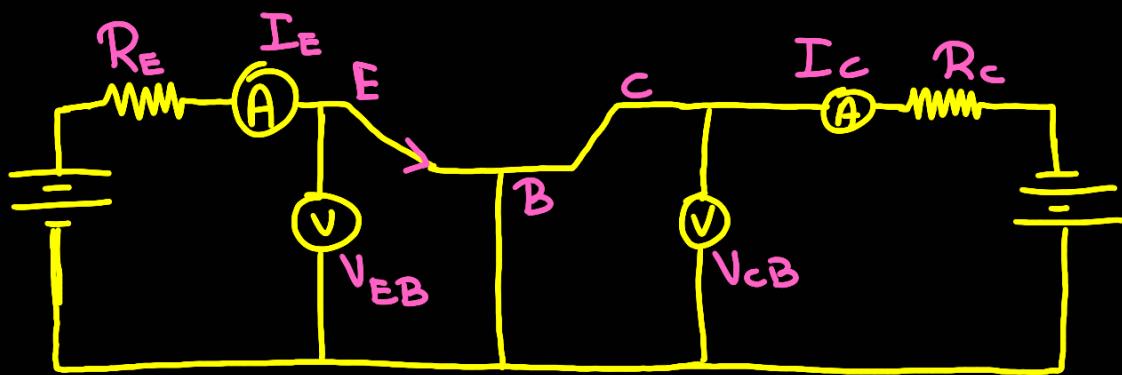
Transistor Configurations :-

- ① Common Base (CB)
- ② Common Emitter (CE)
- ③ Common Collector (CC)

4 H Parameters:
Input Impedance
Reverse Voltage Ratio
&
Output Admittance
Forward Current Gain

$\{ I/P$
 $\} O/P$

Common Base (CB) Configuration:-



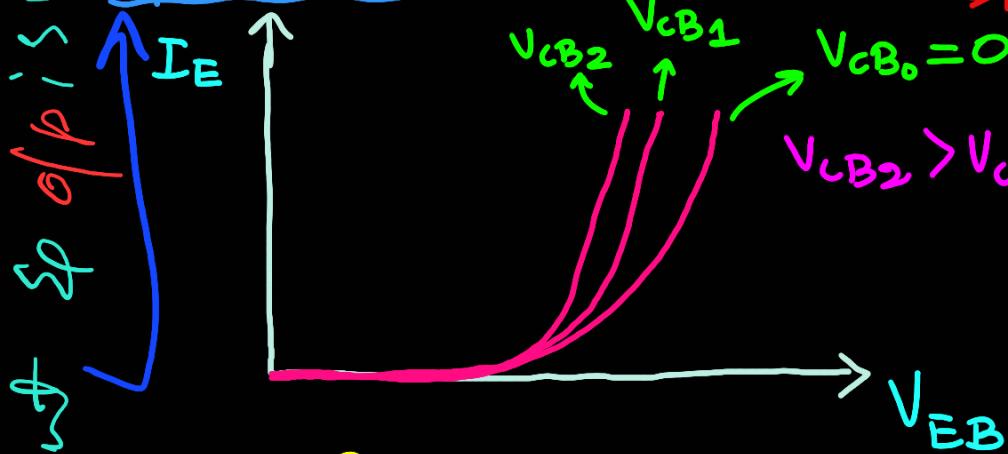
Input Circuit
(V_{EB} , I_E)

Output Circuit
(V_{CB} , I_C)

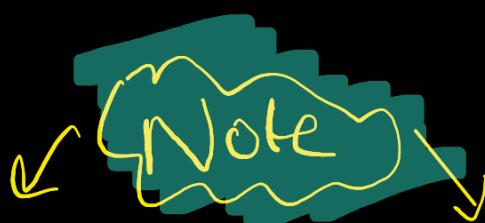
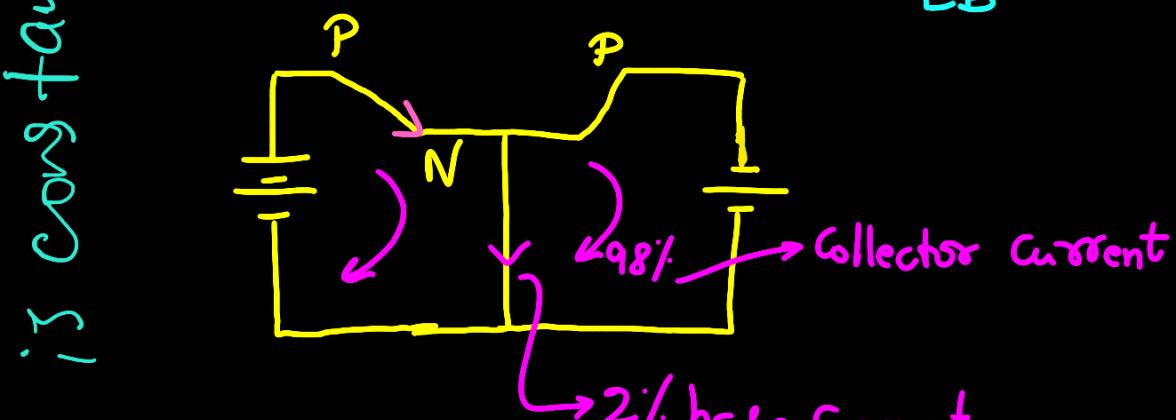
I/P characteristics

O/P characteristics

* I/P characteristics:-



input characteristics
is constant & p of p



Emitter $\delta^n \rightarrow$ F.B ;

Collector δ^n is reverse biased

I/P resistance

$$R_I = \frac{V_{EB}}{I_E} \quad \left|_{V_{CB}} \quad \delta_i = \frac{\Delta V_{EB}}{\Delta I_E} \right|_{V_{CB}}$$

Static

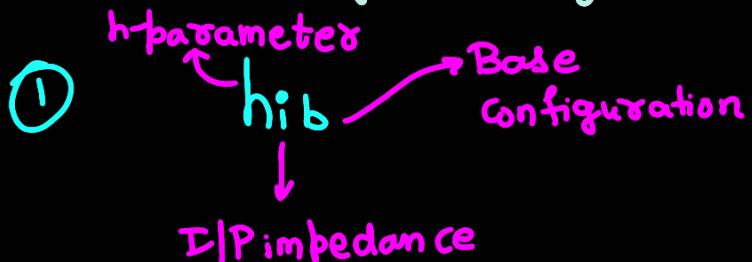
Dynamic

I/P
resistance

I/P impedance

h-parameters:-

↳ A way of measuring → alternative for ohm's law



$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E} \quad \left|_{V_{CB}} \right.$$

② Reverse voltage ratio (h-parameters)

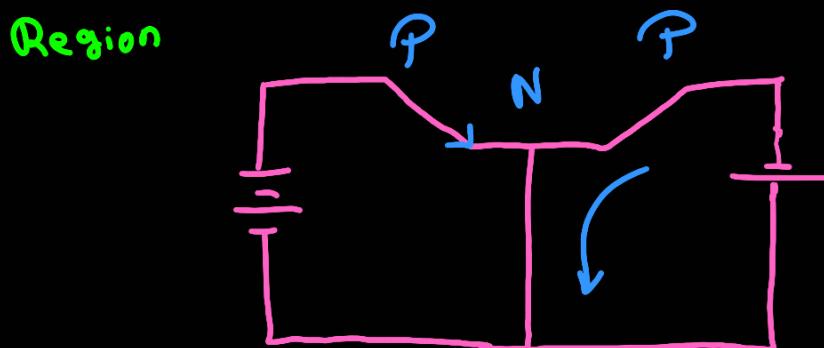
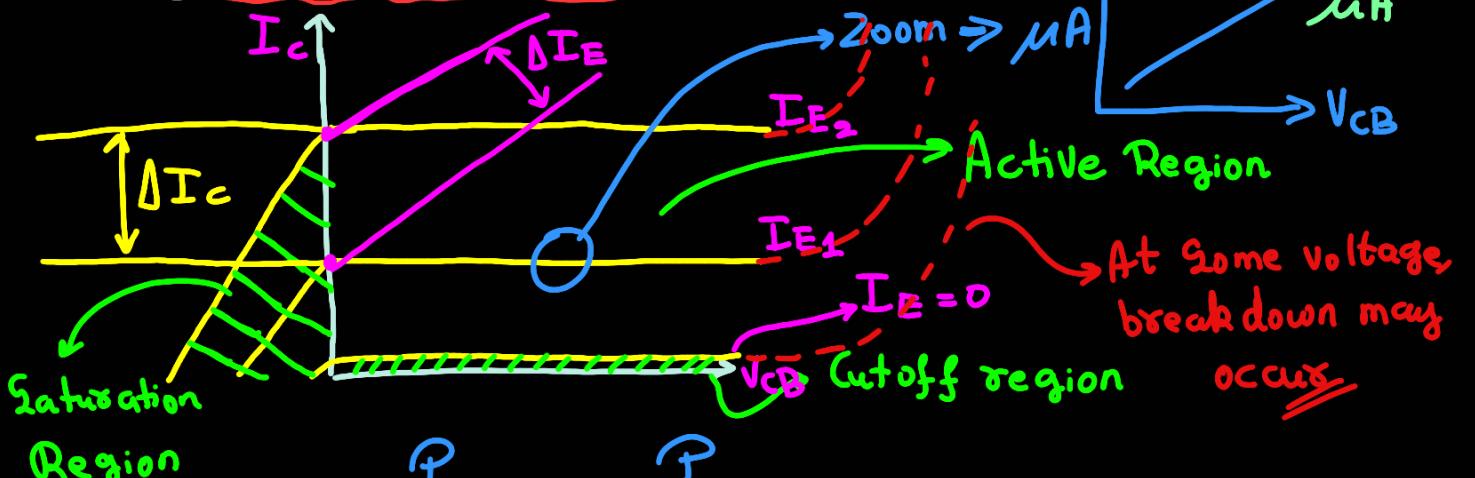
$h_{\sigma b}$ \rightarrow Common base configuration
reverse voltage ratio

$$\frac{O/P}{I/P}$$

But here
∴ reverse ratio
its $\frac{I/P}{O/P}$

$$h_{\sigma b} = \frac{\Delta V_{EB}}{\Delta V_{CB}} \quad \left|_{I_E} \right.$$

Output characteristics:-



① O/P impedance

$$R_o = \left. \frac{V_{CB}}{I_c} \right|_{I_E}$$

① $h_{ob} = \left. \frac{\Delta I_c}{\Delta V_{CB}} \right|_{I_E}$

O/P admittance Common base configuration

In off char O/P is constant if f/p keeps on varying.

② $h_{fb} = \left. \frac{\Delta I_c}{\Delta I_E} \right|_{V_{CB}} = \alpha \rightarrow AC$

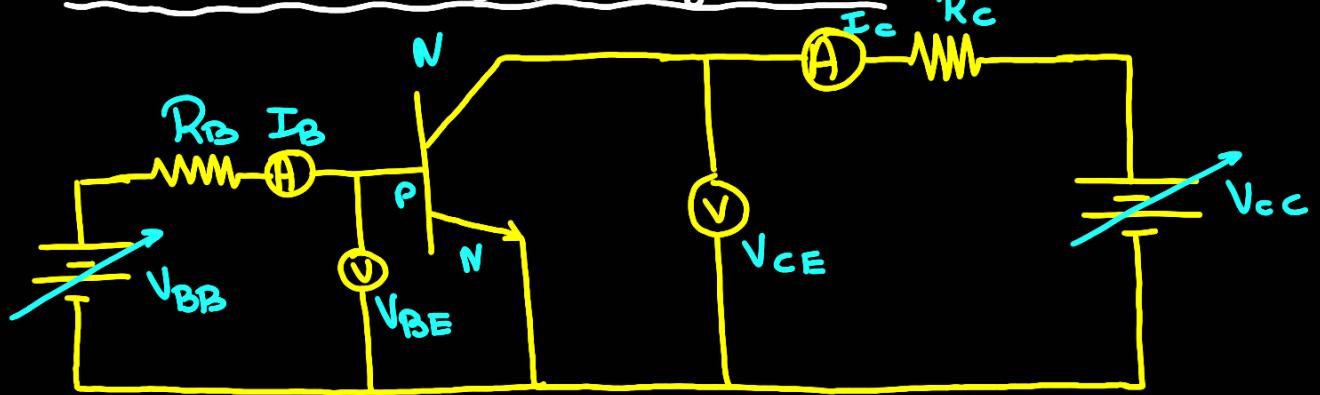
forward current gain Common Base config

Output current
Input current

$$\alpha_{DC} = \frac{I_c}{I_D}$$

Output
Input

Common Emitter (CE) Configuration :-



I/P ckt
(V_{BE} , I_B)

O/P ckt
(V_{CE} , I_C)

Emitter jn is F.B
Collector jn is R.B

★ Input Characteristics

I_B

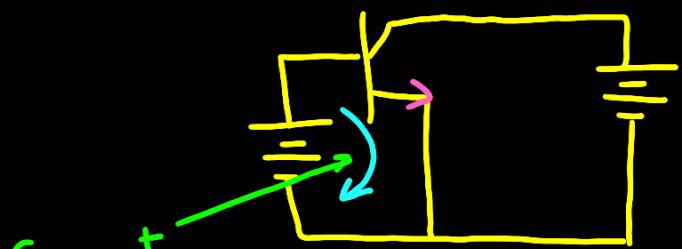
$V_{CE}=0$

V_{C2} V_{C1}

$\{V_{C2} > V_{C1} > V_{CE0}\}$

graph goes forward as O/P \uparrow ,

(Unlike CB, where graph goes backward)



Current flow dia
h-parameter

$$\textcircled{1} \quad h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \Big|_{V_{CE}}$$

I/P impedance

(E config)

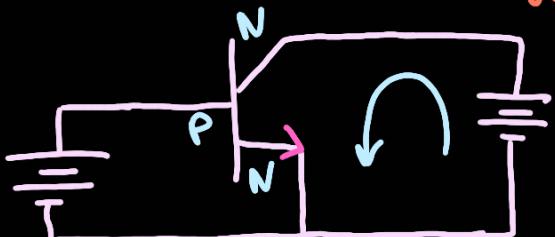
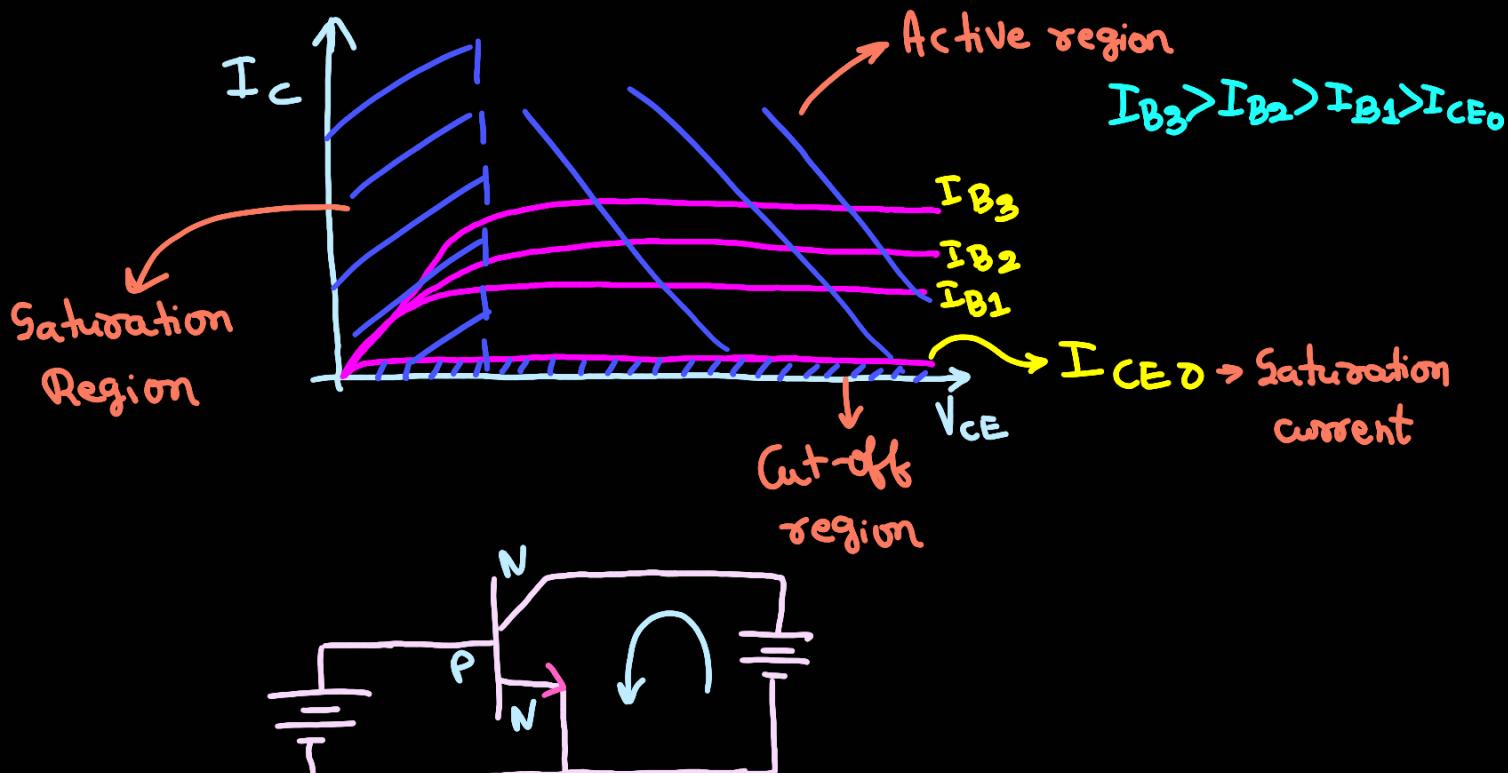
h-parameter

$$\textcircled{2} \quad h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \Big|_{I_B}$$

reverse voltage ratio

(E config)

★ Output characteristics :-



$$\textcircled{1} \quad h_{oe} = \left. \frac{\Delta I_C}{\Delta V_{CE}} \right|_{I_B} \quad \textcircled{2} \quad h_{fe} = \left. \frac{\Delta I_C}{\Delta I_B} \right|_{V_{CE}} = \beta$$

Annotations:
 ① \downarrow O/P admittance
 ② forward current gain

Relation b/w d & β :-

$$\text{W.K.T : } I_E = I_B + I_C \quad \text{throughout}$$

$$I_E = I_B + I_C$$

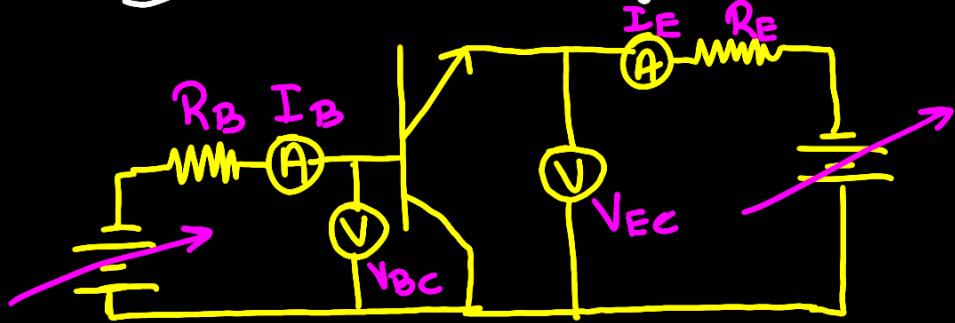
$$I_C \quad I_C \quad I_C$$

$$\Rightarrow \frac{1}{d} = \frac{1}{\beta} + 1$$

$$d = \frac{I_C}{I_E} \quad \beta = \frac{I_C}{I_B}$$

Required relation

Common Collector Configuration :-

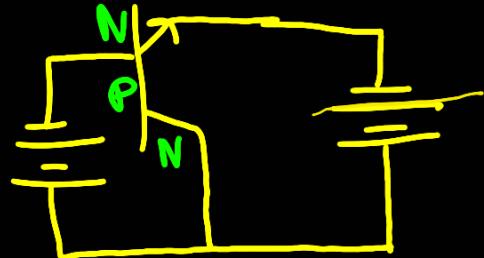
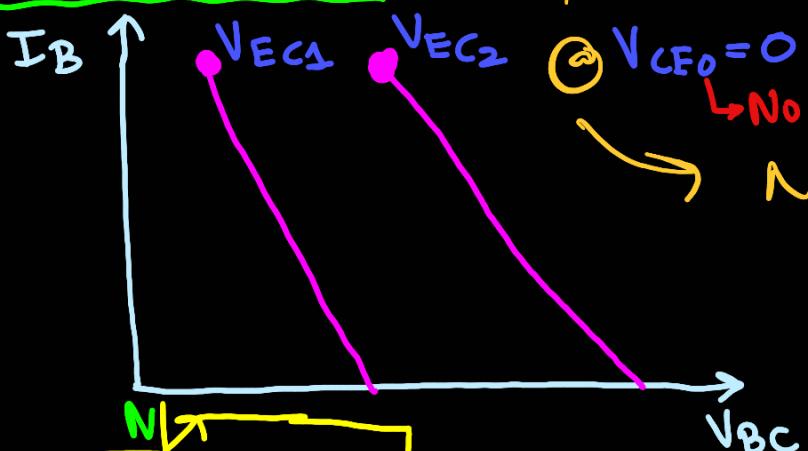


I/P ckt
 V_{BC}, I_B

O/P ckt
 V_{EC}, I_E

β

I/P characteristics:-



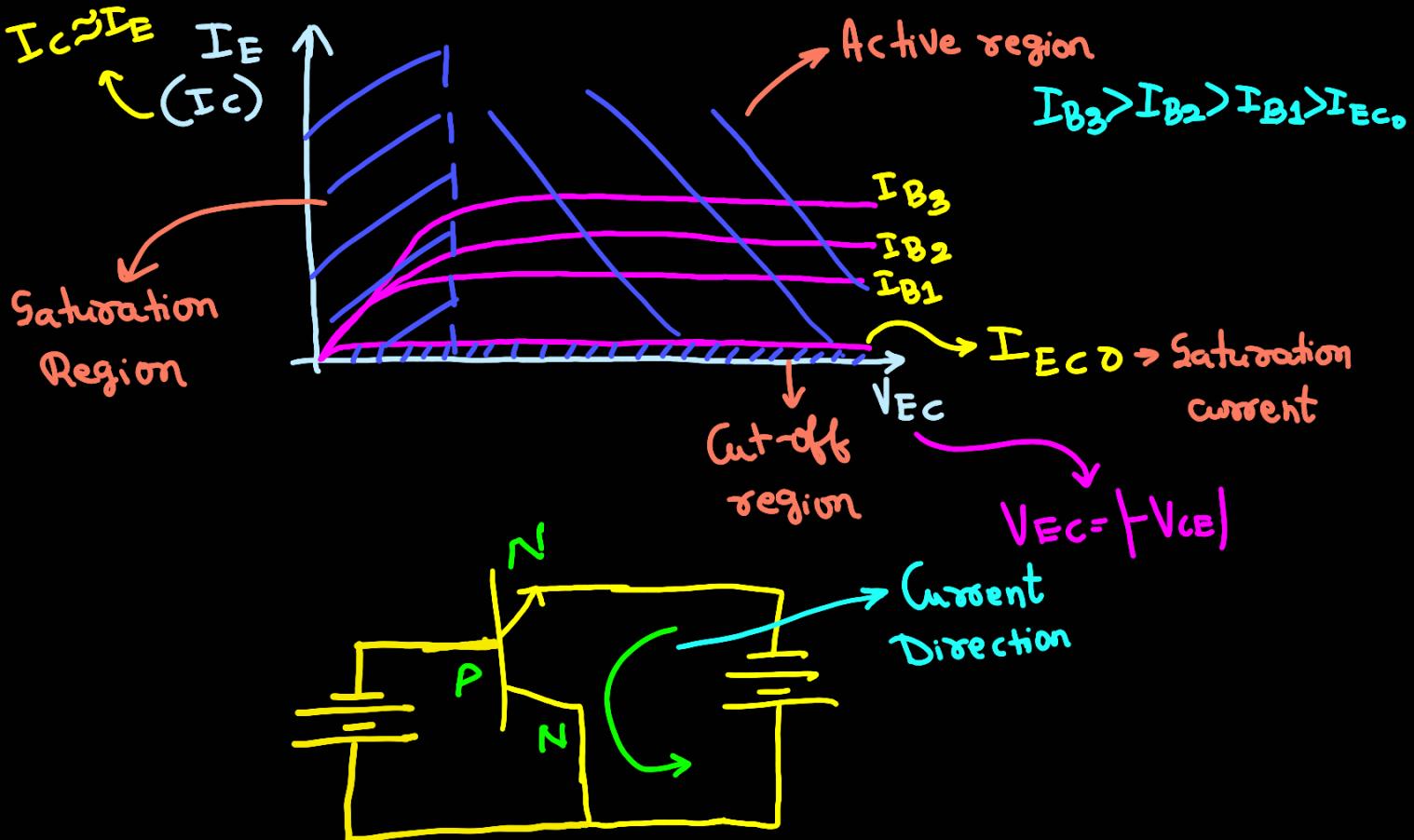
$$\textcircled{1} h_{ic} = \left. \frac{\Delta V_{BC}}{\Delta I_B} \right|_{V_{EC}}$$

I/P impedance

$$\textcircled{2} h_{oc} = \left. \frac{\Delta V_{BC}}{\Delta V_{EC}} \right|_{I_B}$$

Reverse voltage ratio

* O/P characteristics:-



$$\textcircled{1} h_{oc} = \left. \frac{\Delta I_E}{\Delta V_{EC}} \right|_{I_B}$$

OP admittance

$$\textcircled{2} h_{fc} = \left. \frac{\Delta I_E}{\Delta I_B} \right|_{V_{EC}}$$

forward current gain

* Relation b/w α , β , γ :

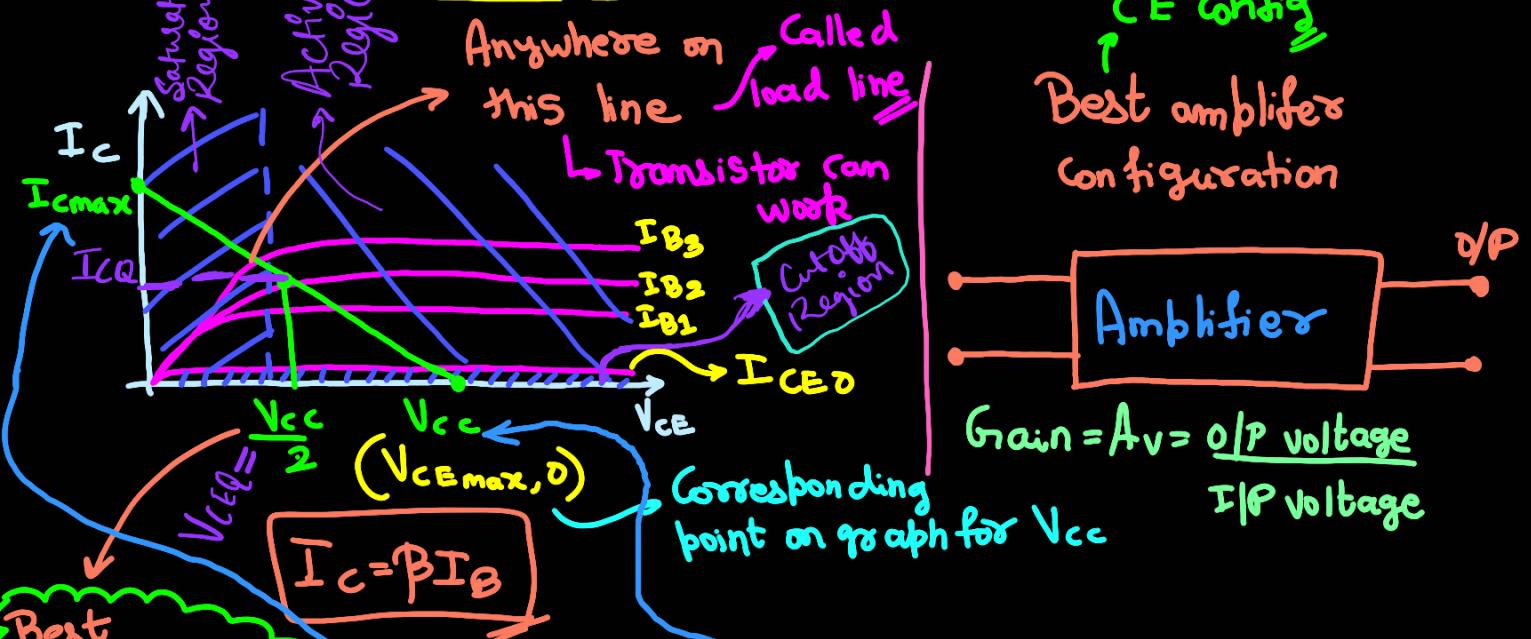
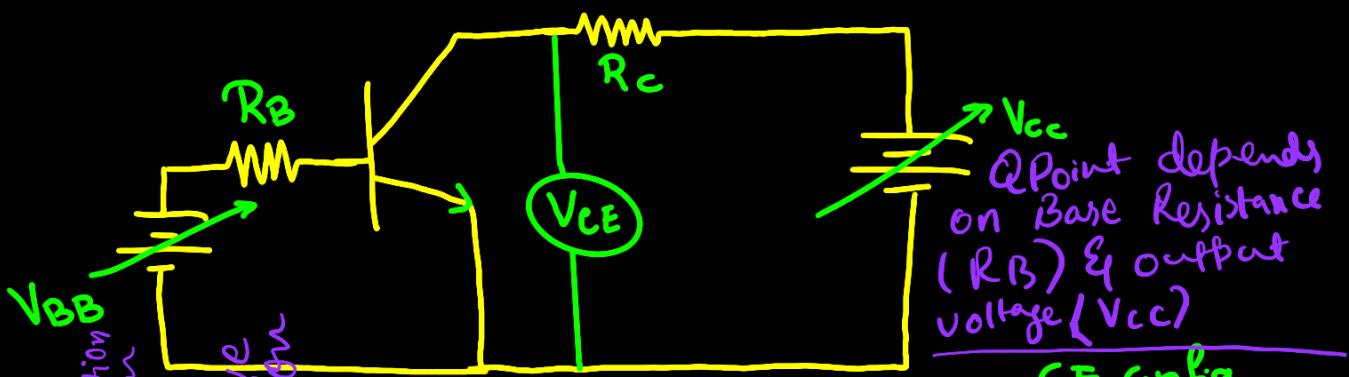
$$\gamma = \beta + 1$$

$$\gamma = \frac{1}{1-\alpha}$$

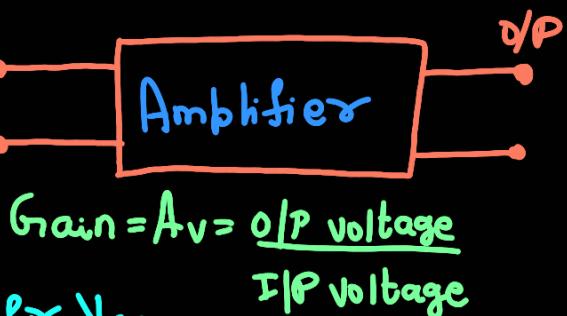
*Derivation not necessary

DC analysis:-

Consider CE Configuration & its O/P characteristics



Best amplifier configuration

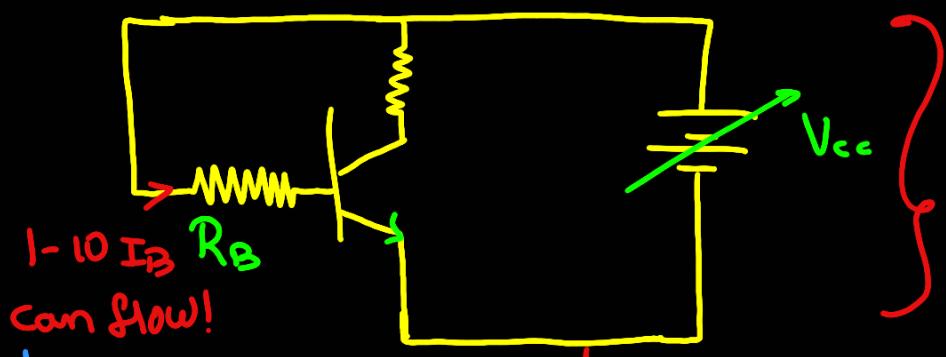


Must be very stable!!

★ Transistor can work as an amplifier b/w these two points (V_{cc} & $I_{c max}$)

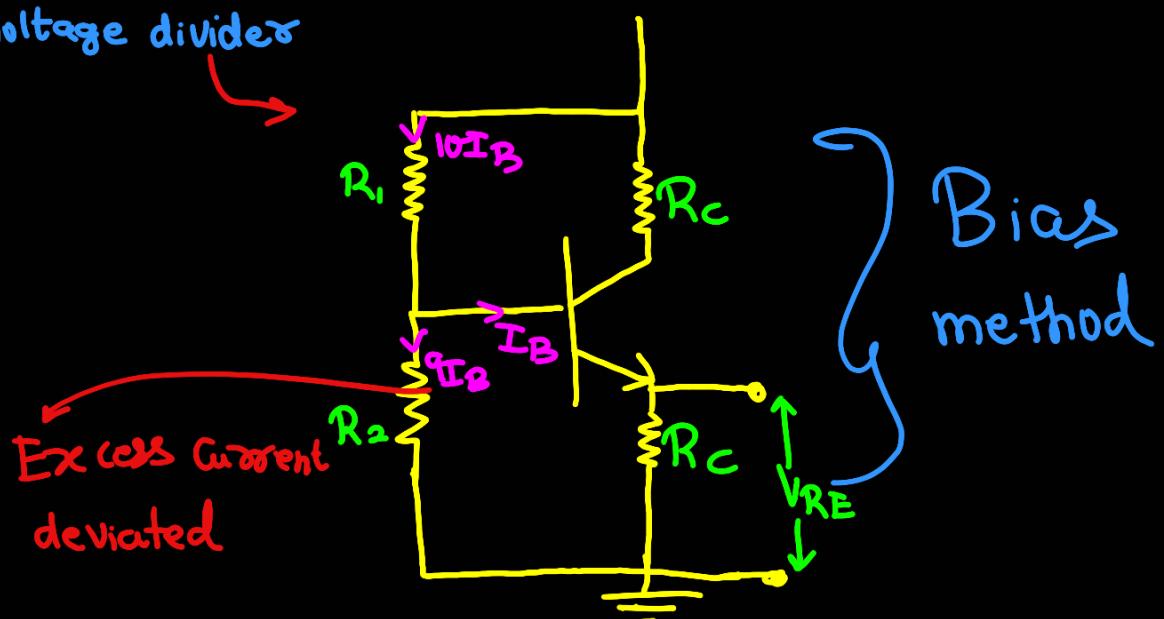
★ Load Line:- Locus of the transistor operating points

$$V_{ceQ} = \frac{V_{cc}}{2}; I_{cQ} = I_c$$



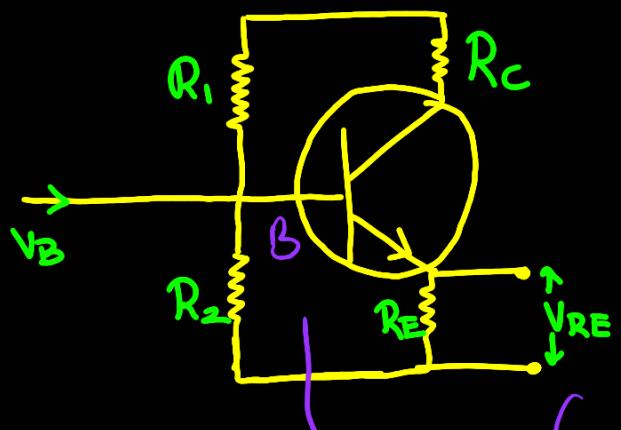
Due to ripple from rectifier O/P, $I_B \& I_c$ can vary accordingly

To avoid ξ , maintain constant I_B in Base, add voltage dividers



Bias method

Bias method:-



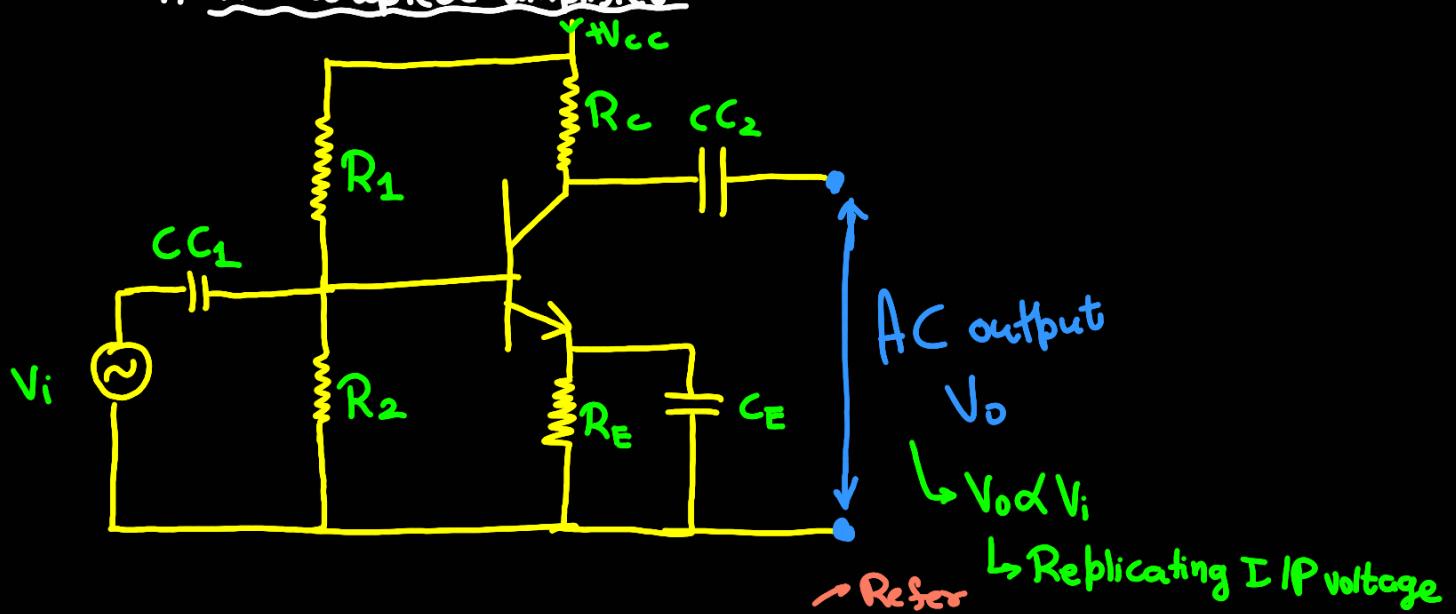
Common Emitter Configuration

$$R_B = \frac{R_1 + R_2}{R_1 R_2}$$

Functions :-

- i) R_C :- Limit Collector current; Act as load resistor
- ii) $R_1 \& R_2$:- AC biasing resistors (Voltage divider bias)
- iii) R_E :- Emitter resistor used for stabilising Q point

RC coupled amplifier :-



Functions:- ① R_C ② $R_1 \& R_2$ ③ R_E Bias method on top

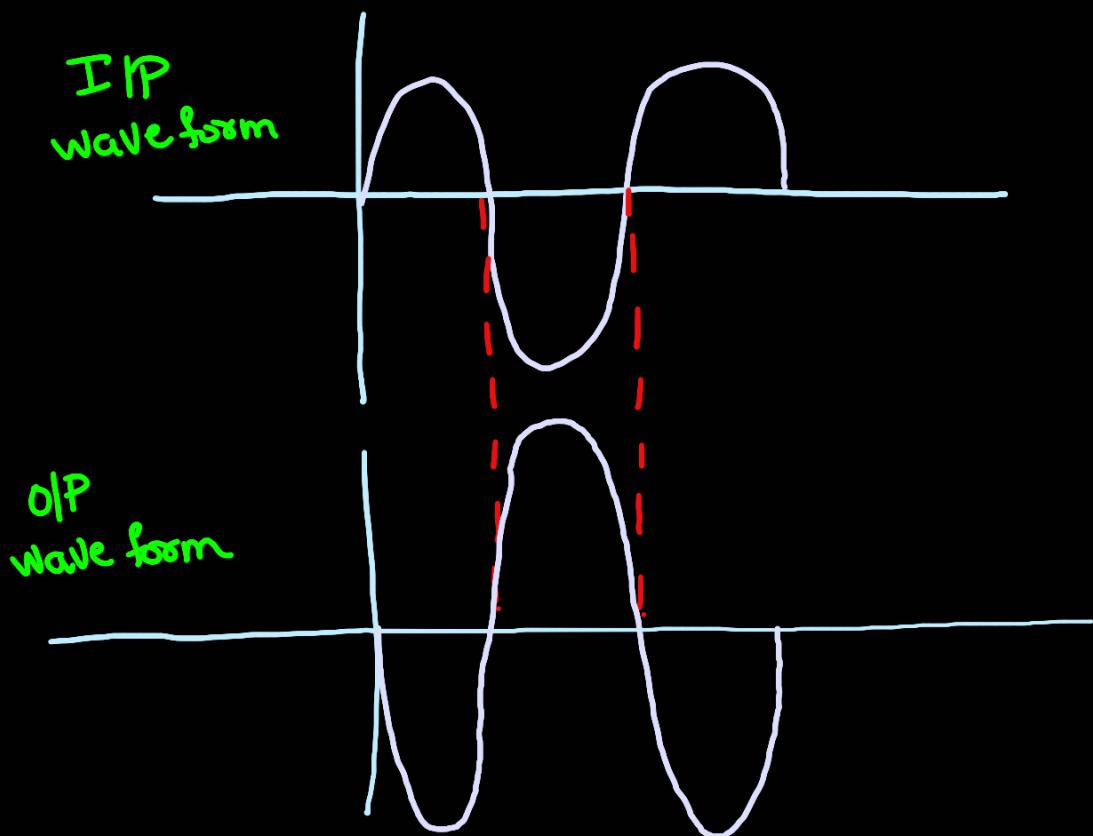
④ $CC_1 \& CC_2$:- Coupling capacitors; Blocks DC voltage and allow only AC voltage & improve AC gain

⑤ C_E :- Bypass Capacitor acts as shunt across R_E

$$\text{Voltage gain} = A_v = \frac{V_o}{V_i} \Rightarrow V_o = A_v V_i$$

∴ O/P voltage V_o is A_v times the input voltage V_i

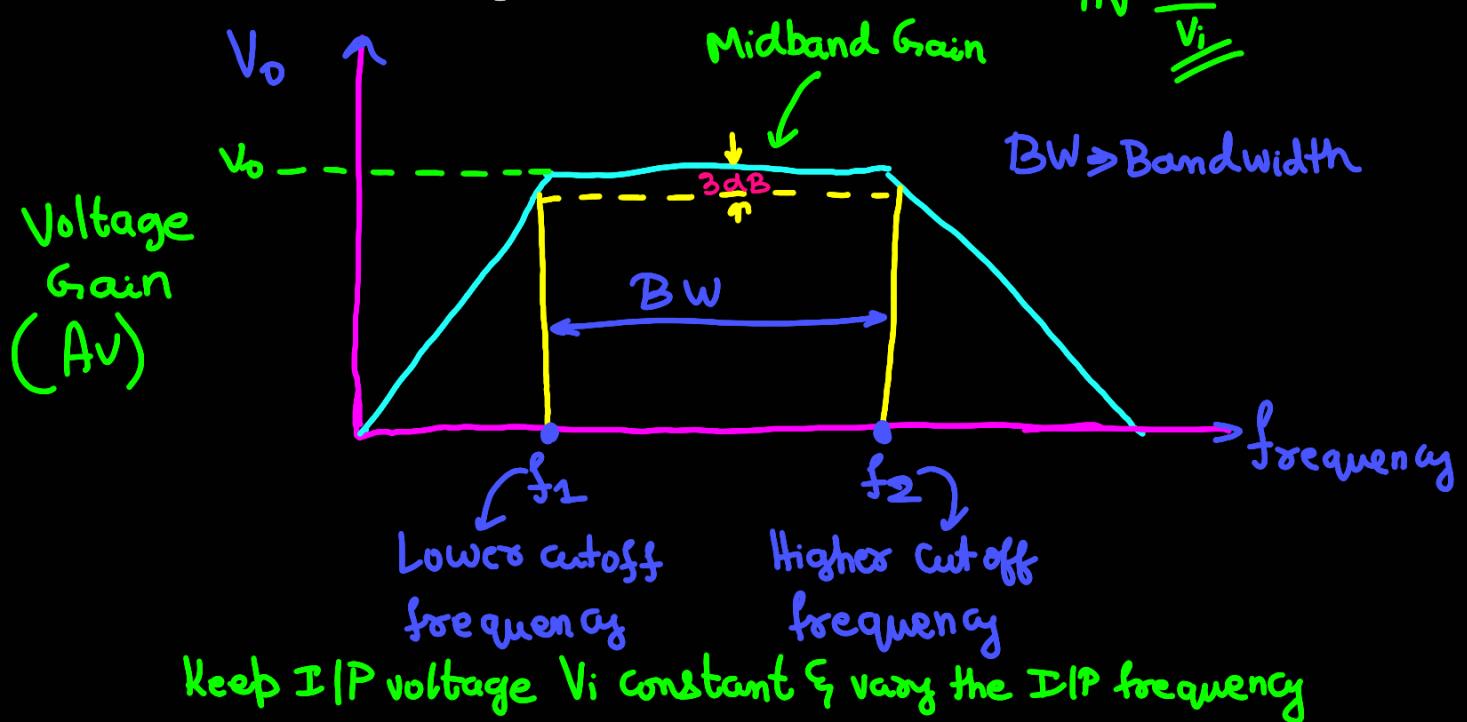
* Waveforms:-



O/P is out of phase by 180°

$$I/P \uparrow \Rightarrow O/P \downarrow$$

* Understanding frequency response:-



DC is blocked by capacitor. At 0 frequency, there is 0 O/P voltage.

$$X_C = \frac{1}{2\pi f C} \Rightarrow X_C \downarrow \Rightarrow f \uparrow$$

Increase in frequency, reactance reduces, O/P voltage increases

At one point it stabilizes at V_0 for a certain frequency range called Bandwidth.

For a larger BW, we sacrifice gain and Vice-Versa

$$A_v(\text{dB}) = 20 \log_{10} \frac{V_o}{V_i} \text{ dB}$$

Voltage gain in dB

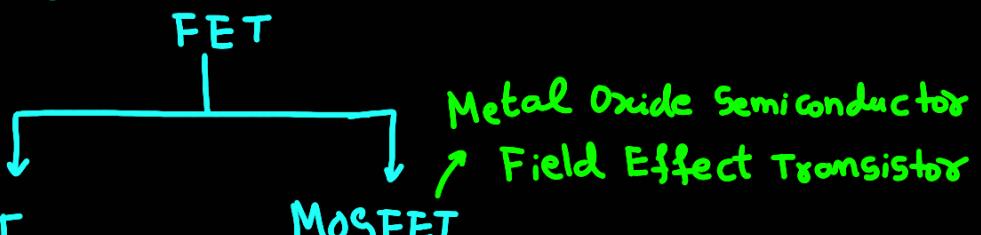
A.K.A midband gain

Gain Bandwidth Product = GBW

$\Rightarrow GBW = A_v \times BW$ } for a given amplifier, GBW is constant

Junction Field Effect Transistor (JFET) :-

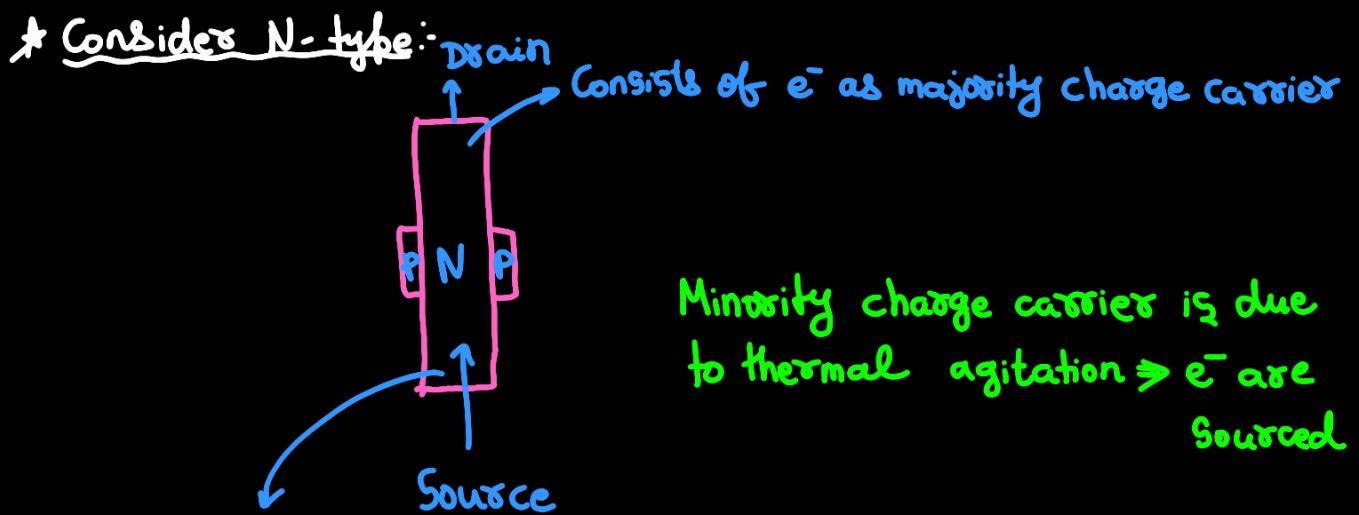
Simply referred to as FET



* JFET: Consist of silicon semiconductor bar either N-type or P-type with opposite type of semiconductor material diffused on either side of the bar.

i.e. for N-type bar \rightarrow P-type is diffused

for P-type bar \rightarrow N-type is diffused



Minority charge carrier is due to thermal agitation $\Rightarrow e^-$ are sourced

e^- move in one dirⁿ based on biasing
but always from -ve to +ve

Semiconductor bar consist of two terminals

* Source
* Drain

P-type diffused to the bar forms a terminal called "gate"

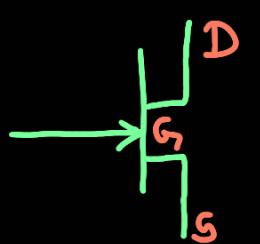
\therefore JFET is a three terminal device consisting of source, drain & gate

e^- move from source to drain when proper voltage is applied b/w source & drain.

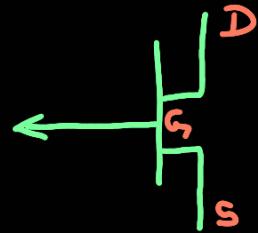
\downarrow \downarrow
 -ve +ve
 Voltage Voltage

* JFET is either N-channel or P-channel
(The bar is the channel)

Circuit symbol for JFET:-



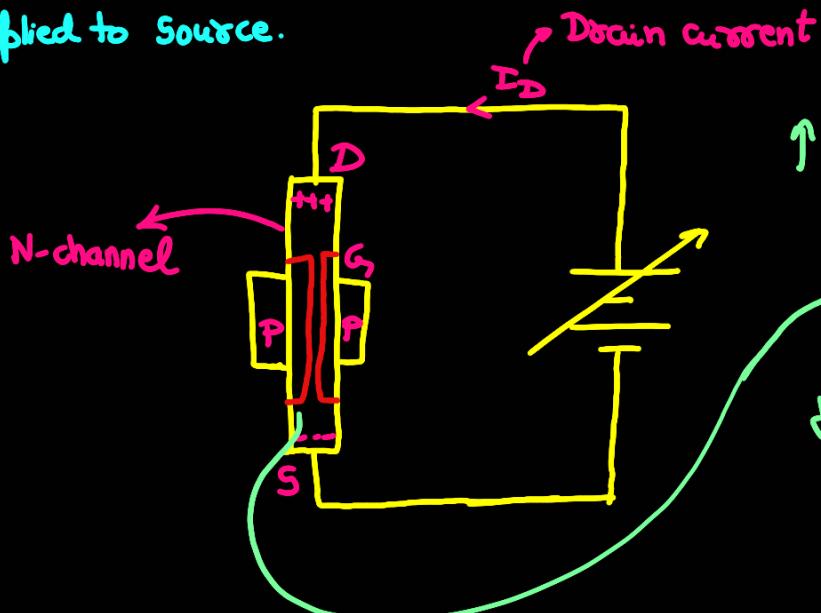
N-channel FET



P-channel FET

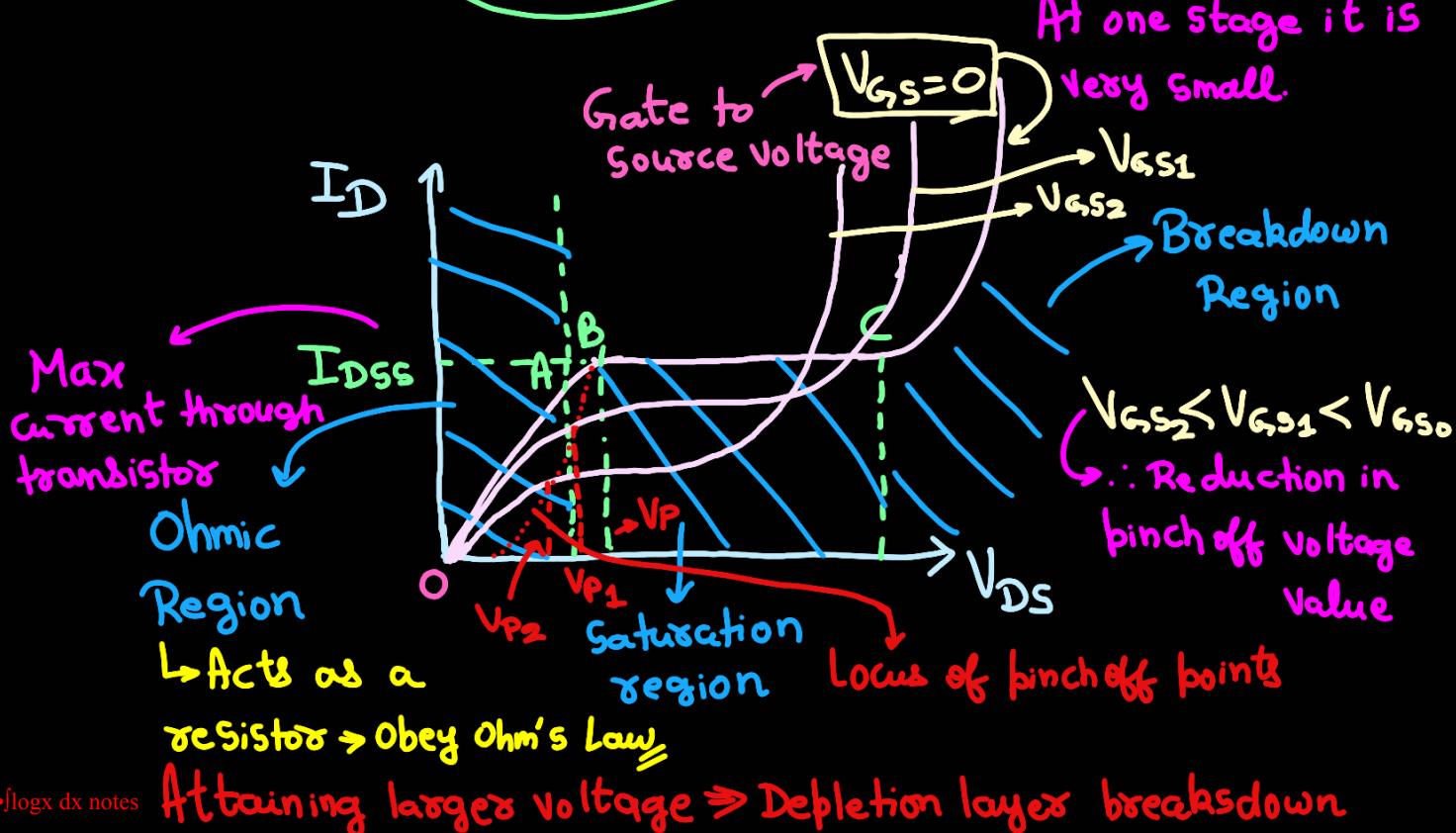
Characteristics of JFET:-

Consider N-channel FET, +ve voltage applied to drain, -ve voltage applied to Source.



→ O/P characteristics

$\uparrow e^-$ in voltage \rightarrow more e^- near Drain
 Depletion region formed penetrates through channel \downarrow
 (conducting path reduces)



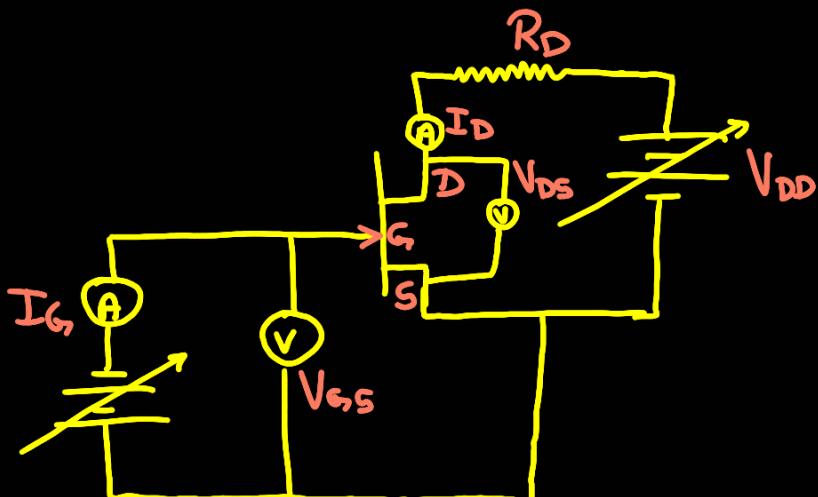
∇V to A \rightarrow Ohmic Region

∇V A to B \rightarrow Drain keeps decreasing because of depletion region b/w gate & drain

∇V At B, drain current is pinched off.

Point B is called Pinchoff point

The drain to source to source voltage (V_{DS}) at B is Pinchoff Voltage



Therefore, there is no I/V characteristics

$I_G = 0$ as P-N junction here is operated in reverse bias
Only a very small negligible saturation current flows which is ≈ 0

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Amplification factor

Transfer characteristics of JFET:-

Remember!!

$$V_P = V_{GS0}$$

V_P

$-V_{GS}$

I_D

I_{DSS}

I_{D1}

Operating points

V_{GS}

* O/P resistance = $\gamma_d = \frac{\Delta V_{DS}}{\Delta I_D}$
 (From O/P char)

* Transconductance (g_m) = $\frac{I_D}{V_{GS}}$

* Transconductance (g_m) = $\frac{\Delta I_D}{\Delta V_{GS}}$

$$\begin{aligned} \therefore \mu &= \frac{\Delta V_{DS} \times I_D}{\Delta V_{GS} \quad I_D} \\ &= \frac{\Delta V_{DS} \times \Delta I_D}{\Delta I_D \quad \Delta V_{GS}} \\ &\downarrow \quad \downarrow \\ &\gamma_d \quad g_m \end{aligned}$$

$\therefore \mu = \gamma_d \cdot g_m$

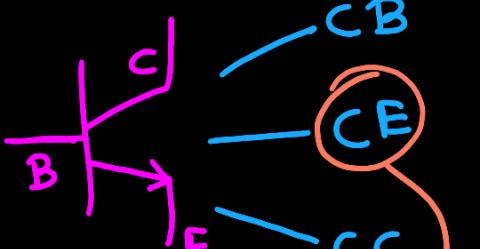
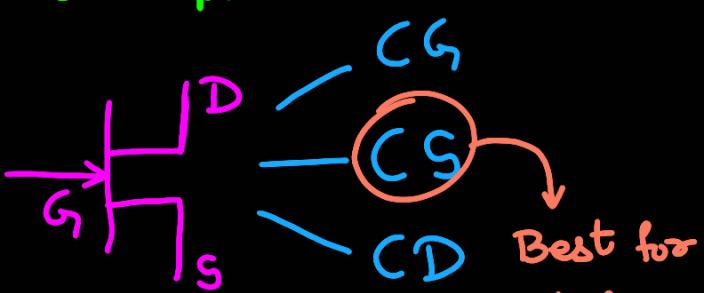
Current Equation of JFET:-

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

To remember

$$\begin{aligned} V_{DS} &= V_{DD} - I_D (R_s + R_D) \\ V_{GS} &= -V_S = I_S R_S = I_D R_S \\ V_{DS} &= V_D - V_S \end{aligned}$$

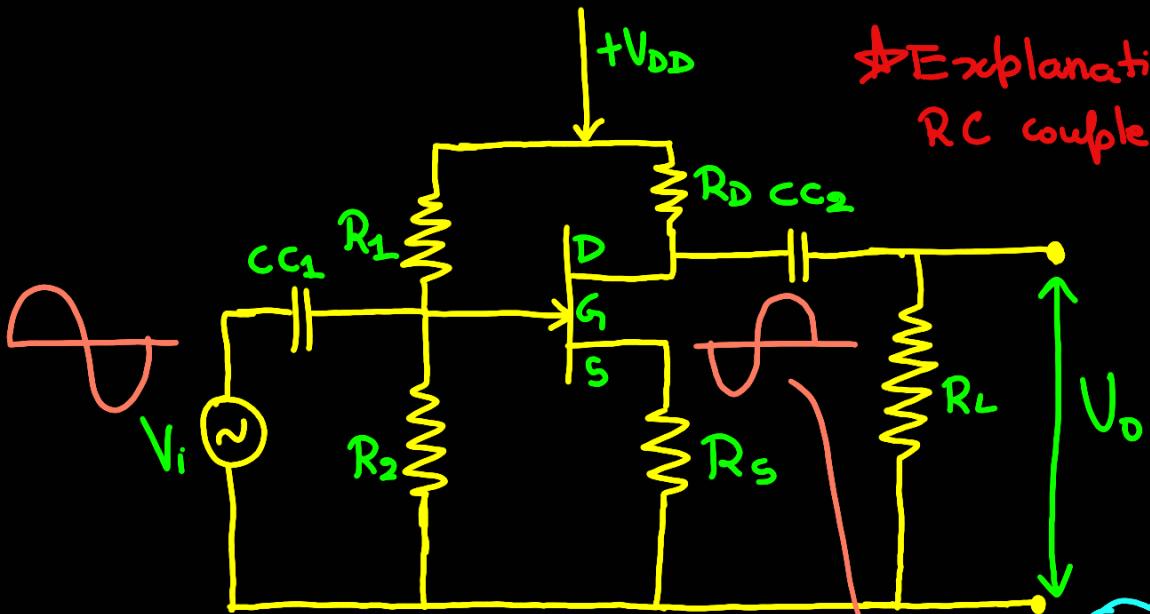
Difference b/w BJT & JFET:-

BJT	FET
* Current operated device	* Voltage operated Device
* Both majority & minority carriers are used for conduction Thus "Bipolar"	* Only majority carriers are used for conduction Thus "Unipolar"
 Best for amplifiers	 Best for amplifiers

CS amplifier:-

Common Source amplifier

↳ Gate to Source Reverse Bias



*Explanation Same as
RC coupled CF

$$I_D = I_S$$

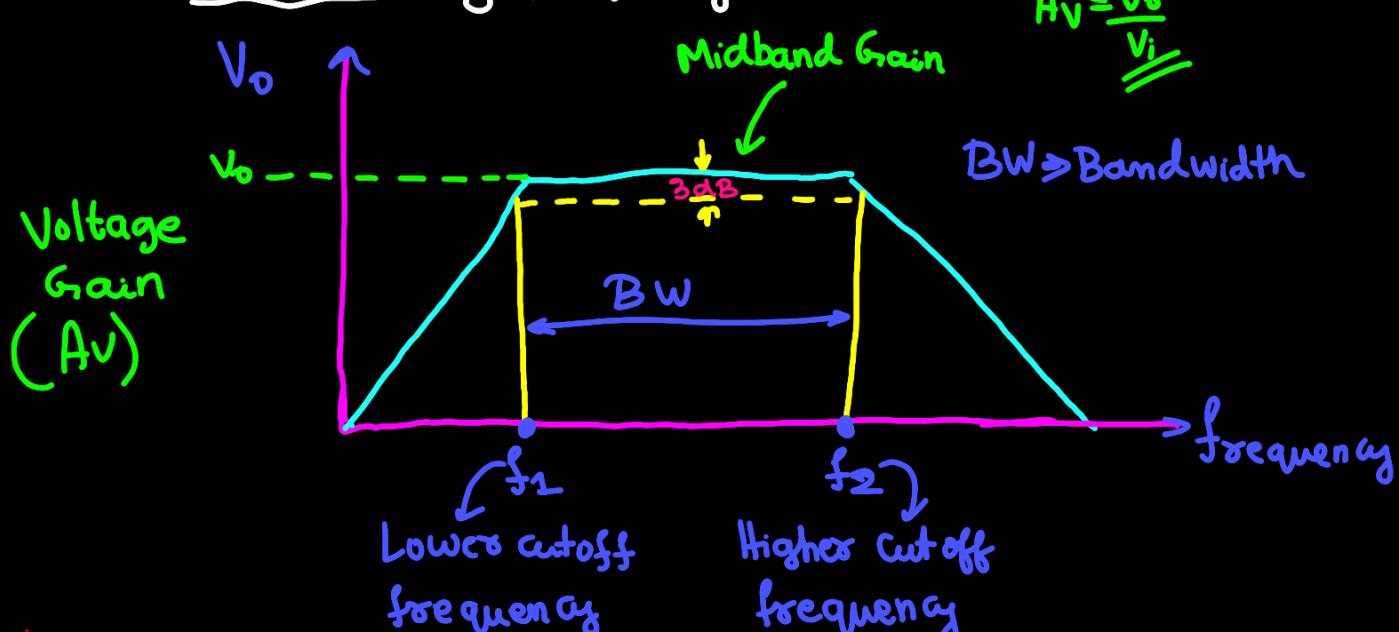
Phase shift b/w
I/P & O/P voltage
is 180°

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

$$\Rightarrow V_{DD} = V_{DS} + I_D (R_D + R_S)$$

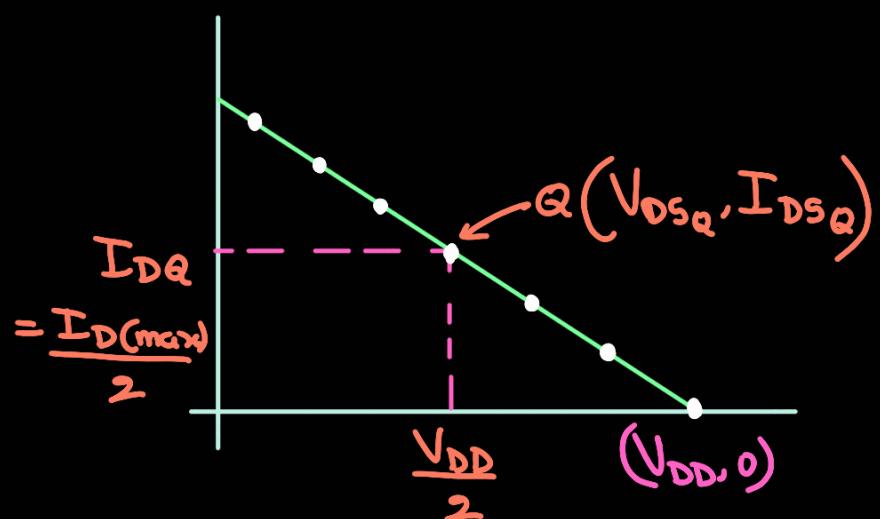
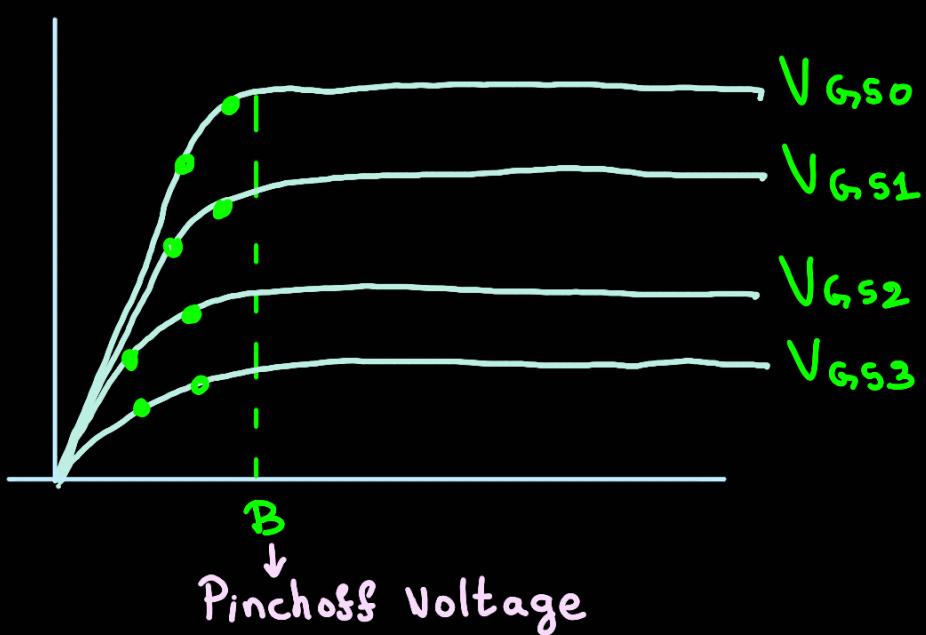
$$\therefore \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \Rightarrow V_{DS} = \mu V_{GS}$$

*Understanding frequency response:-



Keep I/P voltage V_i constant & vary the I/P frequency

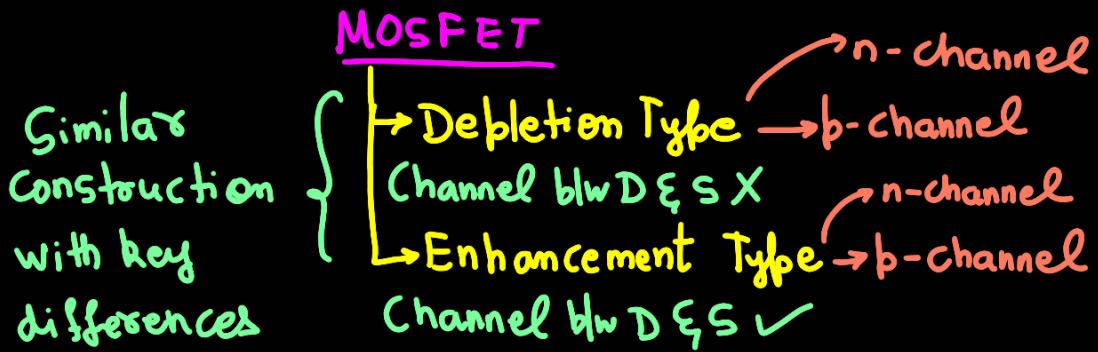
DC analysis:-



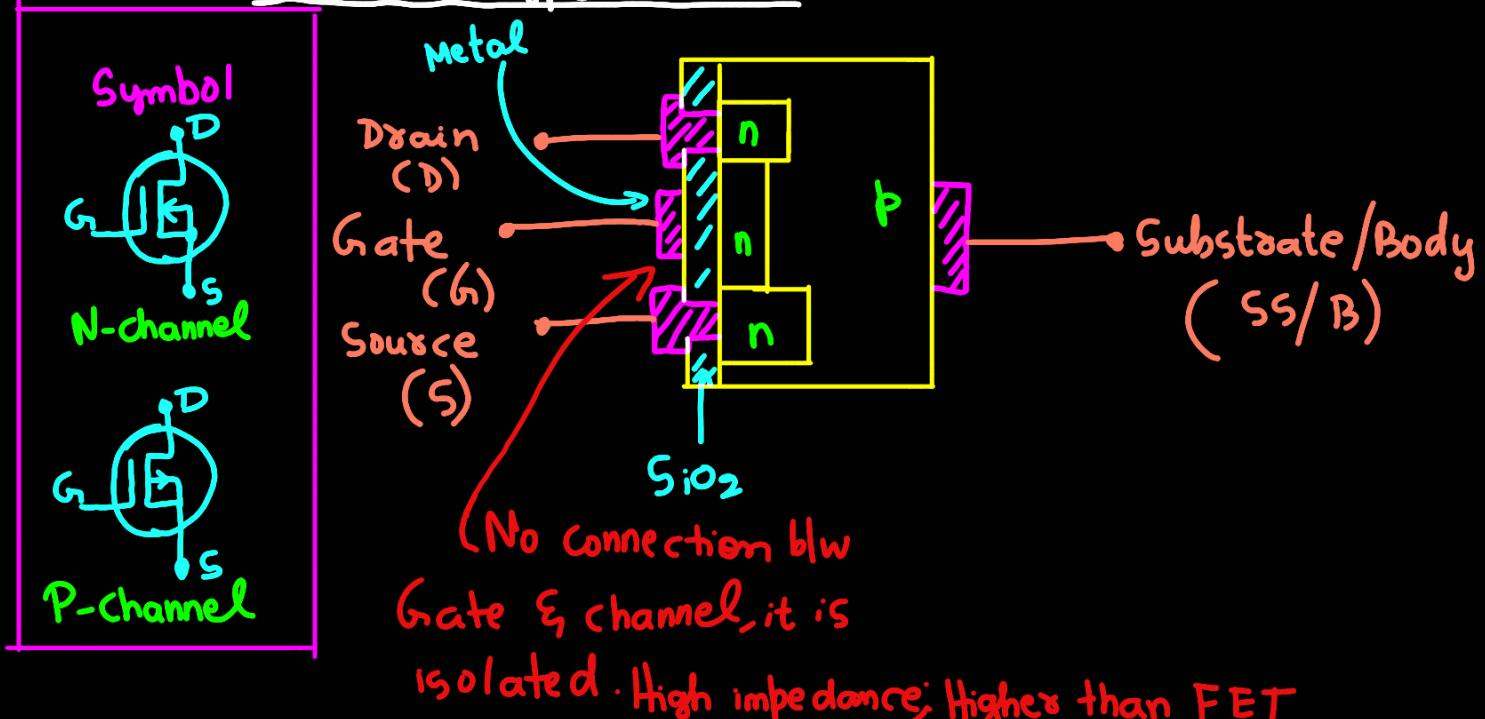
MosFET:-

↳ Metal Oxide Semiconductor Field Effect Transistor

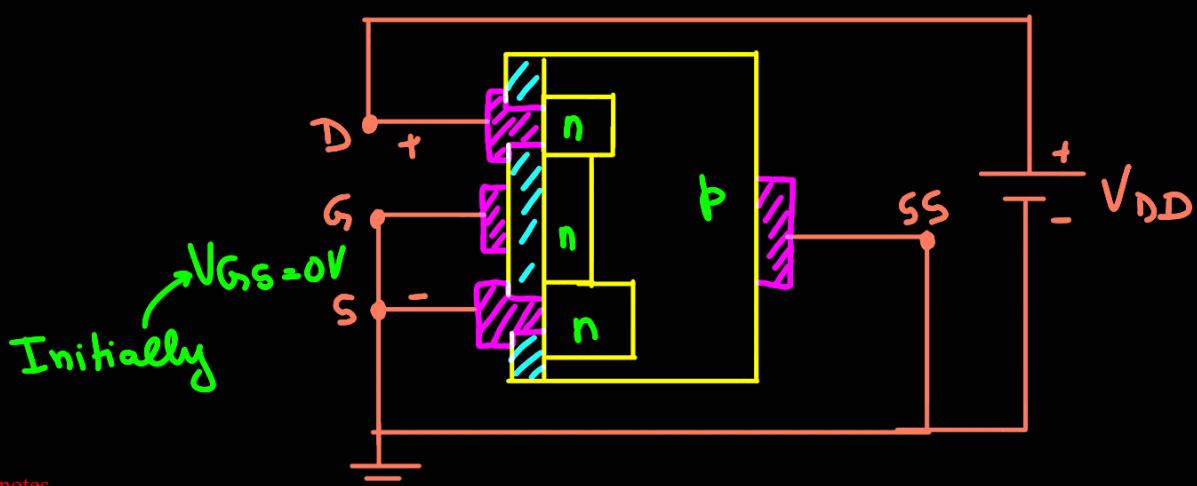
Active Device → Ability to control the flow of e^- 's



Depletion Type MOSFET:- Consider N-channel

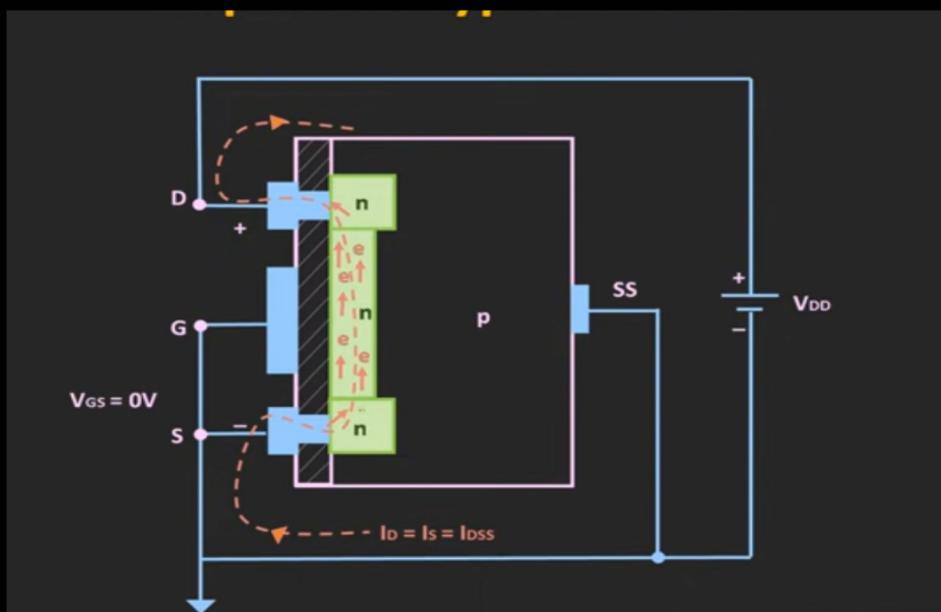


Working of Depletion Type MOSFET:-



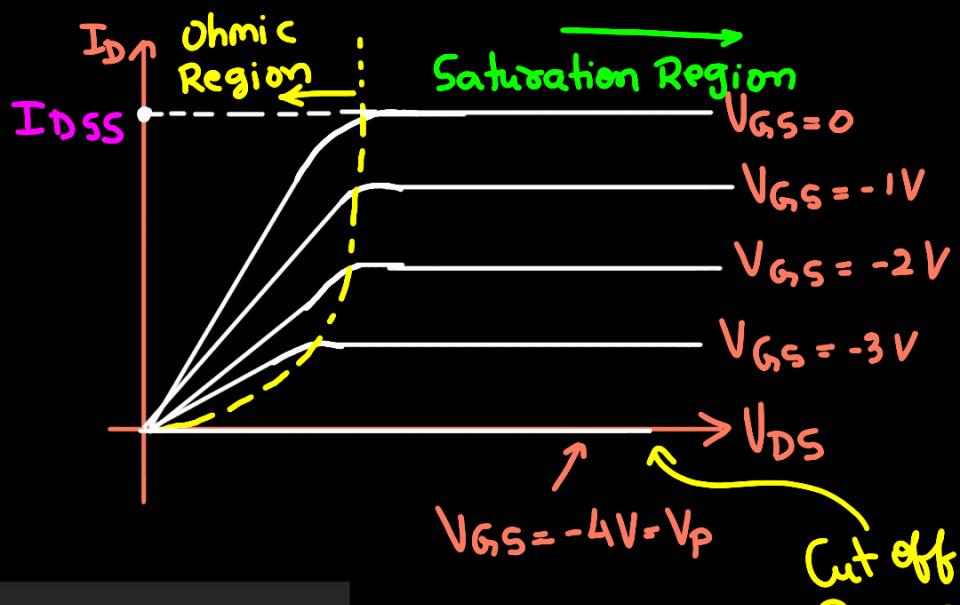
e^- in n-channel get attracted to +ve terminal

This process continues until all e^- have contributed to flow of current

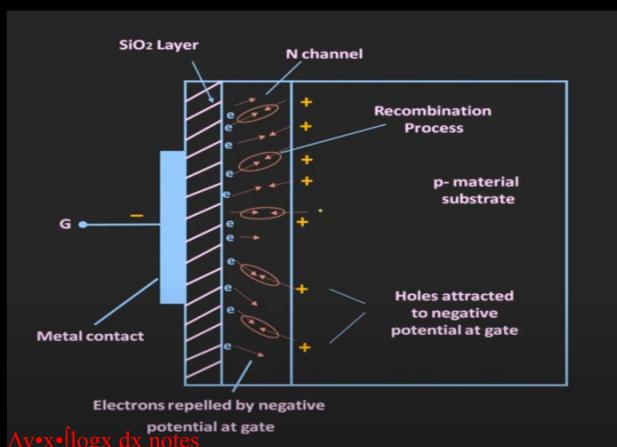


Later on ↑ Voltage, Current will be constant

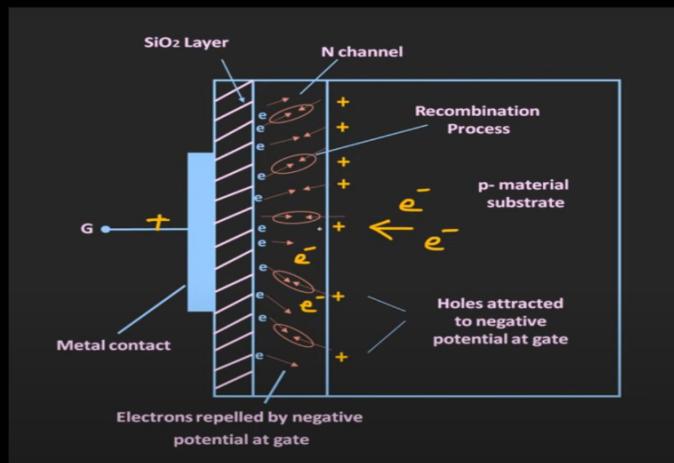
* Drain/O/P characteristics:-



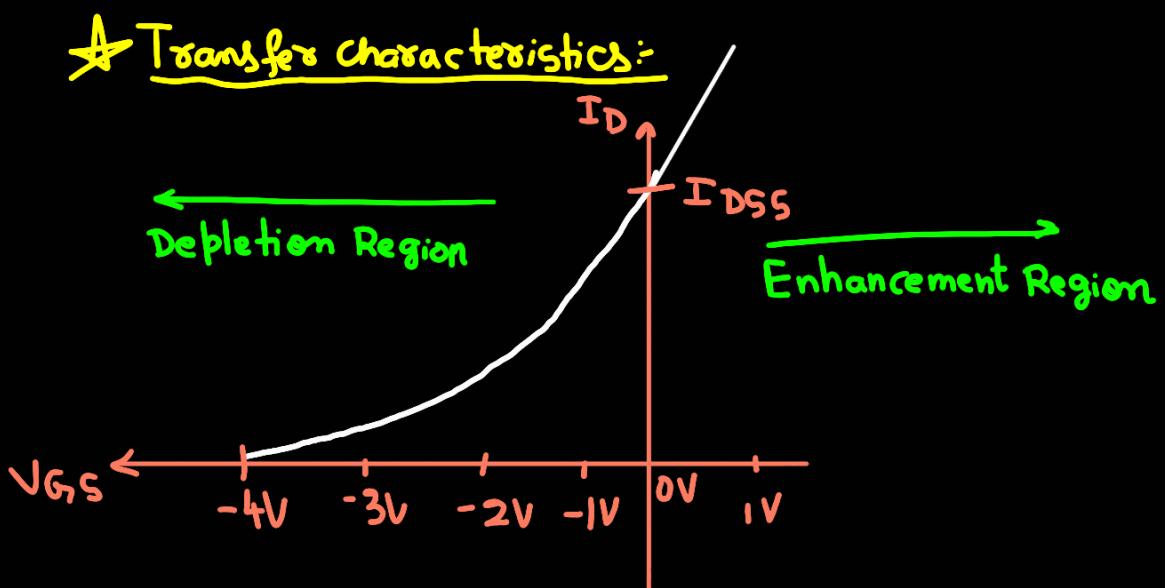
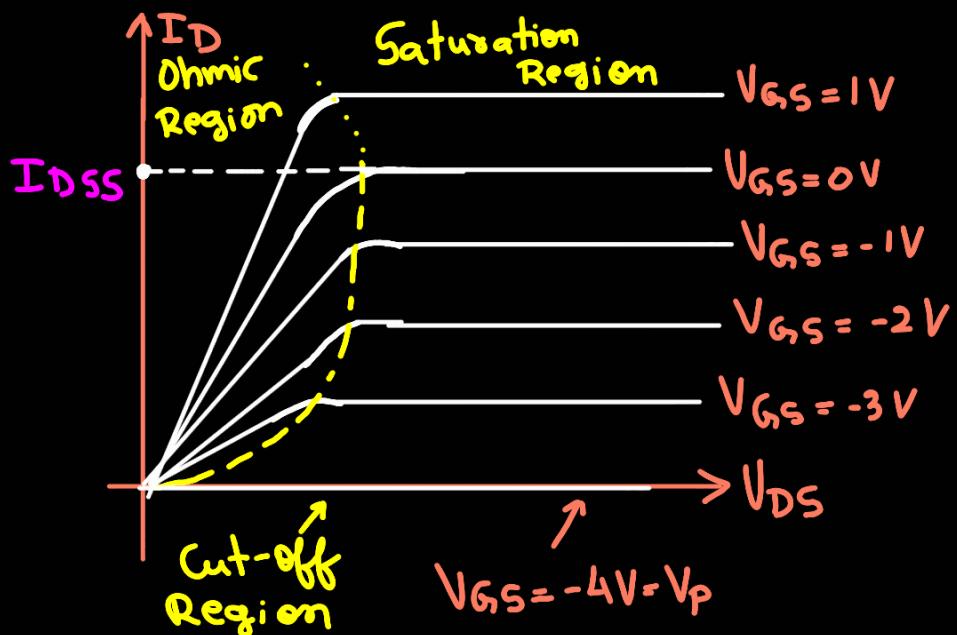
Application of -ve Voltage



$$\Delta v \cdot x \cdot \log x \text{ dx notes}$$



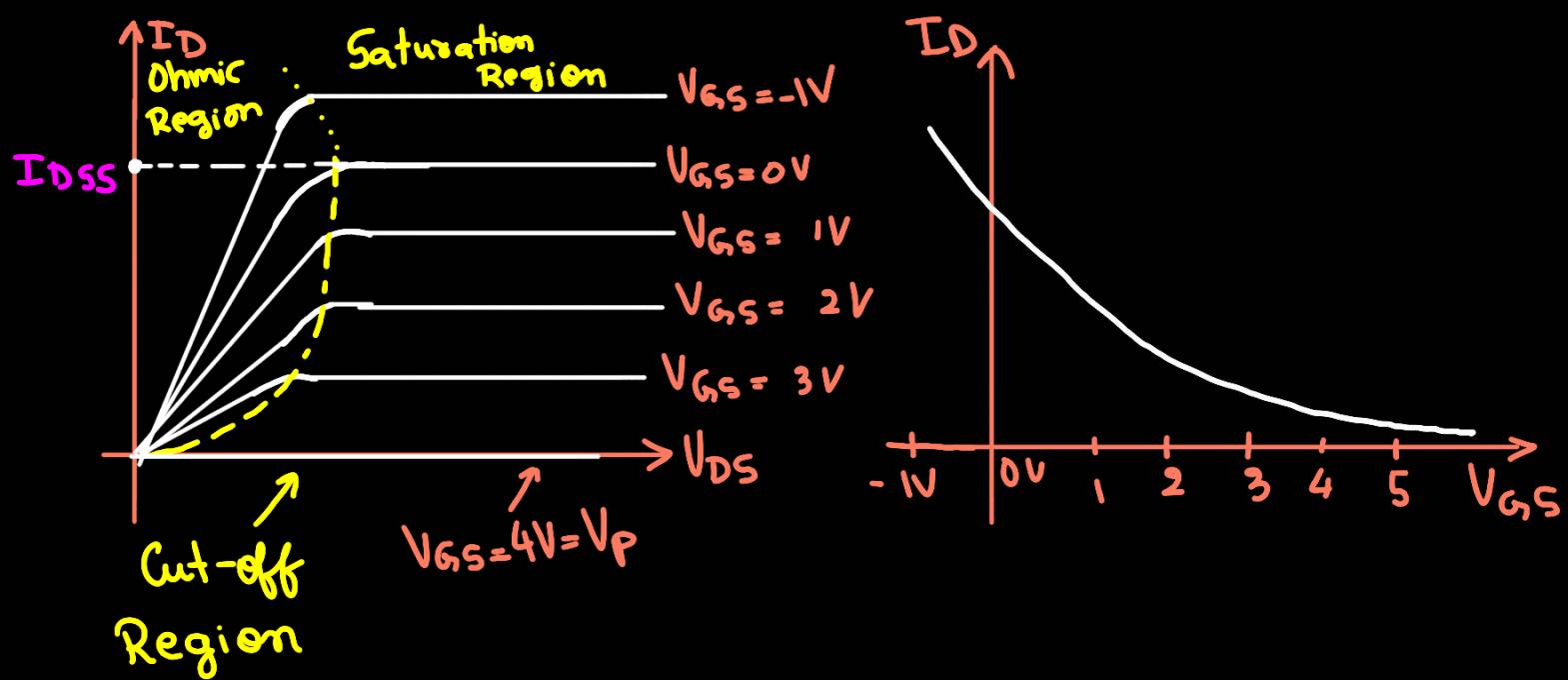
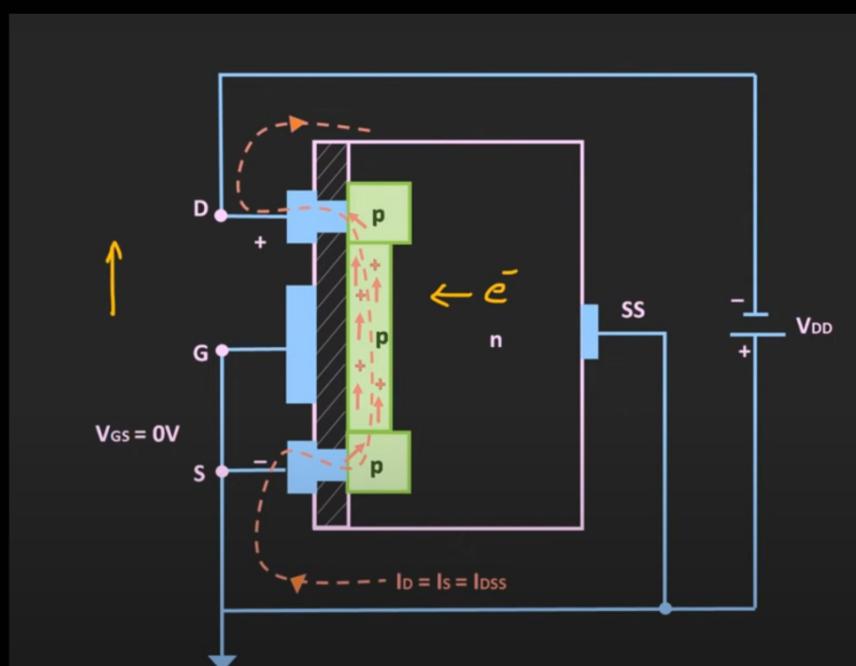
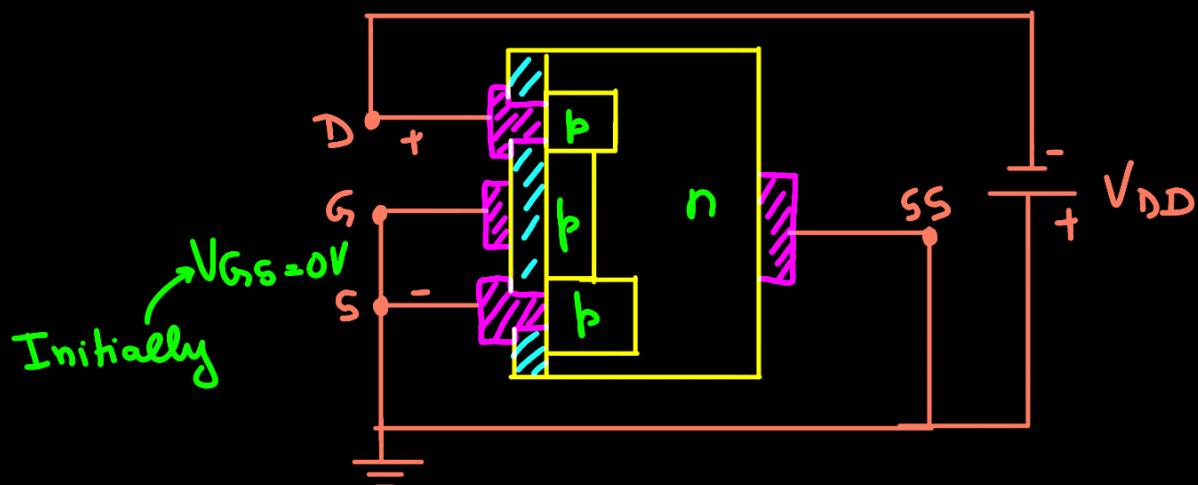
Application of +ve voltage



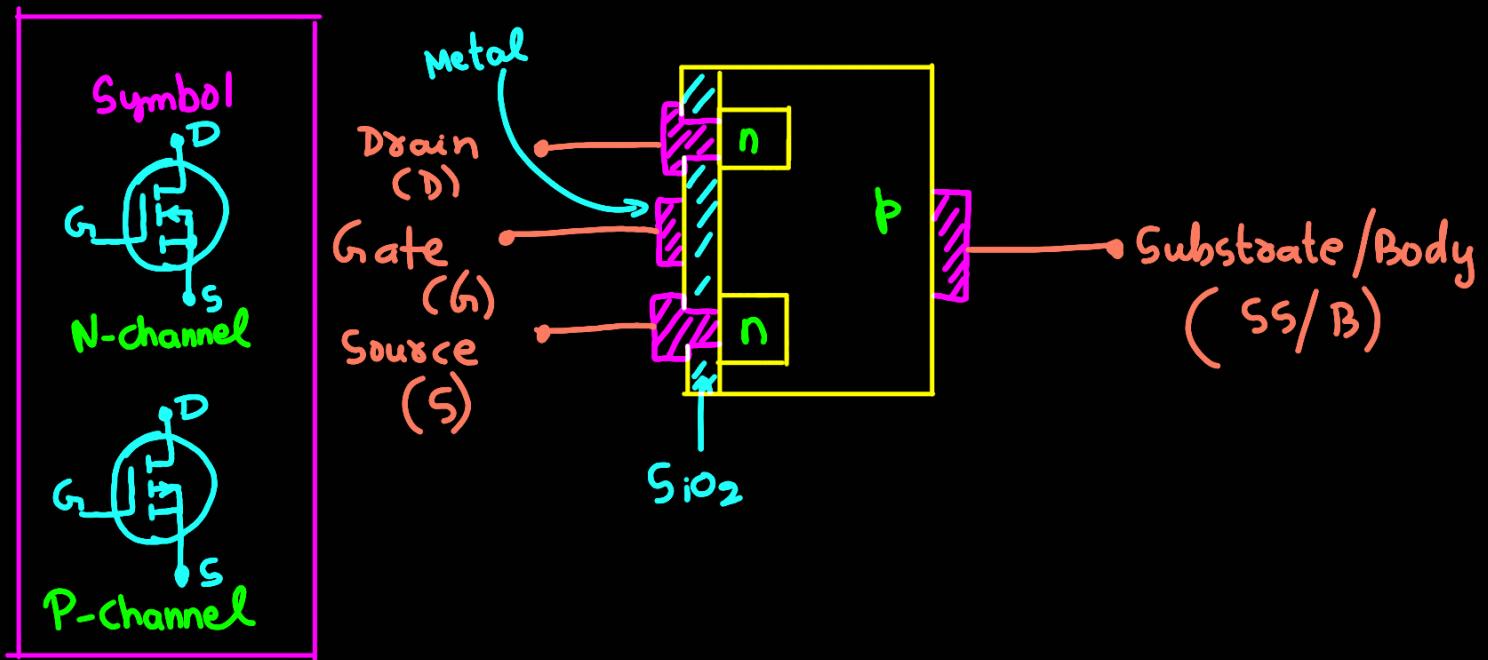
$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$

Eqⁿ for Depletion type MOSFET.
Same as JFET

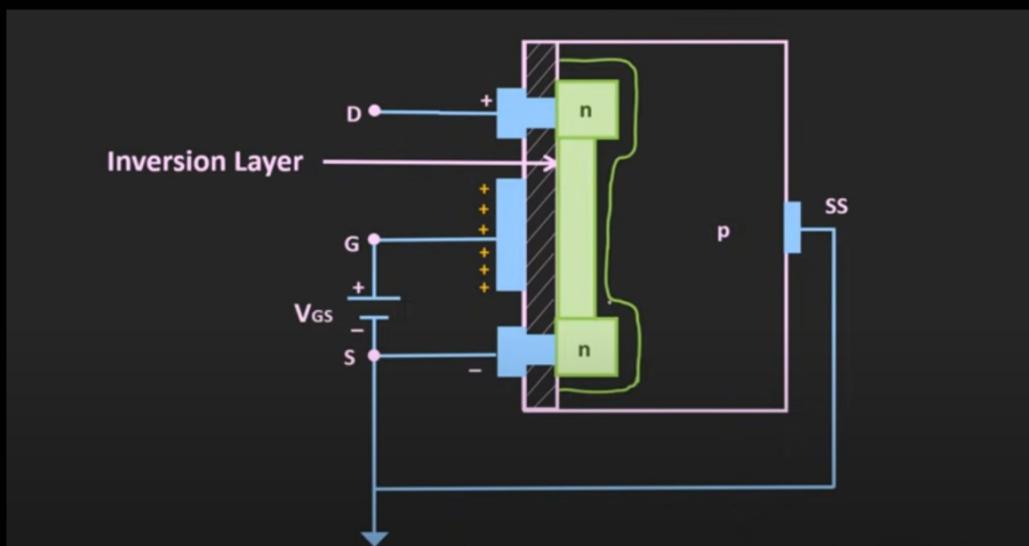
* Depletion type P-channel MOSFET Same as N-channel but polarity reversed



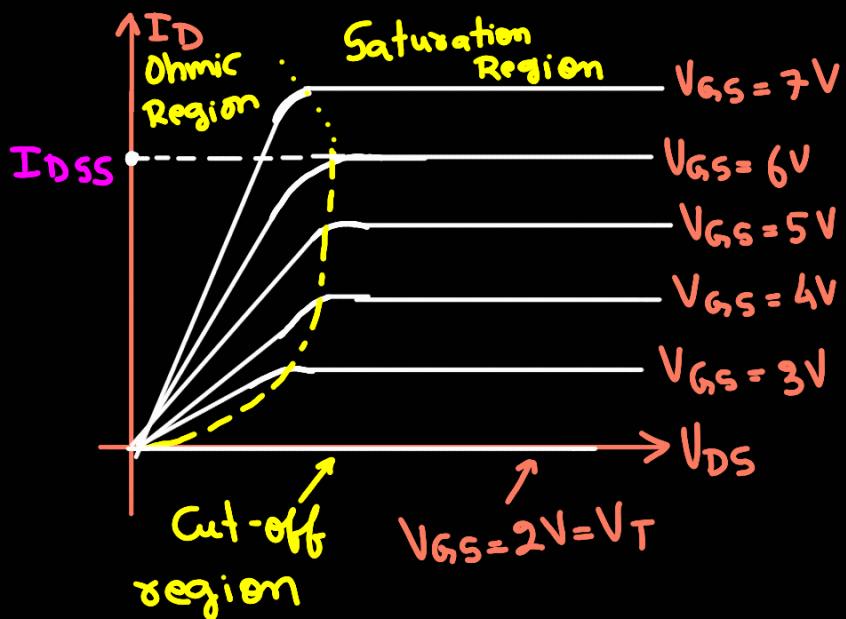
Enhancement type MOSFET:-



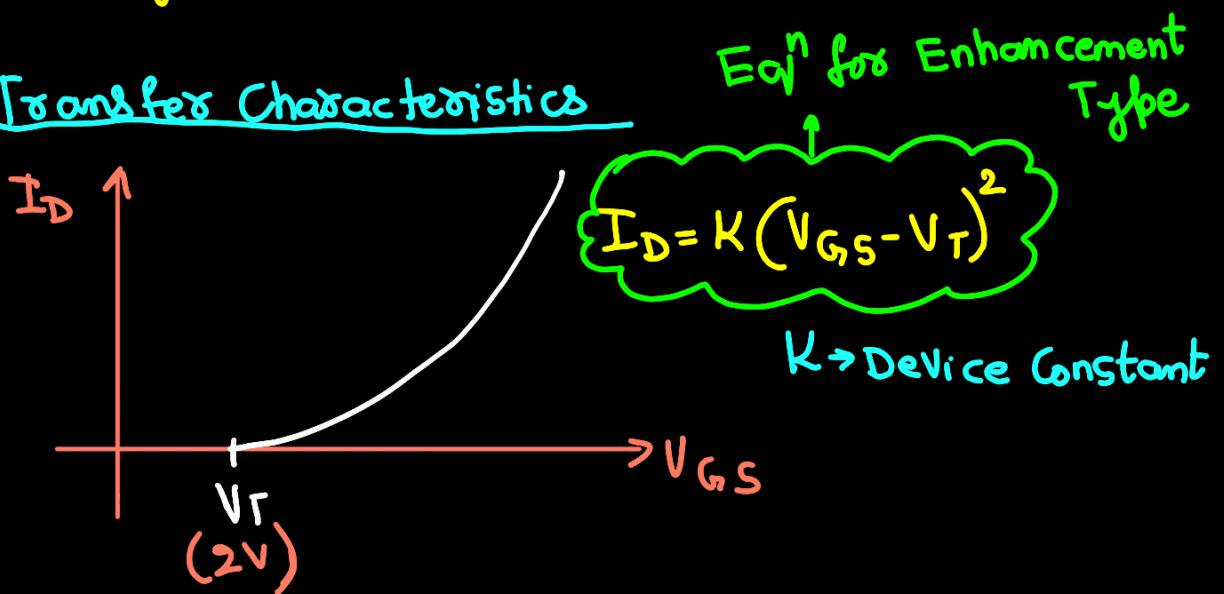
Threshold Voltage (V_{th}): The key feature of an enhancement MOSFET is the threshold voltage. For an N-channel MOSFET, when the gate-to-source voltage (V_{GS}) is greater than the threshold voltage (V_{th}), a conductive channel forms between the drain and source, allowing current to flow. For a P-channel MOSFET, the gate-to-source voltage needs to be less than the threshold voltage to turn on the device.



★ Drain Characteristics



★ Transfer Characteristics



P Channel MOSFET is Similar

Just Change the Polarity



OR

Refer below notes for
MOSFETS

~~transfer conductance = $\frac{\Delta I_D}{\Delta V_{DS}}$ = g_m~~

~~output impedance, $R_o = \frac{\Delta V_{OS}}{\Delta I_D} = \frac{V_{DS}}{I_D}$~~

~~amplification factor~~

~~$\mu = \frac{\text{o/p voltage}}{\text{i/p voltage}}$~~

~~$\mu = \frac{V_{DS}}{V_{GS}} \times \frac{I_D}{I_{GS}}$~~

~~$= \left(\frac{V_D}{I_D} \right) \left(\frac{I_D}{I_{GS}} \right)$~~

~~$= \left(\frac{\Delta V_D}{\Delta I_D} \right) \left(\frac{\Delta I_D}{\Delta V_{GS}} \right)$~~

~~$\boxed{\mu = V_o \cdot g_m}$~~

(a) MOSFET [Metal-oxide semiconductor field effect T.]

* It is unipolar device

* Operates on Voltage

* Insulator separates the gate from channel

* There are two MOSFETs they are

⇒ Depletion type MOSFET

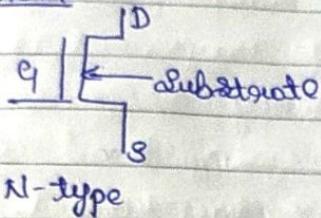
- In this MOSFET the channel is made up of N-type of material & the substrate is of P-type of material.

- SiO₂ is the metallic contact which separates the gate & the channel

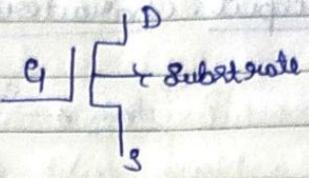
- Gate terminal is isolated from the channel due to the SiO₂ layer & partial channel setup below it



Symbol

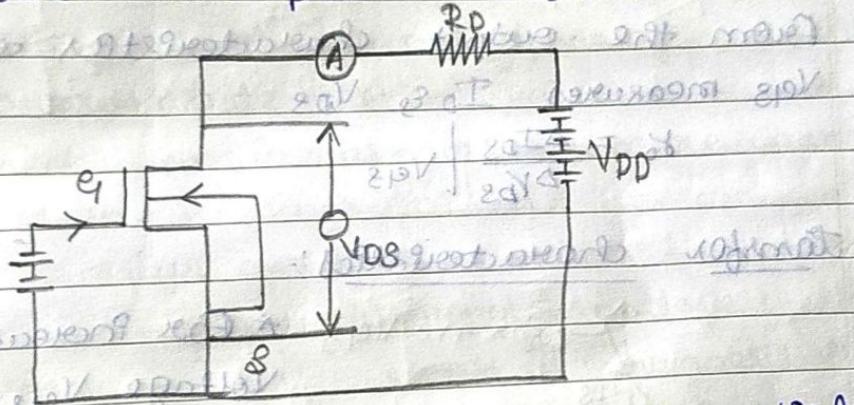


N-type



P-type

- * Due to this insulator input impedance of the gate terminal is very high. Hence MOSFET used in the application where minimum power consumption is required.



- * When $V_{GS} = 0$ & the voltage is applied b/w D & S terminal towards the one side of insulator, the other side it induces the -ve charge.

- * Hence the electron in the N-channel increases results in increase in the I_D .

- * The value of the saturation current for $V_{GS} = 0$ is called I_{DS} .

- * If the $V_{GS} = 0$ the point is called pinch-off voltage.

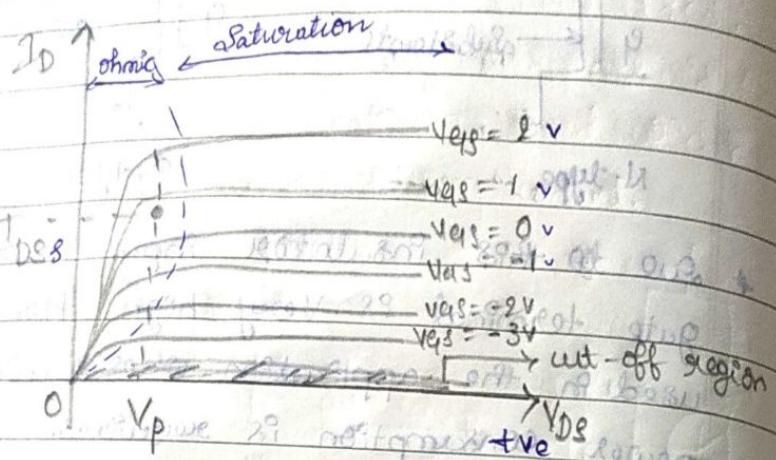
- * The voltage at which $V_{GS} = V_p$ is called cut-off region.

- * The depletion curve also works for the +ve voltage on which I_D increases.



REDMI NOTE 8
AI QUAD CAMERA

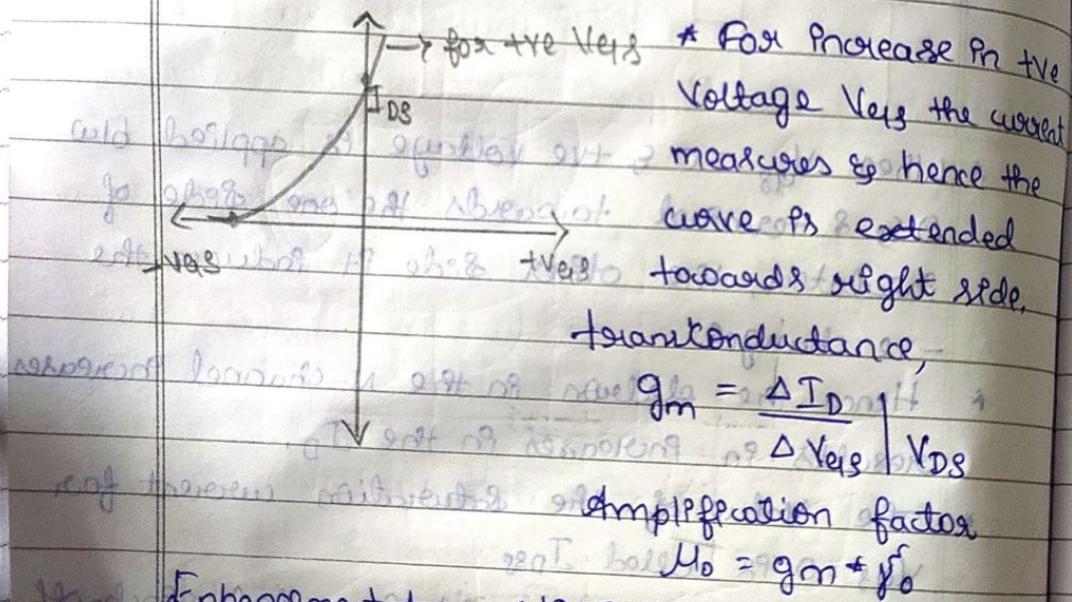
Output characteristics:



From the output characteristics at given V_{DS} measures I_D & V_{DS}

$$g_o = \frac{\Delta I_D}{\Delta V_{DS}} \quad | V_{DS}$$

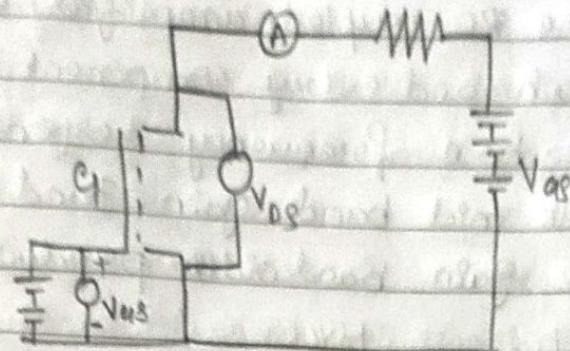
Transfer characteristics:



Enhancement type MOSFET:

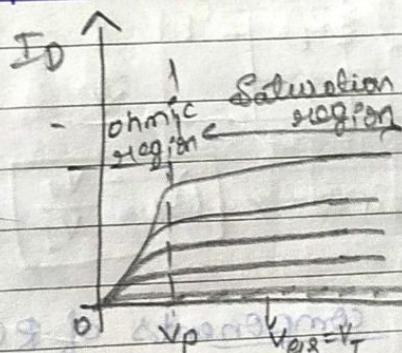
- + Substrate is made up of p-type semiconductor
- + SiO_2 isolates the gate terminal & p-substrate
- + there is no channel b/w d & s
- + When the controlled voltage is applied b/w g & s then channel is formed.





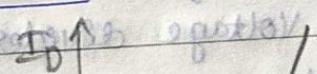
- * When $V_{GS} = 0$ the voltage is applied b/w D & S then current flows in MOSFET
- * When +ve voltage applied b/w G & S then holes near the G pushed away & e- attracted towards gate terminal.
- * When V_{GS} increases more & more channel is created.
- * The value of V_{GS} at which the current increases is called threshold voltage.
- * When $V_{GS} > V_{TH}$ width of channel will increase.
- * The voltage V_{DS} at which the pinch-off condition occurs is called saturation voltage.

Output characteristics



$$k_o^f = \frac{\Delta I_D}{\Delta V_{DS}} \Big|_{V_{DS}}$$

transfer C. :-



at low voltage region for ID $\propto V_{GS}$

however at high voltage $V_{GS} > V_{TH}$ current is controlled by V_{DS}

$$I_{DS} = k \times (V_{GS} - V_T)^2$$

REMI NOTE 6D
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Difference between JFET, BJT & MOSFET

Feature	JFET	MOSFET	BJT
Control Mechanism	Voltage applied to gate controls current	Voltage applied to gate controls current	Current applied to base controls current
Gate Structure	Junction gate	Metal-Oxide-Semiconductor gate	Base (with junctions)
Input Impedance	High	Very high	Low to moderate
Switching Speed	Faster than BJT	Very fast (faster than JFET)	Slower compared to FETs
Power Consumption	Low	Low	Higher due to base current
Thermal Stability	Good	Excellent	Poor
Current Type	Unipolar (one type of carrier)	Unipolar (one type of carrier)	Bipolar (both types of carriers)
Ideal Amplifier Configuration	Common Source	Common Source or Common Drain	Common Emitter