



1. Description

1.1. Project

Project Name	RoboSoccer_F767ZI
Board Name	NUCLEO-F767ZI
Generated with:	STM32CubeMX 6.15.0
Date	08/06/2025

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7
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3. Pins Configuration

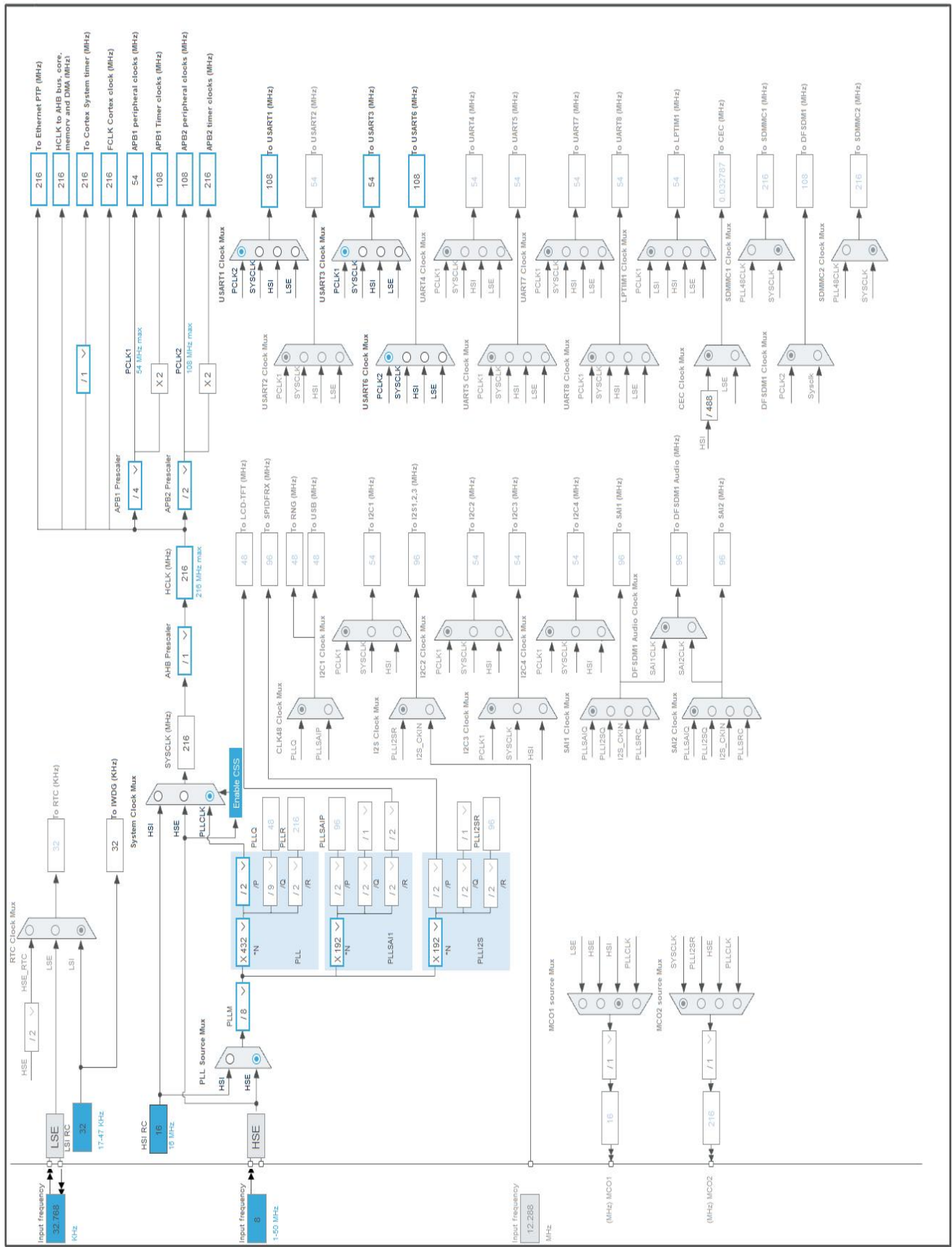
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_Btn [B1]
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
10	PF0 *	I/O	GPIO_Output	SPI_IMU_RST [BNO085_RST]
11	PF1 *	I/O	GPIO_Output	SPI_IMU_CS [BNO085_CS]
12	PF2 *	I/O	GPIO_Output	SPI_IMU_PS0_WAKE [BNO085_P0]
16	VSS	Power		
17	VDD	Power		
23	PH0/OSC_IN	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	USB_OTG_HS_ULPI_STP	
27	PC1 *	I/O	GPIO_Output	USB_OTG_HS_ULPI_RST
28	PC2	I/O	USB_OTG_HS_ULPI_DIR	
29	PC3	I/O	USB_OTG_HS_ULPI_NXT	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	ADC1_IN0	ADC_FSR1
35	PA1	I/O	ADC1_IN1	ADC_FSR2
37	PA3	I/O	USB_OTG_HS_ULPI_D0	
38	VSS	Power		
39	VDD	Power		
41	PA5	I/O	USB_OTG_HS_ULPI_CK	
46	PB0	I/O	USB_OTG_HS_ULPI_D1	
47	PB1	I/O	USB_OTG_HS_ULPI_D2	
48	PB2	I/O	SPI3_MOSI	SPI_IMU_MOSI [BNO085_DI]
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
62	VDD	Power		
69	PB10	I/O	USB_OTG_HS_ULPI_D3	
70	PB11	I/O	USB_OTG_HS_ULPI_D4	
71	VCAP_1	Power		
72	VDD	Power		
73	PB12	I/O	USB_OTG_HS_ULPI_D5	
74	PB13	I/O	USB_OTG_HS_ULPI_D6	
75	PB14 *	I/O	GPIO_Output	LD3 [ERROR]
77	PD8	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	USART6_TX	WIFI_RX [ESP32WROOM32E_IO16]
97	PC7	I/O	USART6_RX	WIFI_TX [ESP32WROOM32E_IO17]
101	PA9	I/O	USART1_TX	MOTOR_TX
102	PA10	I/O	USART1_RX	MOTOR_RX
105	PA13	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
110	PA15	I/O	SYS_JTDI	
111	PC10	I/O	SPI3_SCK	SPI_IMU_CLK [BNO085_SCL]
112	PC11	I/O	SPI3_MISO	SPI_IMU_MISO [BNO085_SDA]
120	VSS	Power		
121	VDDSDMMC	Power		
130	VSS	Power		
131	VDD	Power		
133	PB3	I/O	SYS_JTDO-SWO	
135	PB5	I/O	USB_OTG_HS_ULPI_D7	
137	PB7 *	I/O	GPIO_Output	LD2 [DEBUG]
138	BOOT0	Boot		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
141	PE0	I/O	GPIO_EXTI0	SPI_IMU_INT [BNO085_INT]
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	DS11532_Rev4

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

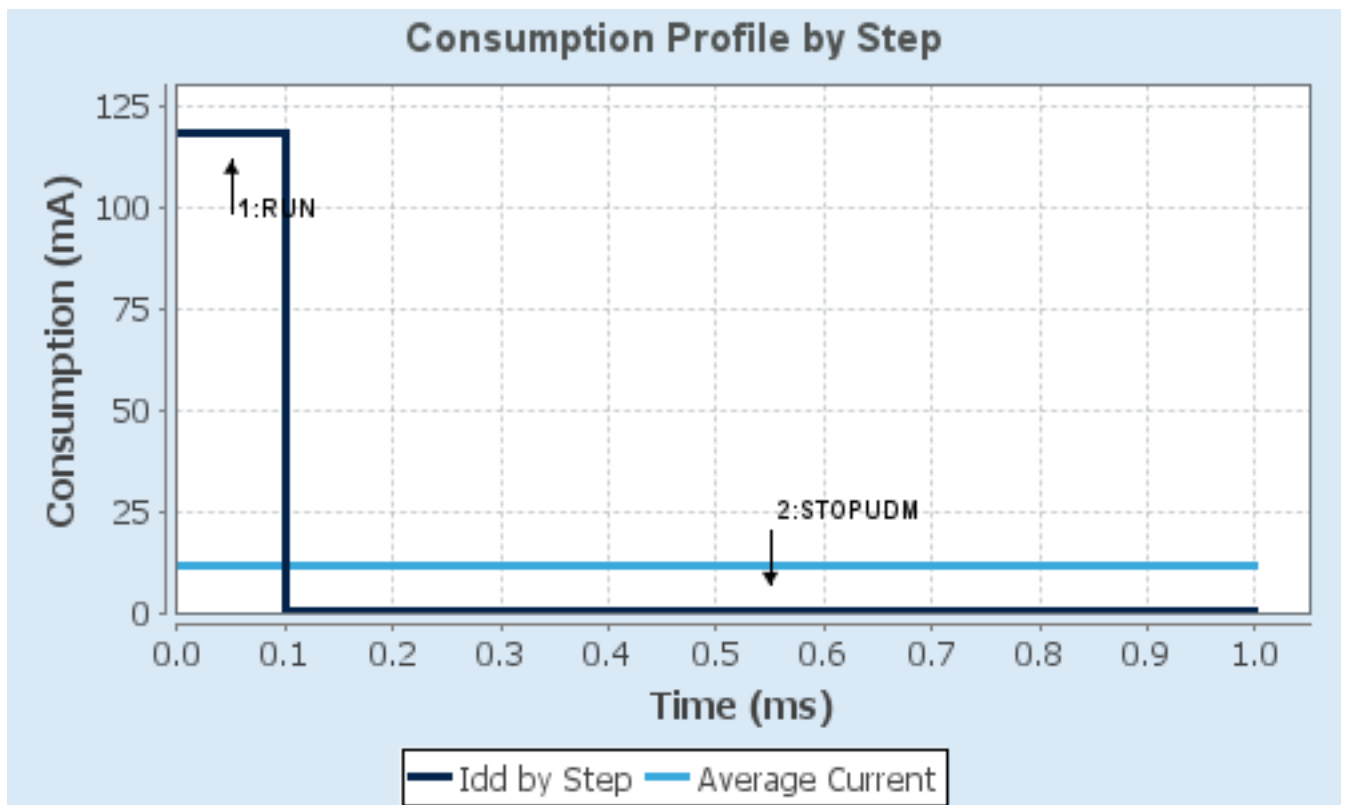
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ICTM FLASH-SingleBank REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	118 mA	130 μ A
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	89.42	104.98
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24005 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	RoboSoccer_F767ZI
Project Folder	C:\Users\Bowen\Documents\UW_Files\Proj\RoboSoccer_F767ZI
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.17.3
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_USART3_UART_Init	USART3
5	MX_ADC1_Init	ADC1
6	MX_TIM2_Init	TIM2
7	MX_SPI3_Init	SPI3
8	MX_USART1_UART_Init	USART1
9	MX_IWDG_Init	IWDG
10	MX_USB_DEVICE_Init	USB_DEVICE
11	MX_USART6_UART_Init	USART6

3. Peripherals and Middlewares Configuration

3.1. ADC1

mode: IN0

mode: IN1

mode: Temperature Sensor Channel

mode: Vrefint Channel

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 6 *
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	4 *
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
<u>Rank</u>	1
Channel	Channel 0
Sampling Time	480 Cycles *
<u>Rank</u>	2 *
Channel	Channel 1 *
Sampling Time	480 Cycles *
<u>Rank</u>	3 *
Channel	Channel Temperature Sensor *
Sampling Time	144 Cycles *
<u>Rank</u>	4 *
Channel	Channel Vrefint *
Sampling Time	144 Cycles *

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

3.2. IWDG

mode: Activated

3.2.1. Parameter Settings:**Watchdog Clocking:**

IWDG counter clock prescaler	32 *
IWDG window value	4095
IWDG down-counter reload value	999 *

3.3. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

3.3.1. Parameter Settings:**System Parameters:**

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

3.4. SPI3

Mode: Full-Duplex Master

3.4.1. Parameter Settings:**Basic Parameters:**

Frame Format	Motorola
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Data Size	8 Bits *
First Bit	MSB First
Clock Parameters:	
Prescaler (for Baud Rate)	32 *
Baud Rate	1.6875 MBits/s *
Clock Polarity (CPOL)	High *
Clock Phase (CPHA)	2 Edge *
Advanced Parameters:	
CRC Calculation	Disabled
NSS Signal Type	Software

3.5. SYS

Debug: JTAG (4 pins)

Timebase Source: TIM6

3.6. TIM2

Clock Source : Internal Clock

3.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	107 *
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0xFFFFFFFF
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

3.7. USART1

Mode: Asynchronous

3.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	1000000 *
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Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

3.8. USART3

Mode: Asynchronous

3.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

3.9. USART6

Mode: Asynchronous

3.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

3.10. USB_OTG_HS

External Phy: Device_Only

3.10.1. Parameter Settings:

Speed	Device High Speed 480MBit/s
Enable internal IP DMA	Disabled
Physical interface	External Phy
Low power	Disabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

3.11. FREERTOS

Interface: CMSIS_V2

3.11.1. Config parameters:

API:

FreeRTOS API CMSIS v2

Versions:

FreeRTOS version 10.2.1

CMSIS-RTOS version 2.00

MPU/FPU:

ENABLE_MPU Disabled

ENABLE_FPU Disabled

Kernel settings:

USE_PREEMPTION Enabled

CPU_CLOCK_HZ SystemCoreClock

TICK_RATE_HZ 1000

MAX_PRIORITIES 56

MINIMAL_STACK_SIZE 256

MAX_TASK_NAME_LEN 16

USE_16_BIT_TICKS Disabled

IDLE_SHOULD_YIELD Enabled

USE_MUTEXES Enabled

USE_RECURSIVE_MUTEXES Enabled

USE_COUNTING_SEMAPHORES Enabled

QUEUE_REGISTRY_SIZE 8

USE_APPLICATION_TASK_TAG Disabled

ENABLE_BACKWARD_COMPATIBILITY Enabled

USE_PORT_OPTIMISED_TASK_SELECTION Disabled

USE_TICKLESS_IDLE Disabled

USE_TASK_NOTIFICATIONS Enabled

RECORD_STACK_HIGH_ADDRESS **Enabled ***

Memory management settings:

Memory Allocation Dynamic / Static

TOTAL_HEAP_SIZE 15360

Memory Management scheme heap_4

Hook function related definitions:

USE_IDLE_HOOK **Enabled ***

USE_TICK_HOOK Disabled

USE_MALLOC_FAILED_HOOK Disabled

USE_DAEMON_TASK_STARTUP_HOOK Disabled

CHECK_FOR_STACK_OVERFLOW **Option2 ***

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS **Enabled ***

USE_TRACE_FACILITY Enabled

USE_STATS_FORMATTING_FUNCTIONS **Enabled ***

Co-routine related definitions:

USE_CO_ROUTINES Disabled

MAX_CO_ROUTINE_PRIORITIES 2

Software timer definitions:

USE_TIMERS Enabled

TIMER_TASK_PRIORITY 2

TIMER_QUEUE_LENGTH 10

TIMER_TASK_STACK_DEPTH 512

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY 15

LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY 5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE size_t

USE_POSIX_ERRNO Disabled

3.11.2. Include parameters:

Include definitions:

vTaskPrioritySet Enabled

uxTaskPriorityGet Enabled

vTaskDelete Enabled

vTaskCleanUpResources Disabled

vTaskSuspend Enabled

vTaskDelayUntil Enabled

vTaskDelay Enabled

xTaskGetSchedulerState Enabled

xTaskResumeFromISR Enabled

xQueueGetMutexHolder Enabled

xSemaphoreGetMutexHolder Disabled

pcTaskGetTaskName Disabled

uxTaskGetStackHighWaterMark Enabled

xTaskGetCurrentTaskHandle Disabled

eTaskGetState Enabled

xEventGroupSetBitFromISR Disabled

xTimerPendFunctionCall Enabled

xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

3.11.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT **Enabled ***

Project settings (see parameter description first):

Use FW pack heap file **Enabled**

3.12. USB_DEVICE

Class For HS IP: Communication Device Class (Virtual Port Com)

3.12.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

3.12.2. Device Descriptor:

Device Descriptor:

VID (Vendor Identifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor HS:

PID (Product Identifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0/WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	ADC_FSR1
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	ADC_FSR2
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO [STM32F103CBT6_PA8]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI3	PB2	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	SPI_IMU_MOSI [BNO085_DI]
	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	SPI_IMU_CLK [BNO085_SCL]
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	SPI_IMU_MISO [BNO085_SDA]
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
	PA15	SYS_JTDI	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	MOTOR_TX
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	MOTOR_RX
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	STLK_RX [STM32F103CBT6_PA3]
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	STLK_TX [STM32F103CBT6_PA2]
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	WIFI_RX [ESP32WROOM32E_IO16]
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	WIFI_TX [ESP32WROOM32E_IO17]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
USB_OTG_HS	PC0	USB_OTG_HS_ULPI_STP	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC2	USB_OTG_HS_ULPI_DIR	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3	USB_OTG_HS_ULPI_NXT	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA3	USB_OTG_HS_ULPI_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA5	USB_OTG_HS_ULPI_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB0	USB_OTG_HS_ULPI_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB1	USB_OTG_HS_ULPI_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB10	USB_OTG_HS_ULPI_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB11	USB_OTG_HS_ULPI_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB12	USB_OTG_HS_ULPI_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB13	USB_OTG_HS_ULPI_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB5	USB_OTG_HS_ULPI_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USER_Btn [B1]
	PF0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI_IMU_RST [BNO085_RST]
	PF1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High *	SPI_IMU_CS [BNO085_CS]
	PF2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI_IMU_PS0_WAKE [BNO085_P0]
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_OTG_HS_ULPI_RST
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [ERROR]
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [DEBUG]
	PE0	GPIO_EXTI0	External Interrupt Mode with Falling edge trigger detection	Pull-up *	n/a	SPI_IMU_INT [BNO085_INT]

4.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Medium *

ADC1: DMA2_Stream0 DMA request Settings:

Mode: **Circular ***
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Half Word
Memory Data Width: Half Word

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
EXTI line0 interrupt	true	3	0
USART1 global interrupt	true	5	0
USART3 global interrupt	true	5	0
EXTI line[15:10] interrupts	true	5	0
SPI3 global interrupt	true	4	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	15	0
DMA2 stream0 global interrupt	true	5	0
USB On The Go HS End Point 1 Out global interrupt	true	5	0
USB On The Go HS End Point 1 In global interrupt	true	5	0
USB On The Go HS global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM2 global interrupt	unused		
USART6 global interrupt	unused		
FPU global interrupt	unused		

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
EXTI line0 interrupt	false	true	true
USART1 global interrupt	false	true	true
USART3 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
SPI3 global interrupt	false	true	true
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	false	true	true
DMA2 stream0 global interrupt	false	true	true
USB On The Go HS End Point 1 Out global interrupt	false	true	true
USB On The Go HS End Point 1 In global interrupt	false	true	true
USB On The Go HS global interrupt	false	true	true

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

Middleware						
<div>FREERTOS </div> <div>USB_DEVICE </div>						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
CORTEX_M7	ADC1	TIM2	SPI3			
DMA			USART1			
GPIO			USART3			
IWDG			USART6			
IVIC			USB_HS			
RCC						
SYS						

6. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32f7_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32f7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32f7-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
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Page 31](https://www.st.com/resource/en/application_note/an5360-getting-started-</p></div><div data-bbox=)

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