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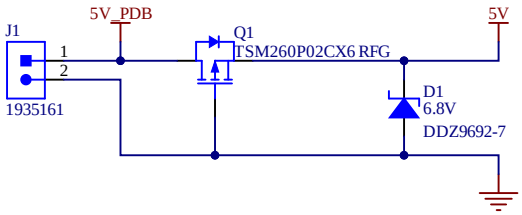
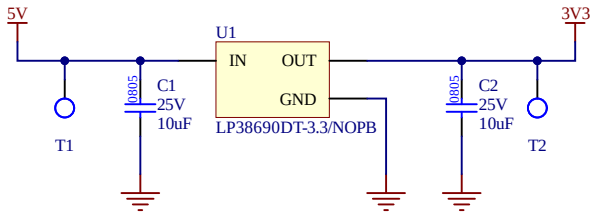
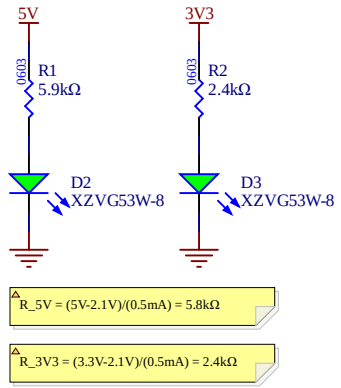
BMS Connector



5V to 3.3V LDO @ 1A Max



Power LEDs



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PROJECT Zeropilot 2.0.PrjPcb, [No Variations]		REVISION *
DOCUMENT LDO.SchDoc		MODIFIED 11/20/2021
ENGINEER Daniel Puratich	REVIEWER *	SHEET 1 OF 9

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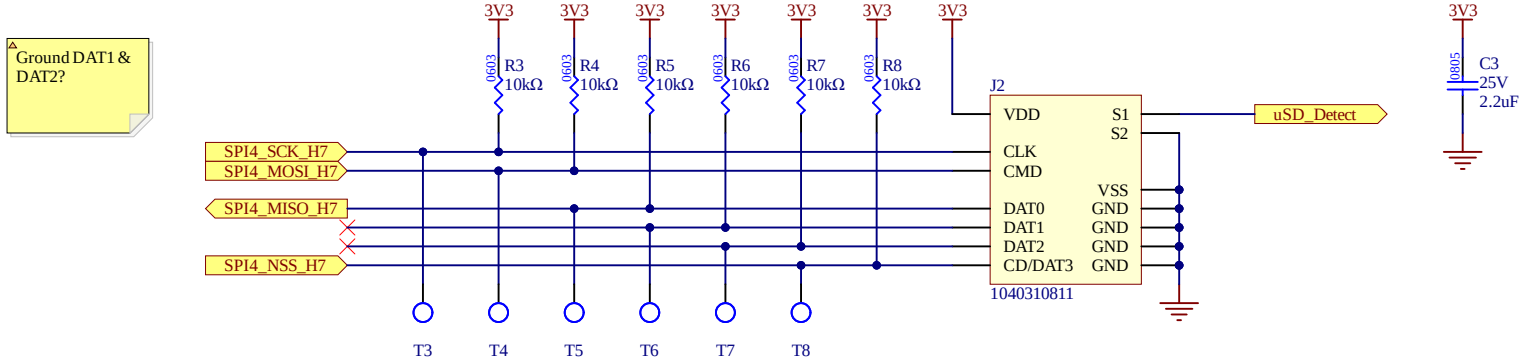
microSD Connector



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PROJECT: Zeropilot 2.0.PrjPcb, [No Variations]	REVISION: *
DOCUMENT: microSD_Connector.SchDoc	MODIFIED: 11/20/2021
ENGINEER: Kiran Surendran / REVIEWER: *	SHEET 3 OF 9

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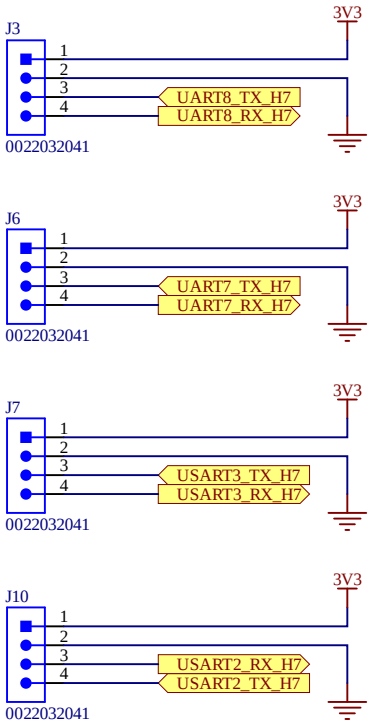
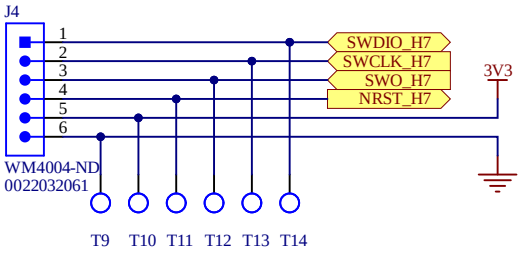
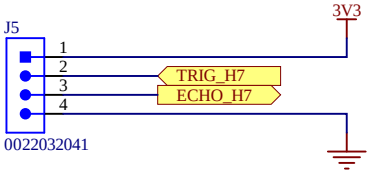
UART Connectors



SWD/SWO Connector

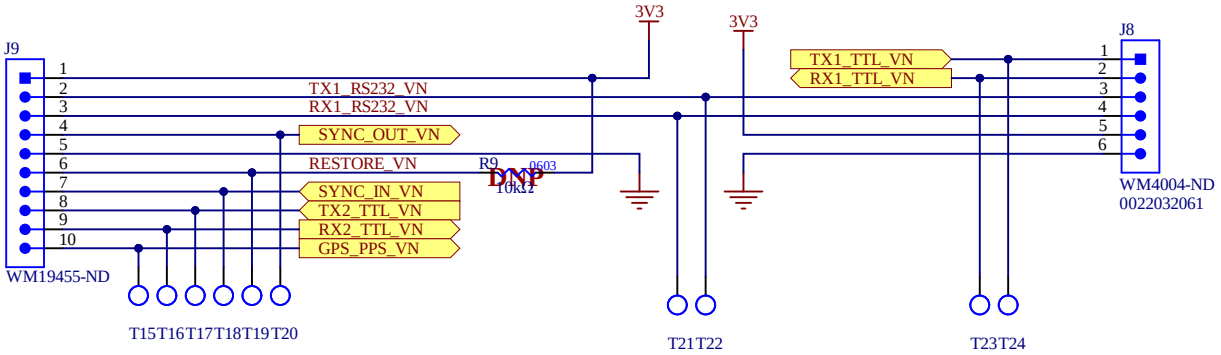


Ultrasonic Connector

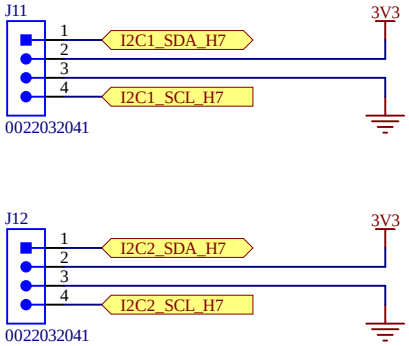


VN-300 Connector

MAX3232 Connector



I2C Connectors



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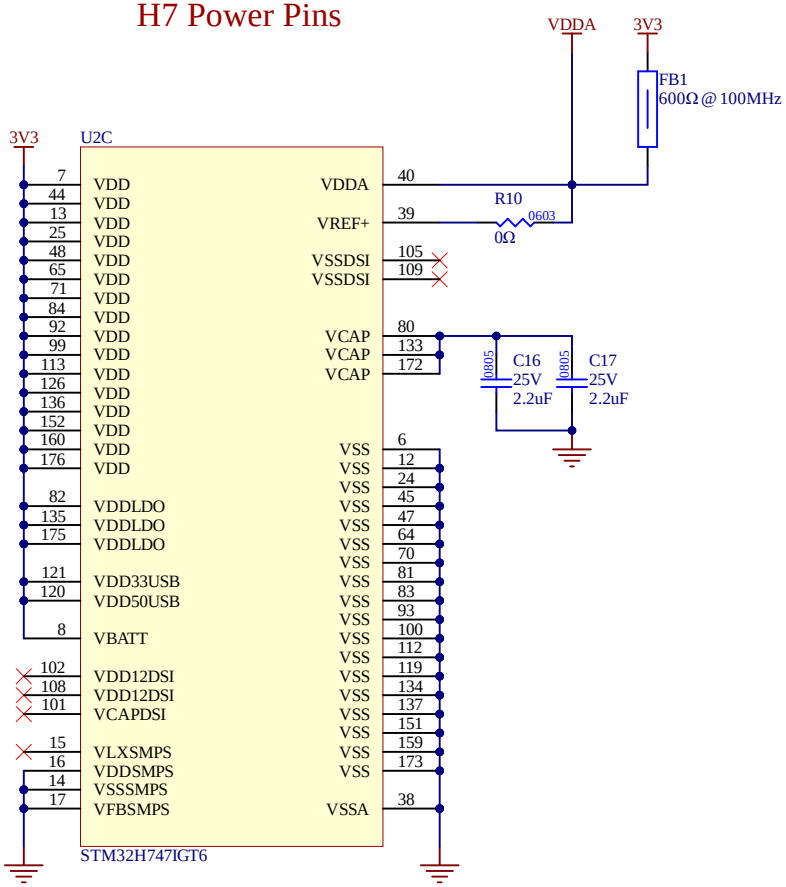
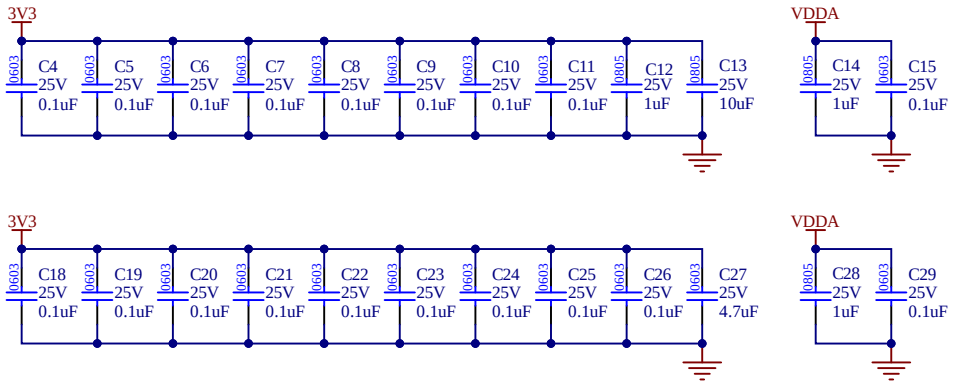
H7 Power Pins



H7 Bypass Capacitors



VDD Bypass: (0.1uF x 16) + (10uF x 1)
VDDLDO Bypass: 4.7uF x 1
VDDUSB Bypass: (0.1uF x 1) + (1uF x 1)
Should be placed as close as possible to each VDD pin.

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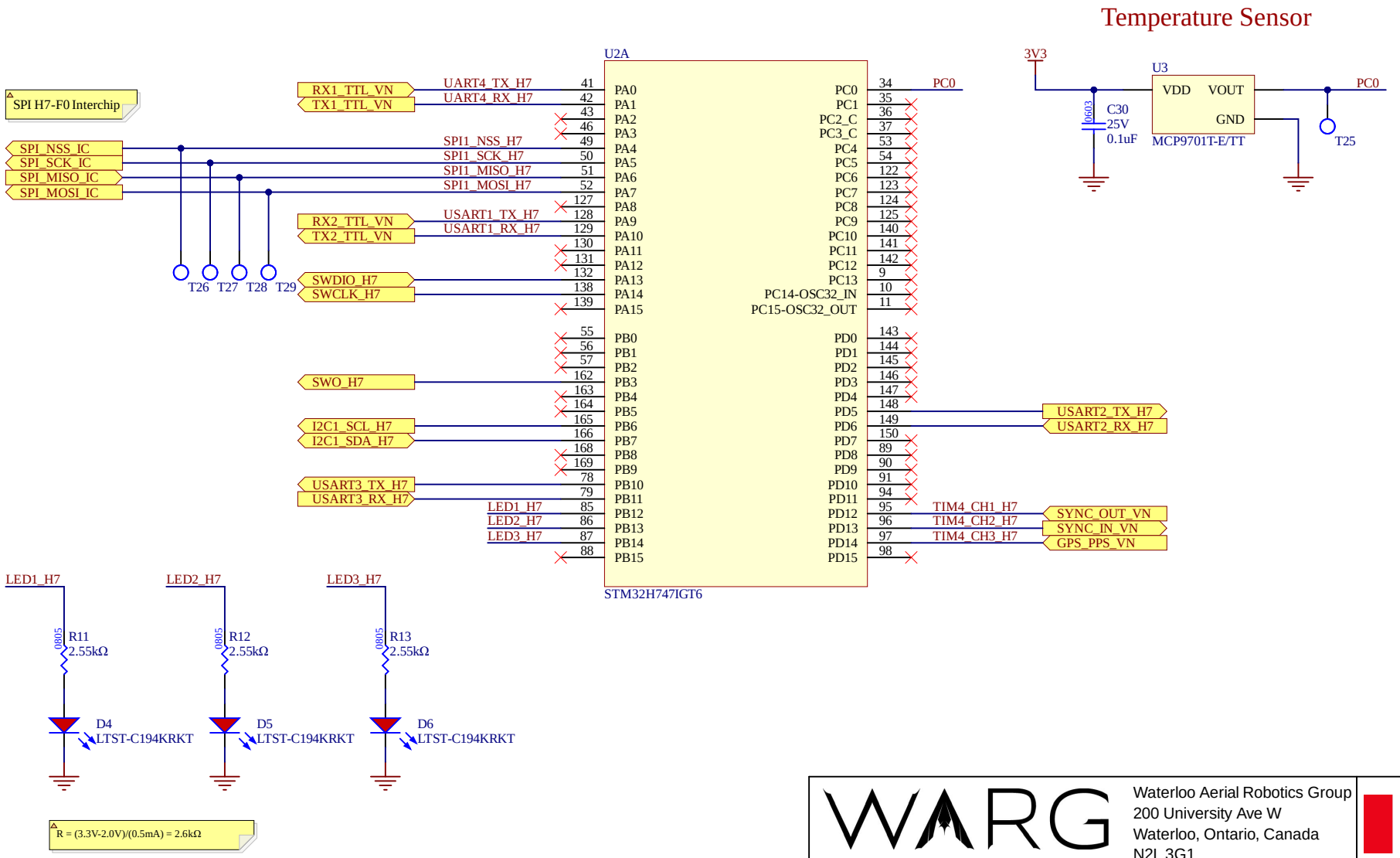
Zeropilot 2.0



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PROJECT: Zeropilot 2.0.PrjPcb, [No Variations]	REVISION: 1
DOCUMENT: H7PartA.SchDoc	MODIFIED: 11/20/2021
ENGINEER: Kiran Surendran	REVIEWER: *
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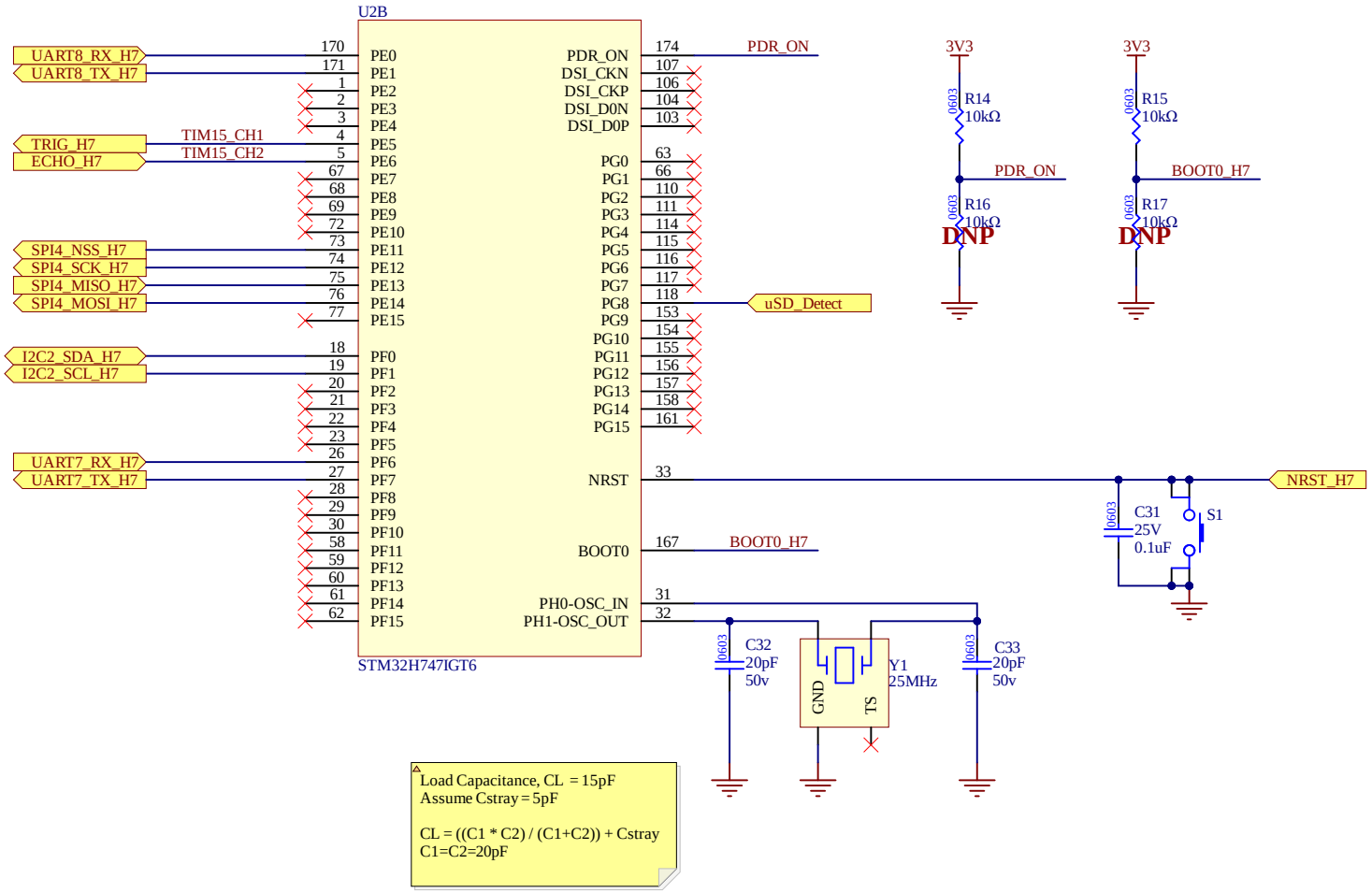

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DOCUMENT: H7PartB.SchDoc	MODIFIED: 11/17/2021
ENGINEER: Kiran Surendran	REVIEWER: *
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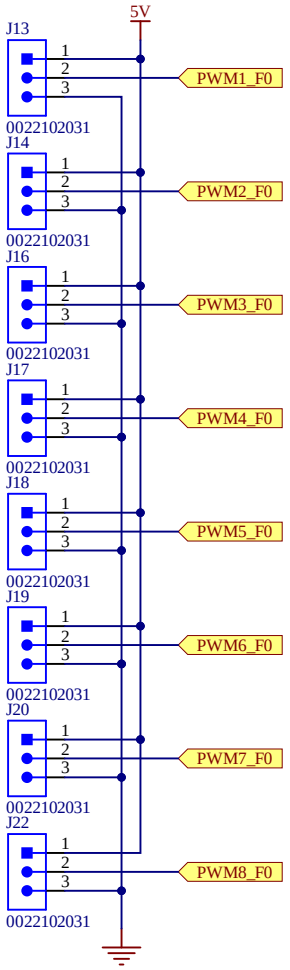
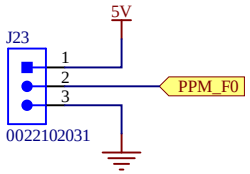
PWM Connectors



PPM Connector



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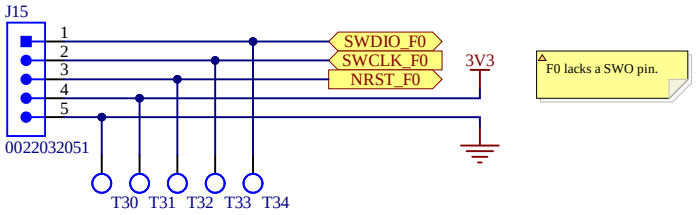
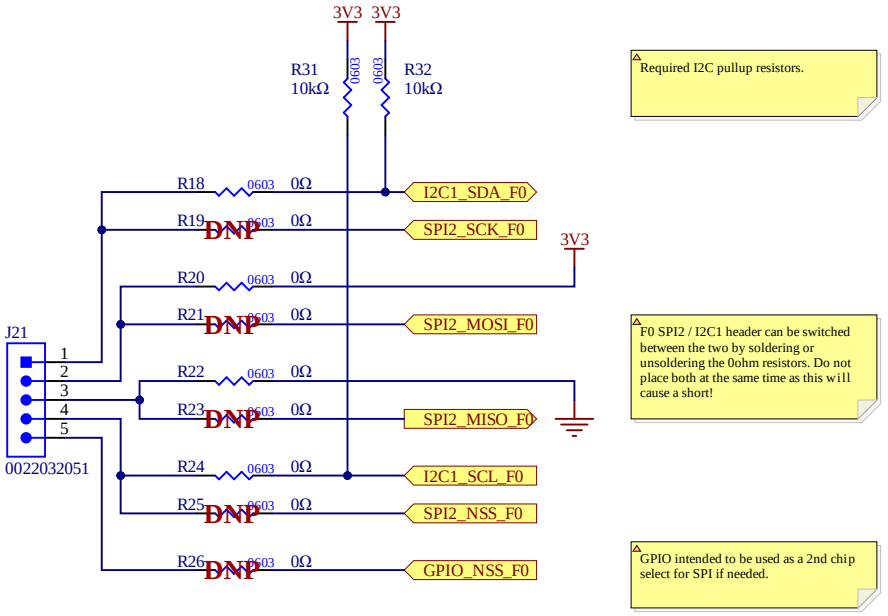
SWD/SWO Connector



SPI/I2C Connector



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Add notes detailling pinout once finalized.

U4

GPIO_NSS_F0
PWM1_F0
PWM2_F0
SWDIO_F0
SWCLK_F0
SPI_NSS_IC
PPM_F0
SPI_SCK_IC
SPI_MOSI_IC
SPI_MISO_IC
I2C1_SCL_F0
I2C1_SDA_F0
SPI2_SCK_F0
SPI2_NSS_F0
PWM3_F0
PWM4_F0
SPI2_MISO_F0
SPI2_MOSI_F0
PWM5_F0
PWM6_F0
PWM7_F0
PWM8_F0
LED1_F0
LED2_F0

PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7 PA8 PA9 PA10 PA11 PA12 PA13 PA14 PA15
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7 PB8 PB9 PB10 PB11 PB12 PB13 PB14 PB15
PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PC8 PC9 PC10 PC11 PC12 PC13
PD2

VDDA VDD VDD VDD VDD VDD
NRST
BOOT0
PC14-OSC32_IN PC15-OSC32_OUT
PF0-OSC_IN PF1-OSC_OUT
VSS VSS VSS VSS VSSA

STM32F030RCT6

3V3

Not using internal ADC so ignoring the requirement of providing VDDA first on startup.

NRST_F0
C39 0603 25V 0.1uF
S2
Internal pull up resistor (40kohms) is present on F0.

BOOT0_F0

Using LSI instead of LSE.

C40 0603 20pF 50v
Y2 8MHz GND TS
C41 0603 20pF 50v

HSE:
CL=((C1*C2)/(C1+C2))+Cstray
CL=15pF, Assume Cstray=5pF,
Assert C1=C2
15pF=((C1*C1)/(2C1))+5pF
C1=C2=20pF

3V3
R27 0603 10kΩ
BOOT0_F0
R28 0603 10kΩ
DNP

F0 Bypass Capacitors

3V3
C34 0603 25V 0.01uF
C35 0603 25V 0.1uF
C36 0603 25V 0.1uF
C37 0805 25V 1uF
C38 0603 25V 4.7uF

Decoupling capacitor placement guide is found in the datasheet on page 42 of the datasheet.

F0 Debugging LEDs

LED2_F0
R29 0603 1kΩ
D7 LTST-C191TBKT-5A

LED1_F0
R30 0603 1kΩ
D8 LTST-C191TBKT-5A

R = (3.3V-2.8V)/(0.5mA) = 1kΩ

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