Seat No. CT-23025

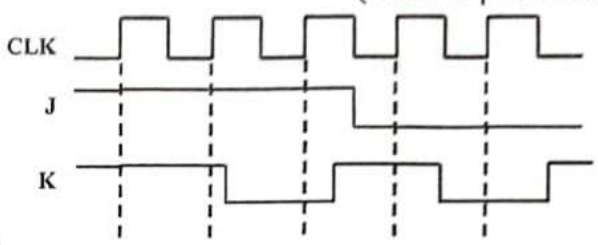
NED UNIVERSITY OF ENGINEERING & TECHNOLOGY

FIRST YEAR (COMPUTER SCIENCE/ GAME & ANIMATION)
SPRING SEMESTER EXAMINATIONS 2024
Batch - 2023

Time: 3 Hours | **Dated:29-07-2024** | **Max.Marks:60**

LOGIC DESIGN & SWITCHING THEORY - CS-251

Question 1: (CLO-1 | 12 Marks)



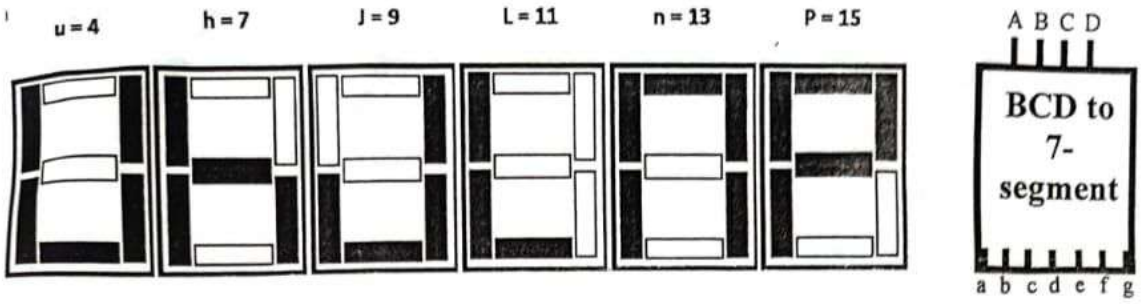
a. *Show* the output of a positive edge triggered JK flipflop the given waveform. Assume the flipflop is initially RESET.
b. ***Differentiate*** between synchronous & asynchronous counters.
c. *Give* excitation / transition table of SR flipflop.
d. *Explain* race-condition with reference to flipflops?
e. *Show* with the help of a diagram how a 4-bit asynchronous counter can be connected to limit it to form a Mod-10 counter.
f. All the flipflops in an asynchronous counter are provided clock inputs. ***Explain*** why they are still considered as asynchronous?

Question 2: (CLO-1 | 12 Marks)

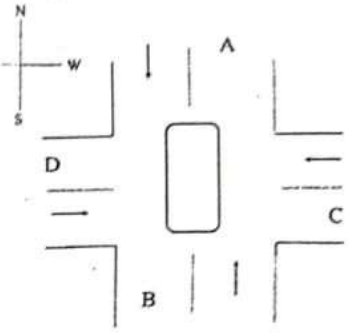
a. *Simplify* using Boolean Algebra:
   i. $F(W,X,Y,Z) = (WX + W\bar{Y})(W + X) + WX(\bar{X} + \bar{Y})$
   ii. $F(A,B,C) = \overline{\overline{(X + \bar{Y}\bar{Z})}(\bar{X}YZ)}$
b. ***Elaborate*** the term 'enable' and ***elaborate*** different kinds of enables in an IC?
c. ***Express*** the following function as a standard sum of minterms and as a standard product of maxterms: $F(A,B,C,D) = C'D + A'B + AD$
d. ***Provide*** the NAND representation of a XOR gate.
e. Consider a 2x1 multiplexer (active high o/p) having select line $S = A$ and data line $D_0 = \bar{B}.C.D$ and $D_1 = \bar{C}.D$. ***Predict*** the output of this multiplexer if $A=1$, $B=1$, $C=1$ and $D=0$? ***Show*** working to support your answer.

Question 3: (CLO-2 | 12 Marks)

a. Using an active low scheme, you need to create logic for displaying alphabets on a 7-segment display. On inputs 4,7,9,11,13 and 15, you need to display alphabets U,h,J,n,L and P on the seven-segment display as displayed in the figure below. ***Customize*** the circuit for led **a** and **b**.



b. Given figure shows the intersection of Shahrah-e-Faisal(SF) with the Shaheed-e-Millat Road (SM) at Baloch Colony. Vehicle detection sensors are placed along Lanes C & D (SF) and A & B (SM). These sensor outputs are LOW(0) when no vehicle is present and HIGH(1) when a vehicle is present in the lane.



The intersection traffic is to be controlled by the following logic:

i. The E-W(east-west) traffic will be green whenever both lanes C and D are occupied.

ii. The E-W light will be green whenever either C or D is occupied but lanes A and B are not occupied.

iii. The N-S(north-south) light will be green whenever lanes A and B are both occupied but C and D are both not occupied.

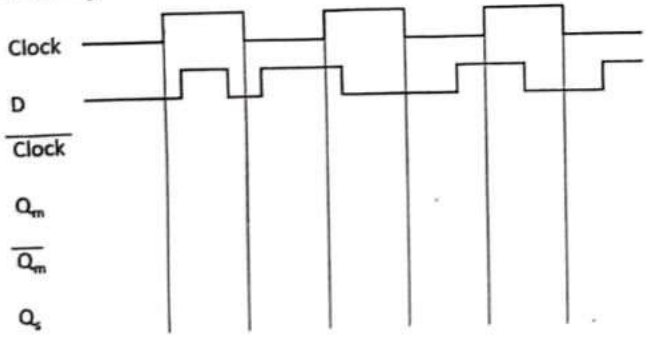
iv. The N-S light will also be green when either A or B is occupies while C and D are both vacant.

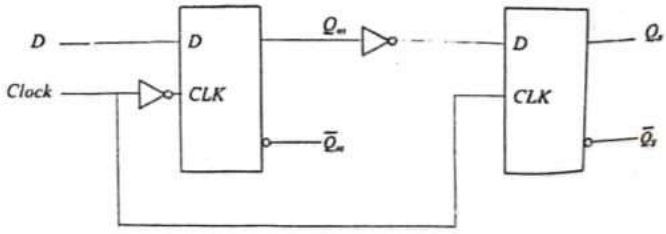
v. The E-W light will be green when no vehicle is present.

Using the outputs of sensors A,B,C and D as inputs, ***design*** a logic circuit that controls the traffic light. There should be two outputs N-S and E-W, which go HIGH when the corresponding light is to be green. Simplify the circuit as much as possible.

Question 4: **(CLO-2 | 12 Marks)**

a. ***Provide*** the characteristic and excitation tables of D flipflop. ***Complete*** the waveform given in the figure below to show the output of the flipflop. The flipflop is negative edge triggered and is initially in SET state.





b. ***Design*** a negative edge triggered Synchronous Mod-8 counter.

Question 5: **(CLO-2 | 12 Marks)**

a. Cascade half adders to form a 3-bit adder/subtractor. (block diagram only).

b. Design a sequential circuit using T flipflop for the state diagram.