SEAT NO. _____

NED UNIVERSITY OF ENGINEERING & TECHNOLOGY

SECOND YEAR FALL SEMESTER (BACHELOR OF SCIENCE IN COMPUTER SCIENCE AND INFORMATION TECHNOLOGY)
EXAMINATIONS 2019
BATCH 2018

Time: 3 Hours

Dated:06-02-2020
Max.Marks:60

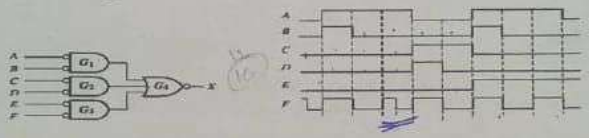
Logic Design & Switching Theory - CS-251

NOTE: Attempt ALL questions

Q.1 Give answers to the following, also draw diagrams where required. (08)

(a) Explain the difference between analog quantity and digital quantity
(b) Write binary numbers from 010011 to 011111
(c) Write Hex numbers from 99 to 100
(d) What is the difference between level and edge triggering?
(e) Draw a pulse train and label it?

Q.2 (a) Make truth table according to the given waveforms and determine the output waveform for the following circuit (08)



(b) What are universal gates, draw equivalent circuits by using NOR universal gate to produce different(AND , OR , NOT and NAND) logics.

Q.3 (a) Write all the rules of Boolean algebra (08)
(b) Draw logic diagrams and truth tables
(i) A(BC + BC) + AC = A(BC) + AC
(ii) [AB'(C+BD) + A'B'] C = B'C

Q.4 (a) Draw diagram and truth tables of XOR and XNOR gates (06)
(b) Draw the complete logic diagram and truth table of Full Adder.

Q.5 (a) Draw diagram of 4-bit decoder and describe it (06)
(b) Draw diagram of Decimal to BCD encoder and describe it

Q.6 (a) The sequence 1011 is applied to the input of a 4-bit serial shift register that is initially cleared. What is the state of the shift register after three clock pulses? (08)
(b) Draw diagram of 4-bit up-counter and explain it

Q.7 Draw diagram and explain working of Master-Slave JK flip flop also draw waveforms of all conditions according to truth table of JK flip flop (08)

- MIDs (1)
- counters (3)
- problems (2)
- tablet bottleneck.

NED UNIVERSITY OF ENGINEERING & TECHNOLOGY
SECOND YEAR FALL SEMESTER (BACHELOR OF SCIENCE IN COMPUTER SCIENCE AND INFORMATION TECHNOLOGY)
EXAMINATIONS 2018
BATCH 2017

Time: 3 Hours **Dated:12-02-2019** **Max.Marks:60**

Logic Design & Switching Theory - CS-251

NOTE: Attempt ALL questions

SECTION A

Q.1 Give answers to the following, also draw diagrams where required. (07)

more precise bcs 3.0 real values

(a) Why digital logic is better than analog system
(b) Write binary number sequence from 010011 to 011111
(c) Write hex number sequence from 99 to 100
(d) What is the difference between level and edge triggering?
(e) Show method to calculate the 2's complement of 60.

CP-074

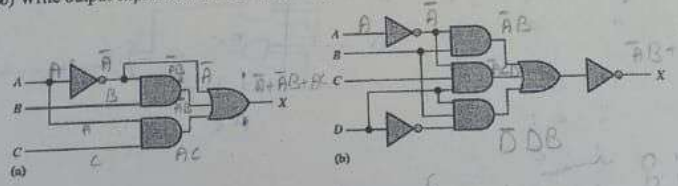
Q.2 (a) Convert following binary numbers to decimal numbers (07)
(1) 100001 (2) 010101
(3) 101010 (4) 111100

(b) What are universal gates, draw equivalent circuits using NAND universal gate to produce different (AND , OR , NOT and NOR) logics. (08)

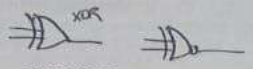
NOT NOR

Q.3 (a) Draw logic diagrams and truth tables
(i) (AB + AC)' + A'B' C
(ii) [AB' (C + BD) + A'B'] C

(b) Write output expression from the following circuits, also write complete truth tables.



A B	XOR	XNOR
0 0	0	1
0 1	1	0
1 0	1	0
1 1	0	1



SECTION B

Q.4 (a) Draw diagram and truth tables of XOR and XNOR gates (08)
(b) Draw the complete logic diagram of 4 input Multiplexer and describe its working

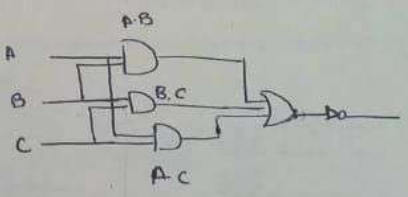
Q.5 (a) Draw diagram of 4-bit decoder and describe it (08)
(b) Draw diagram of Decimal to BCD encoder and describe it

Q.6 (a) Draw block diagram of up-counter and describe its working starting from Count 0000 to 0004. (08)
(b) What is a Shift register, draw diagram of a 4 bit shift register.
The sequence 1011 is applied to the input of a 4-bit shift register that is initially cleared. What is the state of the shift register after three clock pulses?
reset 0, 1

Q.7: Draw diagram and explain working of Master-Slave JK flip flop also draw waveforms of all Four Conditions according to truth table of JK flip flop (08)

Q.8: In a certain chemical processing plant, a liquid chemical is used in a manufacturing process. The chemical is stored in three different tanks. A level sensor in each tank produces a LOW voltage when the chemical level drops below 33% of the full. Design a circuit that monitors the chemical level in each tank and indicates when the level in any of the two tanks drops below 33% of the full. Show the logic diagram and explain it. (06)

A	B	C	output
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0



Ms. Maha Zaka SEAT NO. AI-22001

NED UNIVERSITY OF ENGINEERING & TECHNOLOGY
FIRST YEAR (DATA SCIENCE/ ARTIFICIAL INTELLIGENCE/ CYBER SECURITY)
SPRING SEMESTER EXAMINATIONS 2023
Batch 2022

Time : 3 Hours **Dated : 09-AUG-23**
Max Marks : 60

Logic Design & Switching Theory - CS-251

Note: Attempt all questions.

Q-1 (a) Simplify using Boolean Algebra. CLO-2, C3 , PLO-2 /5

i. $A = XY + X(Y+Z) + Y(Y+Z)$ ii. $\bar{X}\bar{Y}Z+YZ+XZ$

(b) Construct logic circuit for the given logic expression.
CLO-2, C3 , PLO-2 /5

i. $AB + BC(B + C)$ ii. $(A+\bar{B})C$

(c) Minimize the following boolean function using K-map
CLO-1 , C2 , PLO- 1 /10

i. $Y=\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC$

ii. $F(A, B, C, D) = \Sigma m(0, 1, 3, 5, 7, 8, 9, 11, 13, 15)$

Q-2 (a) Construct 4-bit binary Adder-Subtractor assuming 4 bit numbers A & B CLO-1 , C2 , PLO- 1 /5

(b) Implement 3 to 8 decoder using 2 to 4 decoders.
CLO-1 , C2 , PLO- 1 /5

(c) Implement the following higher-order Multiplexer using lower-order Multiplexers . CLO-1 , C2 , PLO- 1 /5
8x1 Multiplexer

Q-3 (a) Design a 3 bit Asynchronous UP counter, assuming clock to be negative edge triggered CLO-1 , C2 , PLO- 1 /5

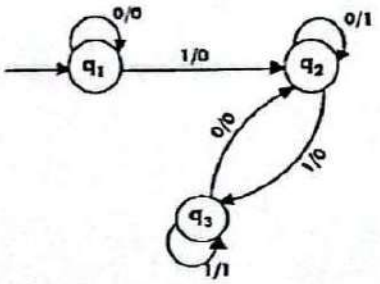
(b) What are the 2 switching problems of **SR Flipflop**

CLO-2, C3 , PLO-2 /5

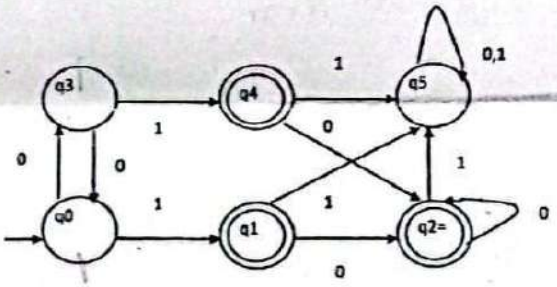
PTO

(c) Which flipflop is called universal flipflop, draw its block diagram, circuit diagram and truth table. CLO-2, C3 , PLO-2 /5

Q-4 (a) Convert the following Mealy machine into equivalent Moore machine. CLO-1 , C2 , PLO- 1 /5



(b) Consider the following DFA shown in figure. Perform state minimization. CLO-1 , C2 , PLO- 1 /5



SEAT NO. CT-21096

NED UNIVERSITY OF ENGINEERING & TECHNOLOGY

FIRST YEAR(BACHELOR OF SCIENCE IN COMPUTER SCIENCE)
SPRING SEMESTER EXAMINATIONS 2022
BATCH 2021

Time: 3 Hours

Dated:20-08-2022
Max.Marks:60

Logic Design & Switching Theory - CS-251

Instructions:

- Attempt **ALL** questions
- Make logical assumptions where necessary and clearly state them.
- Calculators are allowed but show all intermediate calculations to earn full credit.

Q1) Minimize the following Boolean function using K-Map — 10 Marks

i) $F(P,Q,R,S)=\sum m(0,1,3,5,7,8,9,11,13,15)$ (05 marks)
ii) $F(A,B,C,D)=\sum m(3,4,5,7,9,13,14,15)$ (05 marks)

Q2) Simplify the following: — 12 Marks

i) $\bar{A}\bar{B}C + \overline{(A+B+C)} + \bar{A}\bar{B}\bar{C}D$ (03 marks)
ii) $AB + AC + A\bar{C}$ (03 marks)
iii) $(A+\bar{B})(A+C)$ (03 marks)
iv) $1.C + \bar{B}C$ (03 marks)

Q3) Draw the logic circuit for the given logic expression — 12 Marks

i) $Q=\overline{\overline{\bar{C}.B} + A}$ (04 marks)
ii) $R=[A(C+D)]' + BE$ (04 marks)
iii) $S=(A.B.C) + A(\bar{B} + \bar{C})$ (04 marks)

Q4) Perform the following: — 06 Mark

i) Subtraction using **1's complement 10101 – 10111** (03 marks)
ii) Addition using **2's complement -1101 and -1110 in 5 bit** (03 marks)

Q5a) Write down the range of: — 06 Marks

i) Sign Magnitude Form (02 marks)
ii) 1's Complement (02 marks)
iii) 2's Complement (02 marks)

Q5b) Draw the logic symbol, truth table and logic expression of **XOR & XNOR** — 06 Marks

Q6) Convert the following: — 08 Marks

i) **1BC Hexadecimal** number to **Octal** (02 marks)
ii) **011011 Binary** number to **Octal** (02 marks)
iii) **1B7E Hexadecimal** number to **Decimal** (02 marks)
iv) **670 Decimal** number to **Octal** (02 marks)

$A(\bar{C}D + BC) + \bar{A}(B\bar{C} + CD) + BD$

$A(BC + D) + (CD + B) +$

NED UNIVERSITY OF ENGINEERING & TECHNOLOGY

FIRST YEAR(BACHELOR OF SCIENCE IN
COMPUTER SCIENCE & INFORMATION TECHNOLOGY)
SPRING SEMESTER EXAMINATIONS 2021
BATCH 2020

Dated:30-08-2021

Time: 3 Hours

Max.Marks:60

Logic Design & Switching Theory - CS-251

Instructions:

i. **Attempt all parts of a question together.**
ii. State the assumptions clearly, wherever required.
iii. All the work must be legible and clear.
iv. Calculator is not allowed.

QUESTION NUMBER: 1

(10 Marks)

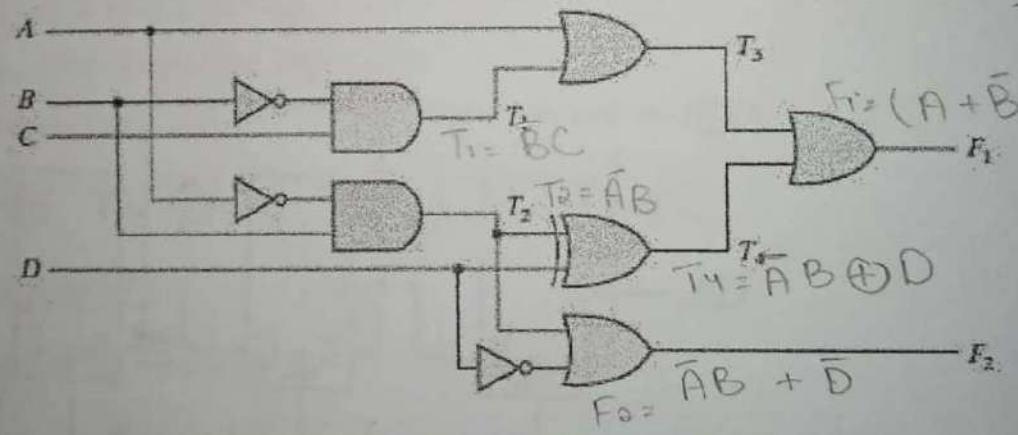
a) Express the following.

i. $(F7)_{16}$ to its equivalent in decimal system. [1]

ii. Value of the even parity bit P_{even} for the number $(0110010101111001)_2$. [1]

iii. Equivalency of $A + \bar{A}.B = A + B$. [1]

b) Consider the circuit given below.



i. Express the Boolean expressions for T_1 through T_4, as well as the outputs F_1 and F_2 as a function of the four inputs. [2]

ii. Illustrate the truth table with input binary combinations, binary values for T_1 through T_4 and outputs F_1 and F_2 in the table. [2]

iii. Minimize F_2 and illustrate the minimized logic circuit. [3]

(10 Marks)

QUESTION NUMBER: 2

a) Construct a three-bit Gray-to-Binary converter. [4]

b) Demonstrate the combinational logic for a printer which prints when there are documents in the queue and the paper is not jammed or the ink is not low. [3]

c) Implement the following Boolean Function using Multiplexer. [3]
$F(A,B,C,D) = \Sigma\,(0,2,4,6,8,10,12,14)$

(10 Marks)

QUESTION NUMBER: 3

a) Construct a Hexadecimal to Seven Segment Decoder. [5]

b) Construct a two's complementor for BCD numbers. [5]

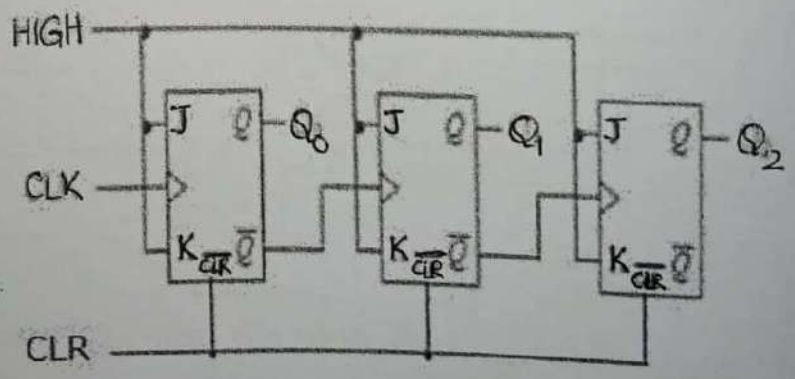
(10 Marks)

QUESTION NUMBER: 4

a) Diagram the three-bit Gray-to-Binary converter of Question 2(a) using *PLA*. [2]
(*No need to repeat the truth table or equations here; use directly*).

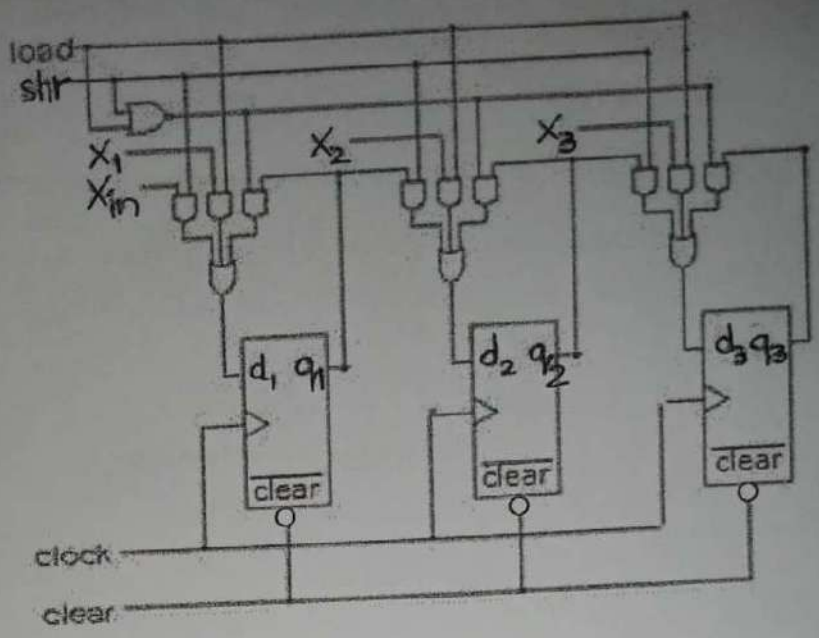
b) Examine the following figures to identify the function and illustrate the working.

i. [4]



[4]

ii.



(10 Marks)

QUESTION NUMBER: 5

a) Interpret the following conditions to produce a sequential circuit with two D flip-flops A and B, and one input X. When $X = 0$, the state of the circuit remains the same. When $X = 1$, the circuit goes through the state transitions from 00 to 01, to 11, to 10, back to 00, and repeats. [5]

b) Suppose you have purchased a certain memory with total capacity of 2 megabytes. If this memory is a nibble long, deduce the following.

i. Number of address lines. [1]

ii. Number of input and output lines. [1]

iii. Number of words. [1]

iv. Basic structure of this memory. [2]

(10 Marks)

QUESTION NUMBER: 6

a) For the following state table

Present State	Next State		Output	
	$X=0$	$X=1$	$X=0$	$X=1$
a	f	b	0	0
b	d	c a	0	0
c	f	e b	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h d	0	1
h	g	a	1	0

d = h
b = e
a = c

i. Produce the corresponding state diagram. [1.5]

ii. Compute the reduced state table. [2]

iii. Produce the state diagram corresponding to the reduced state table. [1.5]

b) Analyze the reduced state machine of part (a) to prepare a sequential circuit with assignment 000, 001, 011, 100, 110, 111. [5]

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N.E.D. University of Engineering & Technology
Department of Computer Science & Information Technology

Quiz # 01 Paper B

24/3/21

Course Title: Logic Design & Switching Theory
Class: FCIT-(A)
Date: 25-March-2020
Maximum Marks: 10

Course Code: CS-251
Instructor: Engr. Huma Tabassum
Time Allowed: 20 Minutes
Marks Obtained: [redacted]

Student Name: [redacted]
Roll Number: [redacted]

1. Convert the following into required number system.
   a. $(47.25)_{10} = (?)_2$

2	47	
2	23	1
2	11	1
2	5	1
2	2	1
	1	0

$0.25 \times 2 = 0.5 \rightarrow 0$
$0.5 \times 2 = 1 \rightarrow 1$

$= (101111.01)_2$

   b. $(A8)_{16} = (?)_{10}$

A → 10, 8 → 8

$= (16^1 \times 10) + (16^0 \times 8) = (168)_{10}$

2. Express $(10100101)_2$ in decimal system using sign-magnitude system and one's complement system.

SIGN-MAGNITUDE SYSTEM:

Since the sign bit is 1, the number will be negative
Consider 7 magnitude bits

0100101
6 5 4 3 2 1 0

$= (2^5 \times 1) + (2^2 \times 1) + (2^0 \times 1) = 37$

Since the sign bit is 1
$= -37$

one's complement → on back side

3. Indicate the following.
   a. BCD equivalent of $(613)_{10}$ 0110 0001 0011
   b. Gray equivalent of $(2)_{10}$ 0011

4. Identify the final quotient of the signed numbers $(0110)_2 \div (0011)_2$ using two's complement system.

[redacted]

N.E.D. University of Engineering & Technology

Department of Computer Science & Information Technology

10 17/7/21

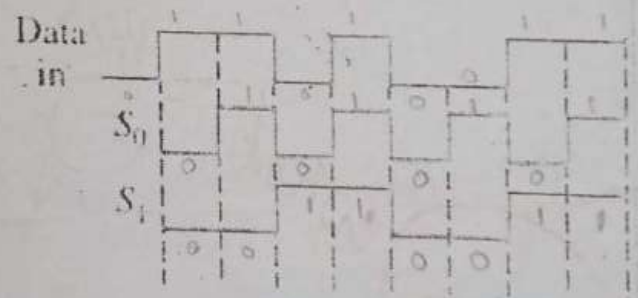
Quiz # 03 Paper A

Course Title: Logic Design & Switching Theory
Course Code: CS-251
Class: FCIT-(A)
Instructor: Engr. Huma Tabassum
Date: 14-July-2021
Time Allowed: 20 Minutes
Maximum Marks: 10
Marks Obtained:

Student Name: [redacted]
Roll Number: [redacted]

1. Construct a circuit for a light fixture controlled by two switches, where flipping one of the switches turns the light on when it is off and turns it off when it is on. 5/5

2. The data-input waveform (Data in) and data-select inputs (S_0 and S_1) are shown in figure. Determine the data-output waveforms on D_0 through D_3 for the 1 x 4 demultiplexer. /5



FUNCTION TABLE:

S_1 | S_0 | D_0 | D_1 | D_2 | D_3

input lines = 1

[redacted]

N.E.D. University of Engineering & Technology

Department of Computer Science & Information Technology

10 17/7/21

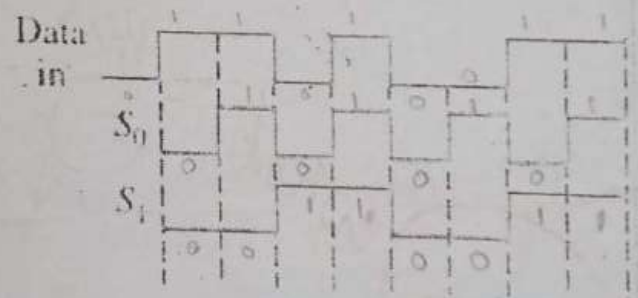
Quiz # 03 Paper A

Course Title: Logic Design & Switching Theory
Course Code: CS-251
Class: FCIT-(A)
Instructor: Engr. Huma Tabassum
Date: 14-July-2021
Time Allowed: 20 Minutes
Maximum Marks: 10
Marks Obtained:

Student Name: [redacted]
Roll Number: [redacted]

1. Construct a circuit for a light fixture controlled by two switches, where flipping one of the switches turns the light on when it is off and turns it off when it is on. 5/5

2. The data-input waveform (Data in) and data-select inputs (S_0 and S_1) are shown in figure. Determine the data-output waveforms on D_0 through D_3 for the 1 x 4 demultiplexer. /5



FUNCTION TABLE:

S_1 | S_0 | D_0 | D_1 | D_2 | D_3

input lines = 1

Ms. Rukhsar Zaka

SEAT NO. CT - 21005

NED UNIVERSITY OF ENGINEERING & TECHNOLOGY

FIRST YEAR(BACHELOR OF SCIENCE IN COMPUTER SCIENCE)
SPRING SEMESTER EXAMINATIONS 2022
BATCH 2021

Time: 3 Hours

Dated:20-08-2022
Max.Marks:60

Logic Design & Switching Theory - CS-251

Instructions:

- Attempt **ALL** questions
- Make logical assumptions where necessary and clearly state them.
- Calculators are allowed but show all intermediate calculations to earn full credit.

Q1) Minimize the following Boolean function using K-Map 10 Marks

i) $F(P,Q,R,S)=\sum m(0,1,3,5,7,8,9,11,13,15)$ (05 marks)
ii) $F(A,B,C,D)=\sum m(3,4,5,7,9,13,14,15)$ (05 marks)

Q2) Simplify the following: 12 Marks

i) $\bar{A}\bar{B}C + \overline{(A+B+C)} + \bar{A}\bar{B}\bar{C}D$ (03 marks)
ii) $AB + AC + A\bar{C}$ (03 marks)
iii) $(A+\bar{B})(A+C)$ (03 marks)
iv) $1.C + \bar{B}C$ (03 marks)

Q3) Draw the logic circuit for the given logic expression 12 Marks

i) $Q=\overline{\bar{C}.B} + A$ (04 marks)
ii) $R=[A(C+D)]' + BE$ (04 marks)
iii) $S=(A.B.C) + A(\bar{B} + \bar{C})$ (04 marks)

Q4) Perform the following: 06 Mark

i) Subtraction using **1's** complement **10101 – 10111** (03 marks)
ii) Addition using **2's** complement **-1101** and **-1110** in **5** bit (03 marks)

Q5a) Write down the range of: 06 Marks

i) Sign Magnitude Form (02 marks)
ii) 1's Complement (02 marks)
iii) 2's Complement (02 marks)

Q5b) Draw the logic symbol, truth table and logic expression of **XOR & XNOR** 06 Marks

Q6) Convert the following: 08 Marks

i) **1BC Hexadecimal** number to **Octal** (02 marks)
ii) **011011 Binary** number to **Octal** (02 marks)
iii) **1B7E Hexadecimal** number to **Decimal** (02 marks)
iv) **670 Decimal** number to **Octal** (02 marks)

SEAT NO. _____

NED UNIVERSITY OF ENGINEERING & TECHNOLOGY

FIRST YEAR(BACHELOR OF SCIENCE IN
COMPUTER SCIENCE & INFORMATION TECHNOLOGY)
SPRING SEMESTER EXAMINATIONS 2021
BATCH 2020

Dated:30-08-2021

Time: 3 Hours

Max.Marks:60

Logic Design & Switching Theory - CS-251

Instructions:

i. **Attempt all parts of a question together.**
ii. State the assumptions clearly, wherever required.
iii. All the work must be legible and clear.
iv. Calculator is not allowed.

QUESTION NUMBER: 1

(10 Marks)

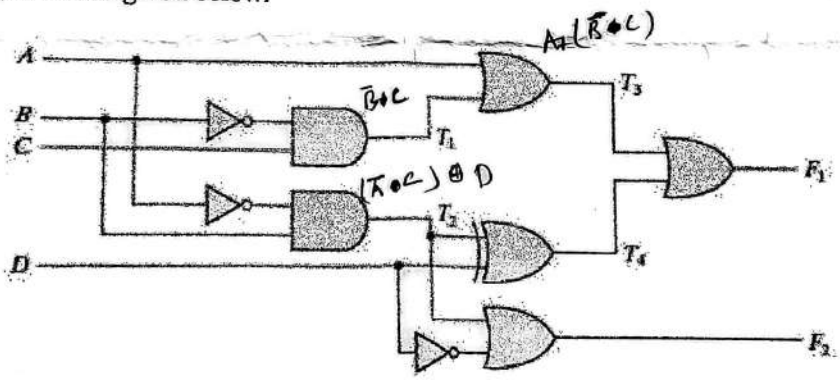
a) Express the following.

i. $(F7)_{16}$ to its equivalent in decimal system. [1]

ii. Value of the even parity bit P_{even} for the number $(011001010111001)_2$. [1]

iii. Equivalency of $A + \overline{A}.B = A + B$. [1]

b) Consider the circuit given below.



i. Express the Boolean expressions for T_1 through T_4, as well as the outputs F_1 and F_2 as a function of the four inputs. [2]

ii. Illustrate the truth table with input binary combinations, binary values for T_1 through T_4 and outputs F_1 and F_2 in the table. [2]

iii. *Minimize F_2 and illustrate the minimized logic circuit.* [3]

QUESTION NUMBER: 2 **(10 Marks)**

a) Construct a three-bit Gray-to-Binary converter. [4]

b) Demonstrate the combinational logic for a printer which prints when there are documents in the queue and the paper is not jammed or the ink is not low. [3]

c) Implement the following Boolean Function using Multiplexer. [3]
$F(A,B,C,D) = \Sigma\,(0,2,4,6,8,10,12,14)$

QUESTION NUMBER: 3 **(10 Marks)**

a) Construct a Hexadecimal to Seven Segment Decoder. [5]

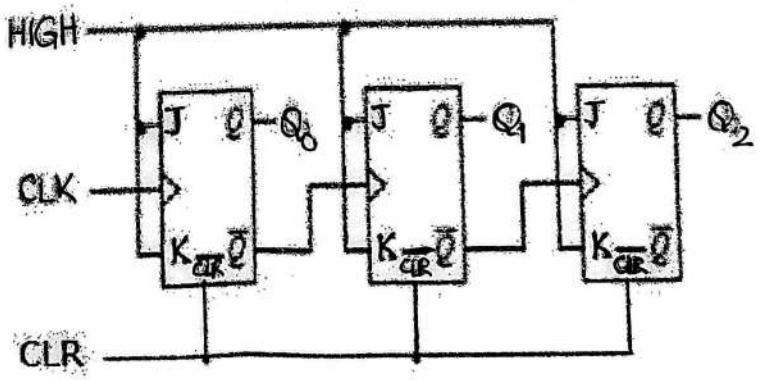
b) Construct a two's complementor for BCD numbers. [5]

QUESTION NUMBER: 4 **(10 Marks)**

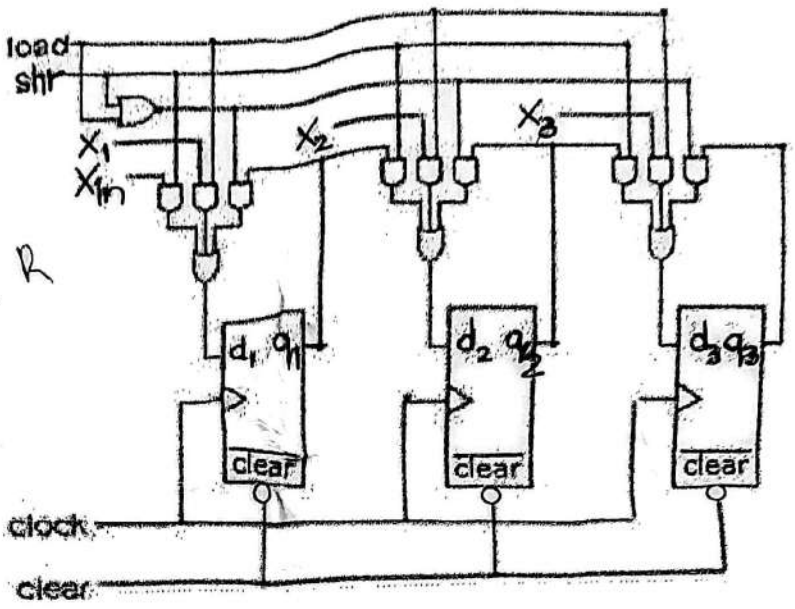
a) Diagram the three-bit Gray-to-Binary converter of Question 2(a) using *PLA*. [2]
(No need to repeat the truth table or equations here; use directly).

b) Examine the following figures to identify the function and illustrate the working.

i. [4]



ii. [4]



QUESTION NUMBER: 5 (10 Marks)

a) Interpret the following conditions to produce a sequential circuit with two *D* flip-flops *A* and *B*, and one input *X*. When $X = 0$, the state of the circuit remains the same. When $X = 1$, the circuit goes through the state transitions from 00 to 01, to 11, to 10, back to 00, and repeats. [5]

b) Suppose you have purchased a certain memory with total capacity of 2 megabytes. If this memory is a nibble long, deduce the following.

i. Number of address lines. [1]

ii. Number of input and output lines. [1]

iii. Number of words. [1]

iv. Basic structure of this memory. [2]

QUESTION NUMBER: 6 (10 Marks)

a) For the following state table

Present State	Next State		Output	
	$X=0$	$X=1$	$X=0$	$X=1$
a	f	b	0	0
b	d	c	0	0
c	f	b	0	0
d	g	a	1	0
e	d	e	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

i. Produce the corresponding state diagram. [1.5]

ii. Compute the reduced state table. [2]

iii. Produce the state diagram corresponding to the reduced state table. [1.5]

b) Analyze the reduced state machine of part (a) to prepare a sequential circuit with assignment 000, 001, 011, 100, 110, [illegible]. [5]

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