Ubaid Bakhtiar

Maryland, USA ubaidb@umd.edu (301)768-5256 /in/ubaid-bakhtiar /ubaidb

RESEARCH SUMMARY

My research focuses on optimizing resource utilization to accelerate the throughput and latency in various computing architectures, including CPUs, GPUs, and FPGAs, while maintaining area and timing constraints. Utilizing dynamic reconfiguration, hardware/software co-design, and novel architectural support, my research encompasses applications across diverse domains, from sparse algebra to scientific computing and large language models (LLMs).

EDUCATION

Ph.D. Electrical and Computer Engineering | University of Maryland-College Park | Fall, 2022- Present

BSc. Electrical Engineering | Lahore University of Management Sciences (LUMS) | 2018-2022

PUBLICATIONS

Acamar: A Dynamically Reconfigurable Scientific Computing Accelerator for Robust Convergence and Minimal Resource Underutilization | Spring 2024

• A dynamically reconfigurable approach to offer robust convergence for diverse datasets and improve the resource utilization of the sparse matrix-vector multiplication operation in scientific computing algorithms. **[Published in MICRO-2024]**

RESEARCH PROJECTS

Pipirima: Predicting Patterns in Sparsity to Accelerate Matrix Algebra | Fall 2023

• A novel approach to accelerate sparse matrix algebra using sparse matrix structural predictions was presented and simulated using a cycle-accurate simulator that showed latency speed up of upto ~120x and ~20x over state-of-the-art sparse accelerators; ExTensor and Tensaurus respectively.

Trace-Driven Processor and On-Chip Memory Simulator | Fall 2022

• A trace-driven out of order RV-32IF pipeline and cache organization simulator for unified as well as instruction and data cache was built in this project. The simulator also catered for cache coherence protocols, evaluating the performance on multi-core system.

RELEVANT EXPERIENCE

Graduate Research Assistant | Computer Architecture and Systems Lab | University of Maryland | May, 2023-Present

• Research Advisor: Dr. Bahar Asgari

• Research Area: Computer Architecture and Domain Specific Designs

• Crafting dynamically reconfigurable domain-specific architecture designs to tackle computational challenges and devising methods to enhance their performance as well as simulation and prototyping on modern architectures, i.e. CPUs, GPUs, FPGAs

Technical Content Engineer | Educative.io | Lahore, Pakistan | Summer, 2022

• Adeptly managed courses on the Educative platform, with a strong emphasis on proficiently utilizing Docker, Linux, Python, and C/C++ programming.

• This role also provided valuable exposure to JavaScript and databases through interactions with the platform.

COURSEWORK

Programming Languages and Computer Architecture | Domain Specific Architecture | Digital Computer Design | Compilers and Optimizations

University of Maryland-College Park

Computer Architecture | Digital System Design | Embedded Systems | VLSI Design | Machine Learning

Lahore University of Management Sciences

SKILLS

Topics	HW/SW Co-design, CPUs, GPUs, Embedded Systems, Data Structures, AI/ML
Programming Languages	C/C++, Python, RTL (Verilog), OpenCL, MIPS/RISC Assembly, MATLAB
Hardware Platforms	AMD Xilinx FPGAs and ZYNQ SoC, RISC, ASIC, Friendly ARM
Software	GPGPU-SIM, Xilinx Vitis, CACTI, Synopsys DC, Nvidia Nsight Compute, Docker, Linux