Ubaid Bakhtiar

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Ph.D. Candidate, Electrical and Computer Engineering, University of Maryland, College Park

Research Summary

General-purpose processors and specialized accelerators often fail to achieve the theoretical gains offered by sparsity due to underutilized hardware resources. To close the gap between peak and achievable performance, my research focuses on developing novel data scheduling, multi-tenancy, and dynamic reconfiguration techniques and integrate into sparse applications accelerators to mitigate the high resource underutilization and consequently, fully exploit the benefits of sparsity. My research has resulted in first-author publications in top-tier computer architecture conferences like MICRO and DAC.

Core Competencies

- **Hardware Prototyping:** Hands-on experience in developing custom accelerators for sparse scientific and machine learning workloads. Skilled in high-level synthesis, placement, and routing on FPGA fabrics, with extensive prototyping of baseline and novel architectures.
- **Simulations:** Development of in-house, cycle-accurate simulators to evaluate architectural tradeoffs in data scheduling, multi-tenancy, and sparsity-aware execution. Experience of performance analysis frameworks such as Xilinx Runtime, CACTI, and Synopsys DC, NVIDIA Nsight Comput and Intel VTune Profiler.
- **Algorithm & Architecture Co-Design:** Identified bottlenecks in sparse stencil solvers and gen AI workloads, bridging algorithmic inefficiencies with architectural design choices to mitigate resource underutilization.
- **Performance optimization.** Expertise in analyzing and optimizing dataflow, memory bandwidth utilization, and compute-resource mapping to close the gap between theoretical peak and achieved performance in sparse accelerators.
- **Tools & Frameworks:** C/C++, Python, Verilog, Xilinx Vitis, TAPA, Rapidstream.

Education

Ph.D. in Electrical and Computer Engineering Aug 2022 – Present
University of Maryland, College Park
B.Sc in Electrical Engineering August 2018 — May 2022
Lahore University of Management Sciences (LUMS), Pakistan

Publications

- **Ubaid Bakhtiar**, Amirmahdi Namjoo and Bahar Asgari. **Chasoň: Supporting Cross HBM Channel Data Migration to Enable Efficient Sparse Algebraic Acceleration**
  International Symposium on Microarchitecture (MICRO) 2025 — Acceptance Rate: 20.7%
- **Ubaid Bakhtiar**, Helya Hosseini and Bahar Asgari. **Acamar: A Dynamically Reconfigurable Scientific Computing Accelerator for Robust Convergence and Minimal Resource Underutilization**
  International Symposium on Microarchitecture (MICRO) 2024 — Acceptance Rate: 22.7%
- **Ubaid Bakhtiar**, Donghyeon Joo and Bahar Asgari. **Pipirima: Predicting Patterns in Sparsity to Accelerate Matrix Algebra**
  Design Automation Conference (DAC) 2025 — Acceptance Rate: 23%
- Helya Hosseini, **Ubaid Bakhtiar**, Donghyeon Joo and Bahar Asgari. **Segin: Synergistically Enabling Fine-Grained Multi-Tenant and Resource Optimized SpMV**
  IEEE Computer Architecture Letters (CAL) 2025 — Acceptance Rate: 20%
- **Ubaid Bakhtiar**, Sanjali Yadav, Donghyeon Joo, Ramyad Hadidi and Bahar Asgari. **Lyra: Mapping Unstructured Sparse LLMs to FPGAs Using Bitmap-Based Dynamic Matrix Partitioning**
  Under review in International Symposium on High-Performance Computer Architecture (HPCA) 2026
- Helya Hosseini, **Ubaid Bakhtiar**, Donghyeon Joo and Bahar Asgari. **Lepus: Leveraging Sparsity to Upend Its Challenges**
  Under review in International Symposium on High-Performance Computer Architecture (HPCA) 2026

Research Experience

- **Research Assistant** – Computer Architecture and Systems Lab (CASL), UMD May 2023 – Present
  - Research Area: Computer Architecrure and Domain Specific Designs
  - Research Advisor: Dr. Bahar Asgari
  - Crafting domain-specific architecture designs to tackle computational challenges in sparse applications and devising methods to enhance their performance as well as simulation and prototyping on modern architectures, i.e. CPUs, GPUs, FPGAs

Relevant Coursework

- Domain Specifc Arhcitecture
- Digital Computer Design
- Programming Languages and Computer Architecture
- Machine Learning
- Systems for Machine Learning

Technical Skills

- **Languages:** C, C++, Verilog, Python, OpenCL, MIPS/RISC Assembly, MATLAB
- **Hardware Platforms:** AMD Alveo Accelerator Cards, AMD ZYNQ SoC, RISC, CPU, GPU
- **Frameworks:** High-level synthesis, Xilinx Vitis, Xilinx Runtime TAPA, Rapidstream, Intel MKL, Nvidia cuSparse
- **Simulations:** In-house cycle-accurate simulator, CACTI, Synopsys DC, GPGPU-SIM, Nvidia Nsight Compute
- **Deployment:** Linux CLI, Docker, Jupyter, Git
- **Topics:** HW/SW Co-design, Hardware for generative AI, Scientific computing accelerator, AI/ML

Awards and Honors

- **Winner 2-Minute Video Contest**, Student Young Fellow at DAC 2025.
- **Student Travel Grant**, ACM/IEEE 57th International Symposium on Microarchitecture (MICRO 2024)
- **Summer Research Fellowship**, University of Maryland-College Park (Summer 2023)
- **Dean's Honor List Award**, LUMS (2019-20)

Professional Services

- Student Volunteer @ SPICE: A Workshop Co-Located with International Symposium on Microarchitecture 2025
- Student Volunteer @ SPICE: A Workshop Co-Located with International Symposium on Microarchitecture 2025
- Graduate Teaching Assistant, Advance Digital Computer Design, University of Maryland-College Park (Fall 2023)
- Graduate Teaching Assistant, Advance Digital Computer Design, University of Maryland-College Park (Fall 2022, Spring 2023)
- Teaching Assistant Feedback Control Systems, LUMS (Spring 2022)
- Teaching Assistant Electromagnetic Fields and Waves, LUMS (Fall 2021)
- Teaching Assistant Engineering Models, LUMS (Fall 2021)
- Teaching Assistant Engineering Models, LUMS (Fall 2021)