BER Measurement

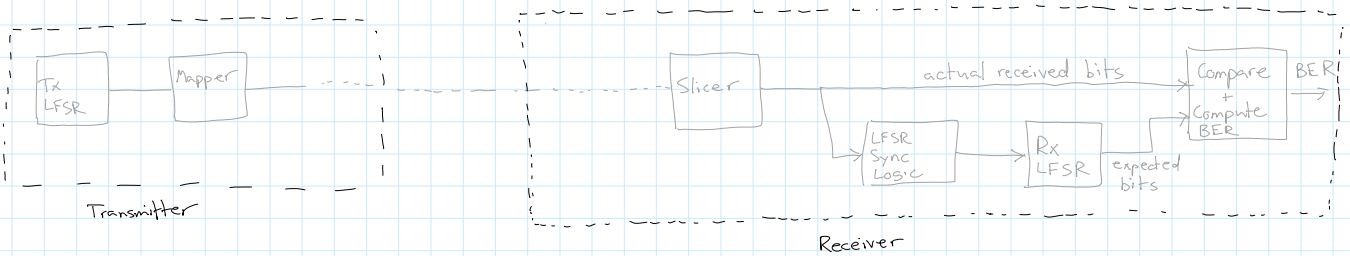
- general concept : tx data → Transmitter → Receiver → rx data → Compare → BER

$$BER = \frac{\#\text{ bits in error}}{\#\text{ bits sent}}$$

Challenge : How can the receiver know what the original tx data bits were?
→ Not practical to run a wire in parallel w/ entire communication system as above.

Approach used in D4:
- build a copy of the Tx LFSR in the receiver
- synchronize the two LFSRs (this is the tricky part!)
- compare bits from slicer to those from receiver LFSR

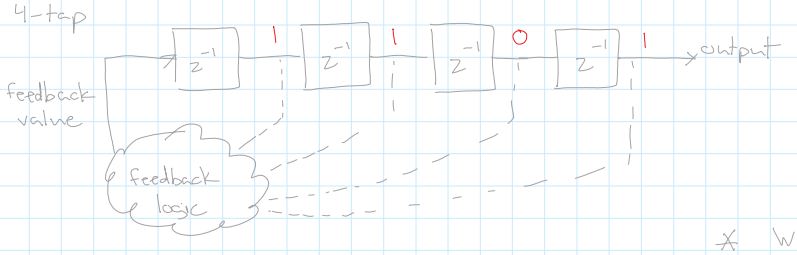
High-level overview:



Key Principles for Synchronizing LFSRs:

- Two LFSRs with the same structure (length + feedback taps) generate the same output sequence
- If the two LFSRs have the same internal state at time n, they will produce the same outputs forever
- The N values in the N registers of an N-tap LFSR reflect the next N output bits from the LFSR

ex. 4-tap



Clock	Output
N	1
N+1	0
N+2	1
N+3	1

✗ What were the values in the 4 registers at time N?

→ Note that knowing these 4 bits lets us predict the LFSR's output at time N+4, N+5, N+6... ∞

When building our BER measurement circuit, we assume that the first few bits out of the slicer are correct.

→ Can use these bits to load the registers of the Rx LFSR.

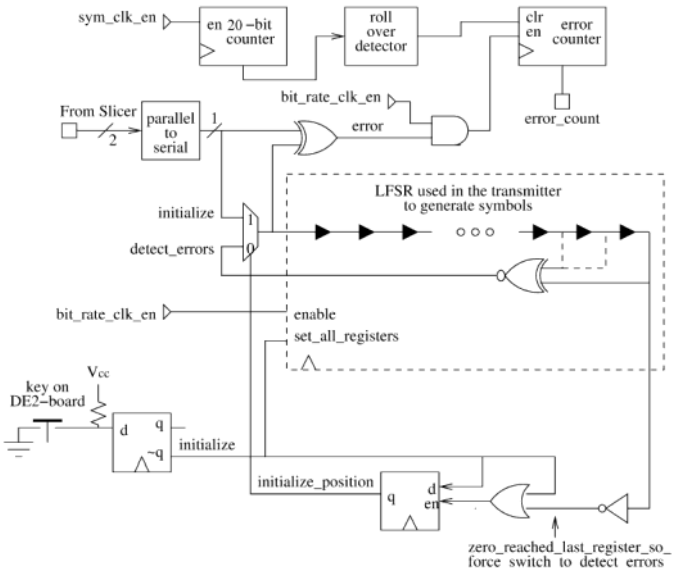
→ Once the Rx LFSR registers have been fully loaded, it is in the same state as the Tx LFSR was when it generated those bits.

→ Enable Rx LFSR. All future bits will match the Tx LFSR.

Critical note: The diagrams in the student guide and this notebook can't anticipate all possible student designs (especially wrt LFSR, mapper, and slicer). Some minor changes may be needed to make the BER circuit work with your design.

Don't follow the examples blindly. Common sense + good judgment are necessary!

Proposed Circuit from Student Guide



Common Problems in BER Measurement:

1) Clock rates → "bit rate clk en" in diagram

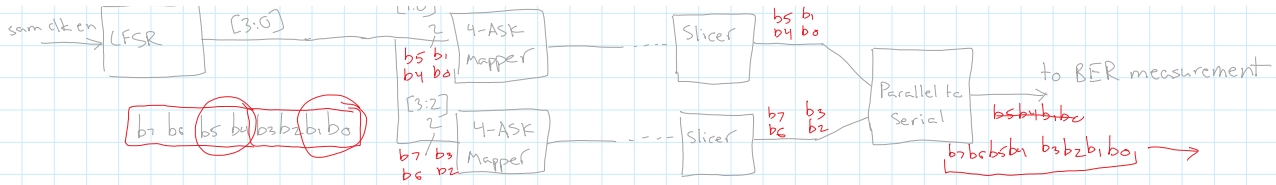
*need to cycle LFSR once for each received bit

→ could be 2x symbol rate or 4x depending on whether I+Q channels are built

2) Parallel to serial conversion: make sure ordering of bits matches mapper in transmitter

3) Make sure all output bits from Tx LFSR are loaded into Rx LFSR during synchronization phase

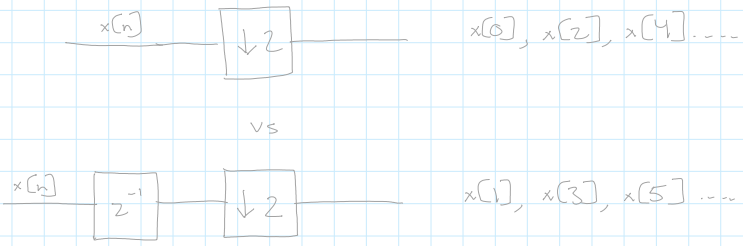
- If Tx LFSR cycles 4 times but only 2 bits are sent through mapper, Rx LFSR won't synchronize



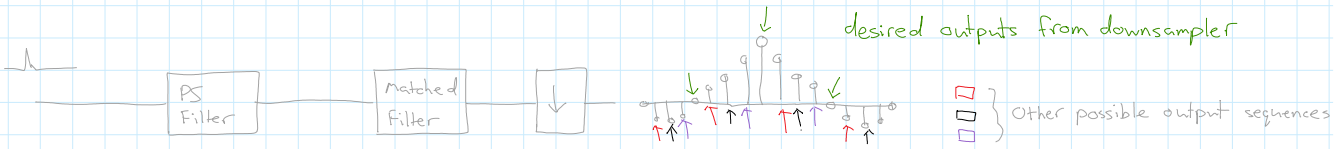
Downsampling - Timing Synchronization:

Recall that a downsampler is a time-variant system. By delaying its input, we can change the output sequence.

↳ which samples are kept, which are thrown away



Recall: we have worked hard to optimize the impulse response of the system wrt MER + ISI

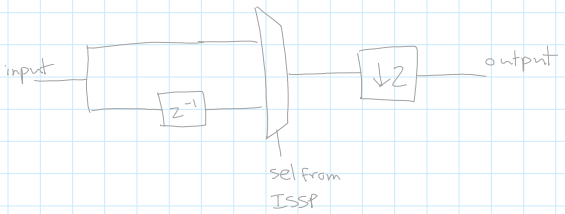


* receivers normally include timing recovery circuits to control the timing of the downsampling

→ done in D5

→ for D4, control using ISSP with variable delays

ex.



(include a circuit like this each time a downsampler is used - as in D3)

* manually adjust delays to achieve the best possible MER