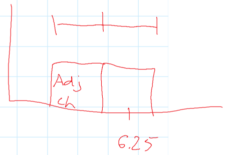
Deliverable 4

Key Circuits in D4

- upsampler (6.25 MHz → 25 MHz)
- downsampler (25 MHz → 6.25 MHz)
- upconverter (baseband → F_c = 6.25 MHz)
- downconverter (F_c = 6.25 MHz → baseband)
- channel model (gain, AWGN, adj ch?)
- BER measurement



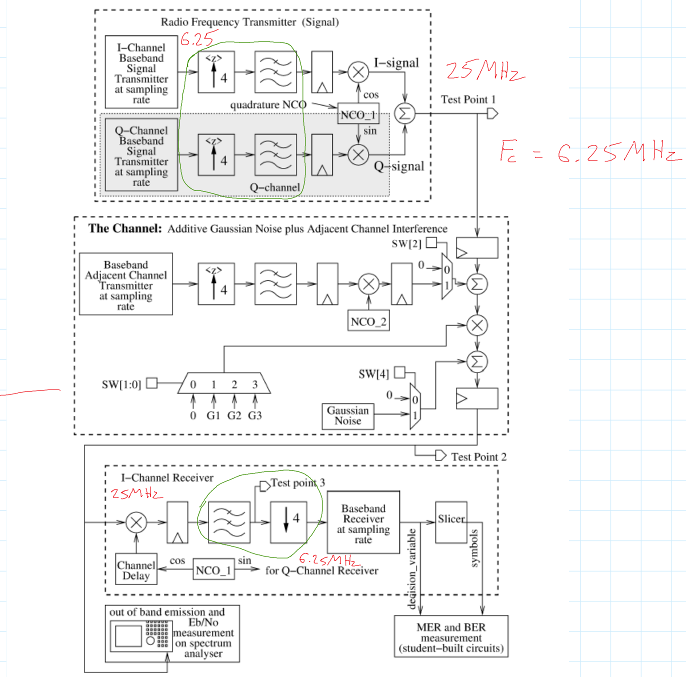


Figure 2.4: Block diagram showing the up/down sampling and up/down conversion.

Key Design Requirements

1) F_c = 6.25MHz
2) MER ≥ 39dB (practical PSF, gold standard MF)
3) meet all OOB reqs from D3 at test point 1 or 2
4) Total mults ≤ 14
   - Upsamplers (I, Q)
   - Downsamplers (I, Q)
   - Upconverter
   - Downconverter

   } total ≤ 14

   (D3 circuits, channel model excluded)
5) G_1 → E_b/N_o = 7.88dB
   G_2 → E_b/N_o = 10.52dB
   G_3 → E_b/N_o = 12.20dB
6) BER Values:
   G_1 → BER ≈ 10^{-2}
   G_2 → BER ≈ 10^{-3}
   G_3 → BER ≈ 10^{-4}

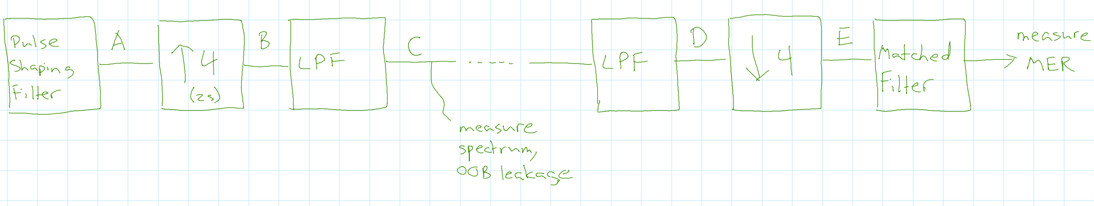
   } when AWGN is enabled
7) When AWGN is disabled, BER ≈ 0

Upsampling + Downsampling

requirements: MER ≥ 39dB (1 dB relaxation wrt D3)
: meet OOB requirements from D3
: minimize cost (≤ 14 mults total)

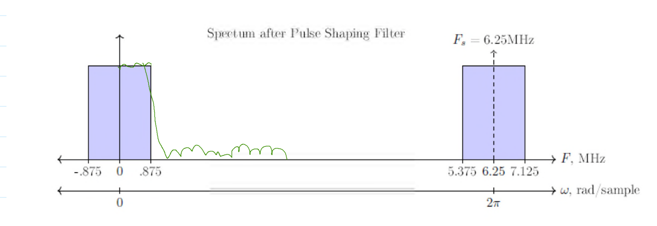
Key question: How does the upsampling + downsampling impact the MER + OOB leakage?

- Consider a simplified system (omit channel model + up/downconversion):

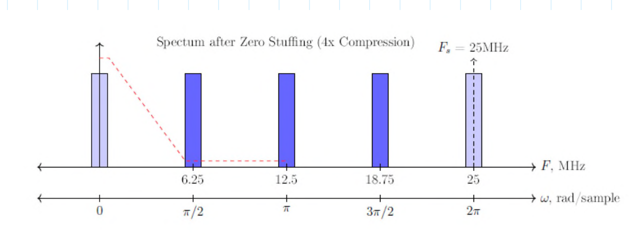


* What does the spectrum look like at points A, B, C, D, E?

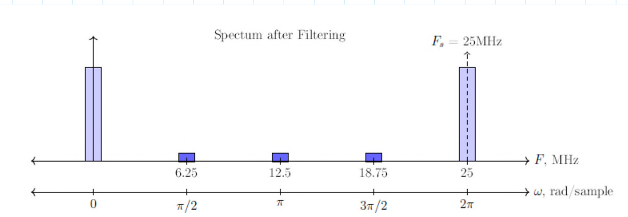
Spectrum at A:



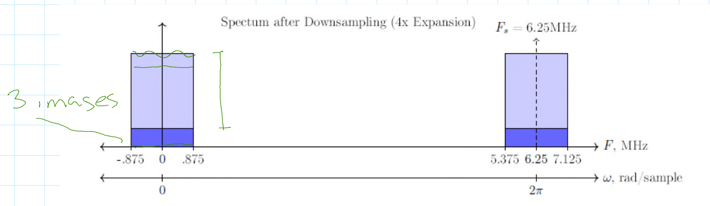
Spectrum at B:



Spectrum at C:, D:



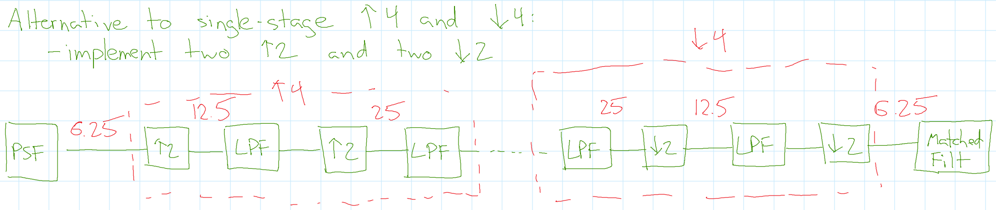
Spectrum at E:



Upsample / Downsample Filter Design: things to consider

- Coeff selection:
  - Fpass or wpass: $\geq$ channel upper edge
  - Fstop or wstop $\leq$ 1st image lower edge
  - Passband ripple, Stopband attn: relate to MER req
- Implementation
  - Zero mult possible?
  - Symmetry
  - Polyphase implementation

Alternative to single-stage ↑4 and ↓4:
- implement two ↑2 and two ↓2



- key advantage: filters can be half-band filters (every 2nd coeff is 0)
- looks more complicated than $\uparrow 4$ and $\downarrow 4$, but <u>may</u> be more economical

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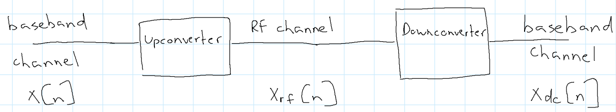
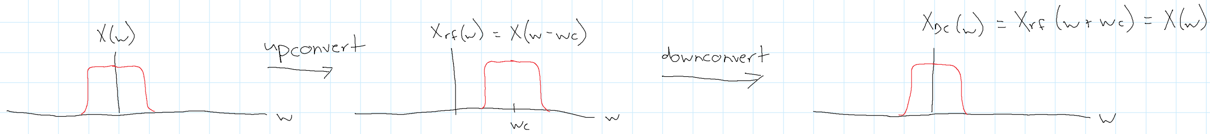
Upconversion + Downconversion

Purpose: shift baseband channel to some chosen center frequency (and vice-versa)



Ideally,



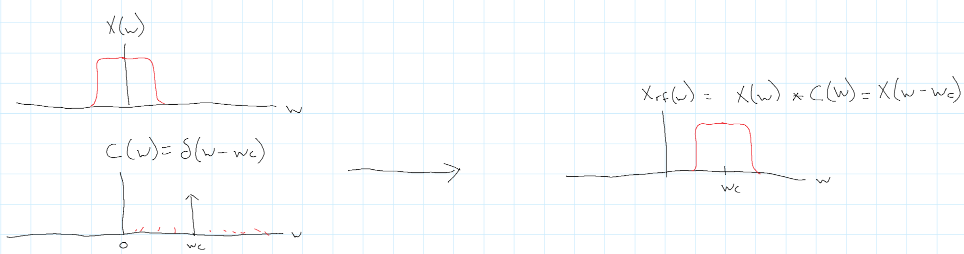
Basic Fourier Transform Theory:

$$X(w) \longleftrightarrow x[n]$$

Modulation property $X(w-w_c) \longleftrightarrow x[n]\,e^{jw_c n}$

shift spectrum right by w_c $\longleftrightarrow$ multiply by complex sinusoid w/ frequency w_c

- define $c[n] = e^{jw_c n}$ $\longrightarrow$ $x[n]\,e^{jw_c n} = x[n]\,c[n]$ ... mult in time domain $\longrightarrow$ convolve in freq domain

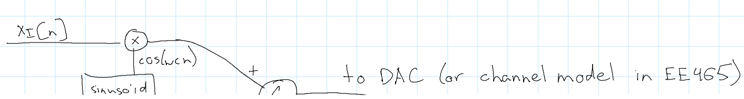


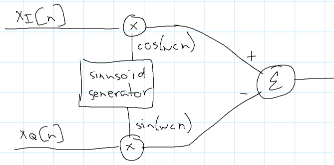
QAM system: $x[n]$ is complex $\longrightarrow$ $x[n] = x_I[n] + j x_Q[n]$ (independent transmitter paths)

$\longrightarrow$ Upconversion: $x_{rf}[n] = x[n]\,e^{jw_c n}$ $\leadsto$ Euler's identity $e^{jw_c n} = \cos(w_c n) + j\sin(w_c n)$

$$x_{rf}[n] = \left(x_I[n] + j\,x_Q[n]\right)\left(\cos(w_c n) + j\sin(w_c n)\right)$$
$$= \underbrace{x_I[n]\cos(w_c n) - x_Q[n]\sin(w_c n)}_{\text{real}} + \underbrace{j x_Q[n]\cos(w_c n) + j\,x_I[n]\sin(w_c n)}_{\text{imag}}$$

* only real part of $x_{rf}[n]$ can be sent to DAC + sent on the cable ...



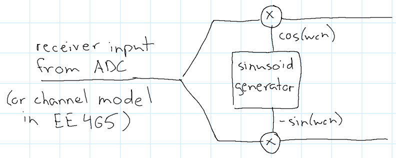


to DAC (or channel model in EE465)

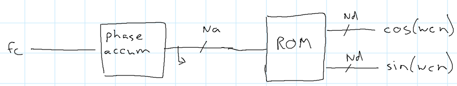
$x_I \cos(w_c n) - x_Q \sin(w_c n)$

Downconversion: input from cable / ADC is real, say $x_c[n]$

$$x_{dc}[n] = x_c[n]\, e^{-jw_c n} = x_c[n]\left[\cos(w_c n) - j\sin(w_c n)\right] = x_c[n]\cos(w_c n) - j\, x_c[n]\sin(w_c n)$$



For arbitrary up/downconversion, need variable sinusoid generators (NCOs)



- choices for N_a, N_d control sinusoid SNR + spurious emissions

In EE465 we simplify the design by using a fixed carrier frequency...

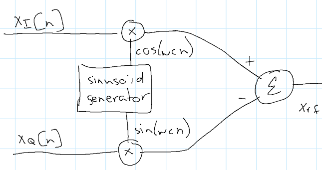
$$F_c = 6.25\,\text{MHz} \longrightarrow w_c = \frac{6.25\,\text{MHz}}{25\,\text{MHz}} \times 2\pi = \pi/2 \text{ rad/sample}$$

$\therefore$ the sequences to multiply by are: $\cos(\pi/2\, n) = [1\ 0\ -1\ 0\ 1\ 0\ \cdots]$

$\sin(\pi/2\, n) = [0\ 1\ 0\ -1\ 0\ 1\ \cdots]$

* no actual multiplications are needed!

ex. Upconversion:



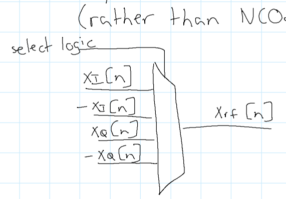
to DAC (or channel model in EE465)

$x_{rf} = x_I \cos(w_c n) - x_Q \sin(w_c n)$

n	0	1	2	3	4	5 ...
$\cos(\pi/2\, n)$	1	0	-1	0	1	0
$\sin(\pi/2\, n)$	0	1	0	-1	0	1
$x_I \cos(\pi/2\, n)$	$x_I[0]$	0	$-x_I[2]$	0	$x_I[4]$	0
$x_Q \sin(\pi/2\, n)$	0	$x_Q[1]$	0	$-x_Q[3]$	0	$x_Q[5]$
x_{rf}	$x_I[0]$	$-x_Q[1]$	$-x_I[2]$	$x_Q[3]$	$x_I[4]$	$-x_Q[5]$

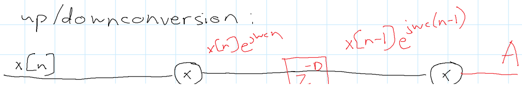
* each sample out of the upconverter is either x_I, $-x_I$, x_Q, or $-x_Q$

→ idea: implement with multiplexing logic (rather than NCOs + mixers)



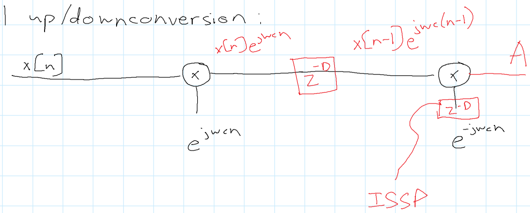
- similar idea can be applied to downconversion

Overall up/downconversion:



recall from EE 456: coherent receiver (requires phases of oscillators in Tx and Rx to be identical)

Overall up/downconversion:

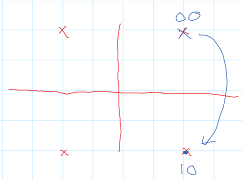


$x[n-1]\, e^{j\omega_c(n-1)}\, e^{-j\omega_c n}$

at A: $x[n-1]\; e^{-j\omega_c}$ $\pi/2$

$x[n-1]\; \underbrace{e^{-j\pi/2}}$

⟶ rotate by $-\pi/2$ radians



recall from EE 4SG: coherent receiver
(requires phases of oscillators in Tx and Rx to be identical)

- each sample gets multiplied by the conjugate of what it was multiplied by in the transmitter:

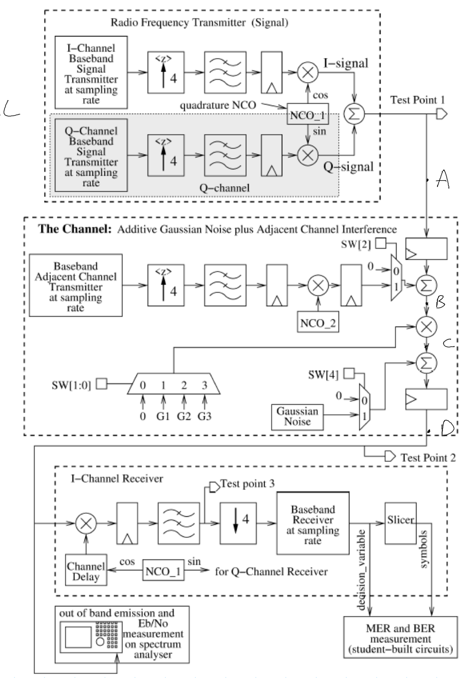
$$x[n]\, e^{j\omega_c n}\, e^{-j\omega_c n} = x[n]$$

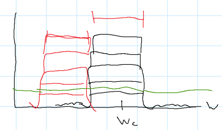
- what if they don't match?
(due to different startup times or delay through channel)

ex. channel delay $D = 1$

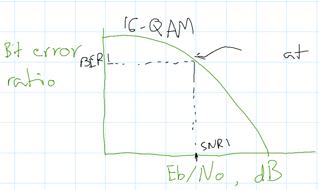
Channel Model

- models effects of transmission medium on our signals
  1) addition of adjacent channel ⟶ OPTIONAL
  2) applying a gain to the signal
  3) adding AWGN to the signal





Waterfall curves

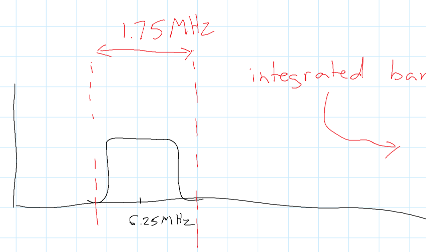


at SNR1, an optimal receiver will have a BER of BER1

Eb/No
- 7.88 dB ⟶ 10^{-2}
- 10.52 dB ⟶ 10^{-3}
- 12.20 dB ⟶ 10^{-4}

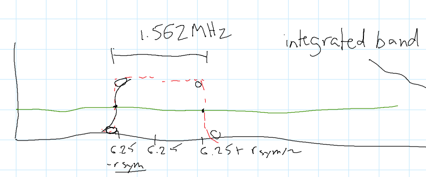
Measuring SNR of System

1) Enable signal, disable noise view tp2 on SA



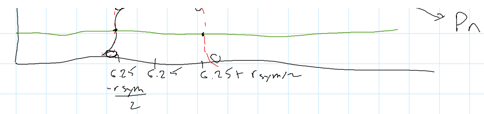
integrated band power ⟶ P_s

2) Enable noise, disable signal view tp2 on SA



integrated band power ⟶ P_n

Es/No $\xrightarrow{\text{compensate}}$ Eb/No



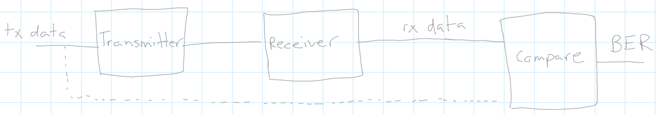
$E_s/N_o \xrightarrow{\text{compensate}} E_b/N_o$

3) $SNR = \dfrac{P_s}{P_n}$ $\qquad P_{s\,dBm} - P_{N\,dBm} = SNR_{dB}$

4) Adjust gains

BER Measurement

- general concept :

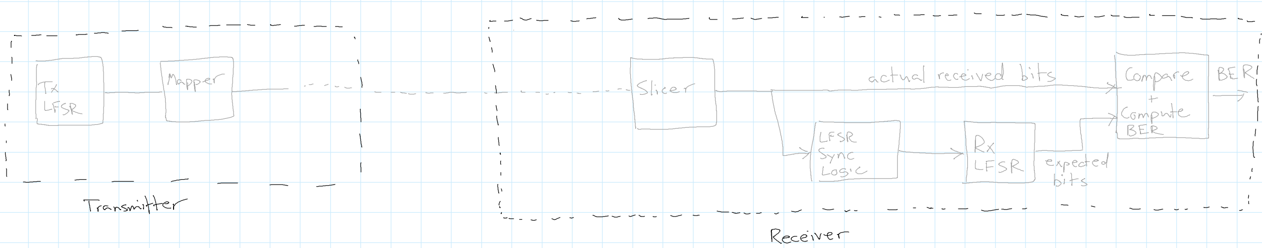


$BER = \dfrac{\#\text{ bits in error}}{\#\text{ bits sent}}$

Challenge : How can the receiver know what the original tx data bits were?
→ Not practical to run a wire in parallel w/ entire communication system as above.

Approach used in D4:
- build a copy of the Tx LFSR in the receiver
- synchronize the two LFSRs (this is the tricky part!)
- compare bits from slicer to those from receiver LFSR

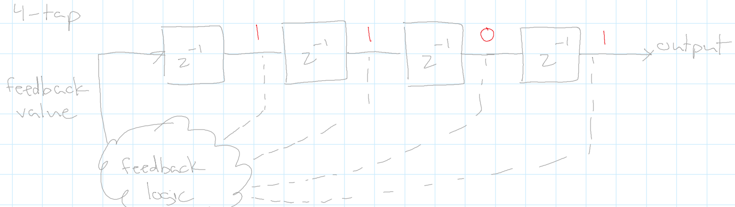
High-level overview:



Key Principles for Synchronizing LFSRs:

- Two LFSRs with the same structure (length + feedback taps) generate the same output sequence
- If the two LFSRs have the same internal state at time n, they will produce the same outputs forever
- The N values in the N registers of an N-tap LFSR reflect the next N output bits from the LFSR

ex. 4-tap



Clock	Output
N	1
N+1	0
N+2	1
N+3	1

* What were the values in the 4 registers at time N?

→ Note that knowing these 4 bits lets us predict the LFSR's output at time at time N:

→ Note that knowing these 4 bits lets us predict the LFSR's output at time N+4, N+5, N+6 ... ∞

When building our BER measurement circuit, we assume that the first few bits out of the slicer are correct.

→ Can use these bits to load the registers of the Rx LFSR.

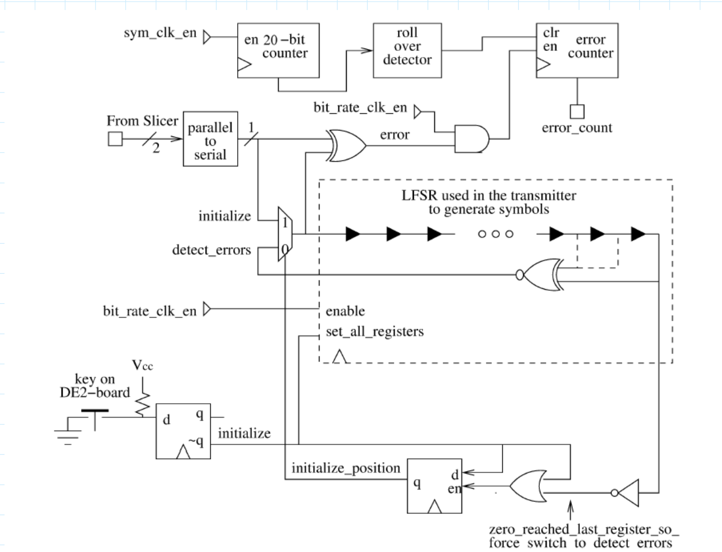
→ Once the Rx LFSR registers have been fully loaded, it is in the same state as the Tx LFSR was when it generated those bits.

→ Enable Rx LFSR. All future bits will match the Tx LFSR.

Critical note: The diagrams in the student guide and this notebook can't anticipate all possible student designs (especially wrt LFSR, mapper, and slicer). Some minor changes may be needed to make the BER circuit work with your design.

Don't follow the examples blindly. Common sense + good judgment are necessary!

Proposed Circuit from Student Guide



Common Problems in BER Measurement:

1) Clock rates → "bit rate clk en" in diagram

*need to cycle LFSR once for each received bit

→ could be 2x symbol rate or 4x depending on whether I+Q channels are built

2) Parallel to serial conversion: make sure ordering of bits matches mapper in transmitter

3) Make sure all output bits from Tx LFSR are loaded into Rx LFSR during synchronization phase

- If Tx LFSR cycles 4 times but only 2 bits are sent through mapper, Rx LFSR won't synchronize

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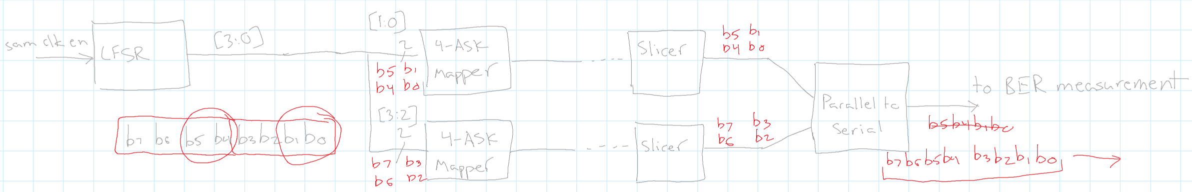
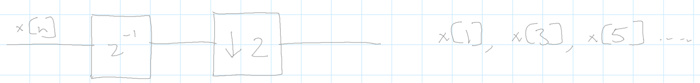


Downsampling - Timing Synchronization:

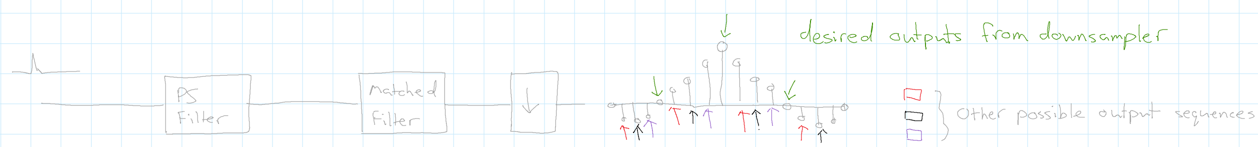
Recall that a downsampler is a time-variant system. By delaying its input, we can change the output sequence.

which samples are kept, which are thrown away

vs



Recall: we have worked hard to optimize the impulse response of the system wrt MER + ISI

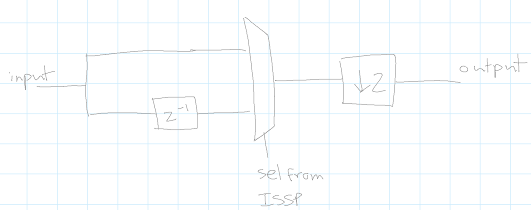


* receivers normally include timing recovery circuits to control the timing of the downsampling

→ done in D5

→ for D4, control using ISSP with variable delays

ex.



(include a circuit like this each time a downsampler is used - as in D3)

* manually adjust delays to achieve the best possible MER