Testcase	Description of Feature	Description of Stimulus	Verification Criteria
Synchronous Reset	ALU has a synchronous reset	Assert “reset”	alu_y_out & alu_co_out should be cleared or 0
Basic operation	ALU has various arthimetic functions that can be completed in one clock cycle	Assert opcodes 0, 1, 4, 5, 6, & 7 with random stimulus	Depending on the operation (ex: addition opcode=1), the output of the opcode should be A + B, where the carry_out flag may be asserted based on stimulus
Multiplication	ALU requires two clock cycles to complete, where a 16-bit output will be generated in two consecutive clock cycles	Assert opcodes 2, with random inputs A & B	Should expect two 8-bit outputs to be asserted consecutively by the DUT where the first byte is the upper 8 MSB and the second byte is the lower 8 MSB. The carry_out flag may be asserted depending on the stimulus
Division	ALU requires three clock cycles to complete, where an 8-bit output will be generated after three clock cycles	Assert opcodes 3 with random inputs A & B	After three clock cycles, should expect the output to be A/B.

Notes:

- Multi-cycle operation will ignore intermediate operations until the multi-cycle op has finished