Bahdan Udaltsou

Senior Application Engineer
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Type of communication:
Email, Messengers

LANGUAGES

English (Upper-Intermediate)

Polish (Intermediate)

Russian (Native)

SKILLS

Programming

SystemVerilog

UVM

Functional Verification

Computer Architecture

Synthesis

C

C++

Python

SvUnit

Natural Docs

Sphinx

PCIe

MIPI Soundwire

APB

AXI

ABOUT ME

Have knowledge of various IPs(traffic convertors, audio, memory subsystems) verification. Had created qualitative verification plans, according to the spec. requirements, which provided high standards of the functional verification. Can write testbenches and all verification infrastructure from scratch in SystemVerilog, using UVM methodology. Familiar with basic protocols, such as AMBA APB4, AXI, UART, SPI, I2C, MIPI SoundWire. Also possess knowledge of PCIe Gen5. Have experience in synthesis with conformal analysis of the chip with writing SDC constraints for the design. Have worked with simulators from big three (Cadence, Synopsys, Mentor) and with its VIPs. CI/CD was performed in Jenkins, or using Cadence software, as vManager, with vsif scripts. Team-player, responsible and attentive to details. Work on a high result. Had mentorship experience for the newcomers, and willing to share my experience with the team, for improving overall quality of work. Constantly improving my level of competency, by reading technical literature(computer architecture) and articles(DVcon). According to the last one, like to try new technics and observe their advantages/disadvantages. Ready for the interesting projects and new challenges.

EDUCATION

Masters in Radio Engineering

2016 - 2020

Moscow Power Engineering Institute(Technical University)

B.E in Radio Engineering

2012 - 2016

Moscow State Institute of Radio Engineering, Electronics and Automation (Technical University)

EXPERIENCES

Senior Application Engineer

July 2024 - Present

Cadence Design Systems

Creating a new methodologies for customers and inner use, according to the provided task. Providing Design and verification services. Mentor support for the new employees.

Application Engineer

Nov 2022 - June 2024

Cadence Design Systems

Providing Design and verification services for inner and customer's use. In the majority, utilization of the Cadence tools, but it depend's on the customer.

Module Verification Design Engineer

Jul 2021 - Aug 2022

Tecon MT

Module verification of the inner IPs, using Synopsys VCS and AXI VIP.

Senior RF Design Engineer

Nov 2014 - Jul 2021

Engineering center Era

Developing various equipments from idea to experimental model. Providing microwave simulation and modelling with various tools, PCB and mechanical design, adjusting for further putting on stream.

PROJECTS

PCIe IP integaration and Verification

Cadence Design Systems

Creation of the PCIe Gen5 subsystem, according to the customer needs, by integration inner IPs and providing additional design stuff, with further verification and synthesis tasks. Responsible for the design of the inner modules for the interrupts and for the verification environment with RAL. RAL is performed by the reg_verifier with advanced prediction for set of registers.

Verification packages and open-source libs integration

Cadence Design Systems

Creation of the verification libraries for the future reusability in the projects. Observing and adoption of the open-source tools for further use with Cadence tools. Creating new methodology for the acceleration of the simulation;

AXI4L2APB4 bridge

Cadence Design Systems

Design and verification of the inner module for further use in the various projects. Full design and verification cycle. Code linting for RTL was done with Jasper tools, regress and coverage annotation into the verification plan was done in the vManager, with vsif files support. For the verification purposes various VIPs from VIPCAT were used.

Design and Verification reuse library

Cadence Design Systems

Hub creation with design reuse modules and verification components for different purposes. Static website with sphinx engine was written with search included(stork-search) and deployed on the Github pages.

Memory integration testing

Cadence Design Systems

Creating verification environment from scratch using uvm-methodology for performing synthesised memory modules of different types connectivity check and its verification. All environment was written, according to the way, which was described in the article on the DVCON by Dave Rich form Siemens with abstract interface usage, for avoiding parametrization, and full incapsulation of the interface signals.

Chip's synthesis

Cadence Design Systems

Performing synthesis of the chip, with advance nodes usage in the Genus software with LEC. Writing SDC constraints for the synthesis. Preparing scripts for customer for different purposes, such as simulation, synthesis, formal checks, etc.

Soundwire IP integration and verification

Cadence Design Systems

Integration of the IP into existing chip from the customer's side and providing verification according to the verification plan and existing verification environment. All legacy environment was written in an old-fashioned way, so it was rewritten in the UVM. Original testcases were debugged. For the verification VIP from Cadence was used, and verification was impelemented with legacy code support. For verification plan was used Vmanager, as for the regression with vsif scripts, simulator was xcelium.

Module Verification

Tecon MT

Verification of the company's IP with its custom protocol. IP is an converter from one kind of traffic into AXI4 traffic with multiple modes. Full verification environment was written from scratch, using UVM methodology, according to the verification plan and responses from the meetups with the design team. For AXI4 load was used VIP from Synopsys. At the end it was put on the regress, using Jenkins, for collecting coverge and it's further observation. For verification plan creation and coverage annotation Verdi software was used, simulator was Synopsys VCS.

IC_SPEC finder

Pet-project

Program with GUI for downloading pdfs for the ICs, which are defined in the textfile. Full code is written in python, with additional imported packages, such as phantom, for browsing in hide mode, and selenium, for parsing webpage and trigger events.

Stand for measurements automation

Pet-project

Automotive measurable stand, which consists of multiple software-measurable tools such as generators, specter analyzers, scalar and vector analyzers, etc. plus the system for configuring the measurable device, and the program for analyzing and parsing final data. The main task of this project is to give to any user an opportunity to choose measurable device and scripts for basic measurements. After the completion of the measurements, automatically fill the xsl template with parsed data and print it.

RF-transcievers for various purposes

Engineering Center Era

Equipment creation according to the technical specification, with multiple steps. For PCB and Schematics Altium Designer was used. Various tools for microwave modelling: Microwave CST, Ansys HFSS, Keysight MWO. In the majority Intel Altera FPGAs were used, so Quartus was chosen as software for firmware creation. STM32 were used as top-priority MCs, for its firmwares Eclipse or Coocox IDE. At the end for adjustments and measurements different tools were used from multimeter to spectrum analyzers.

LICENSES & CERTIFICATIONS

SystemVerilog Assertions v5.1 Exam — Feb 2023

Cadence Design Systems

SystemVerilog Accelerated Verification with UVM — Nov 2022

Cadence Design Systems

SystemVerilog for Design and Verification v21.10 — Nov 2022

Cadence Design Systems

SystemVerilog Assertions v5.1 Exam — Feb 2020

Cadence Design Systems

Basics of radio-location and navigation — Mar 2020

Moscow Aviation Institute (National Research University MAI)

Anti-jamming equipment design — Feb 2018

NPF Rodnik

Circuit design and signal integrity — Feb 2018

NPF Rodnik

SKILLS & PROFICIENCY

SystemVerilog

UVM

Python

C++