DESIGN PROJECT

"IMPLEMENTATION OF A PID CONTROLLER"

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FACULTY OF ENGINEERING, UNIVERSITY OF JAFFNA

EC 5030 – CONTROL SYSTEMS

DESIGN PROJECT

"IMPLEMENTATION OF PID CONTROLLER"

Design 1 – Design of a second order system

1.

1. Voltage follower:

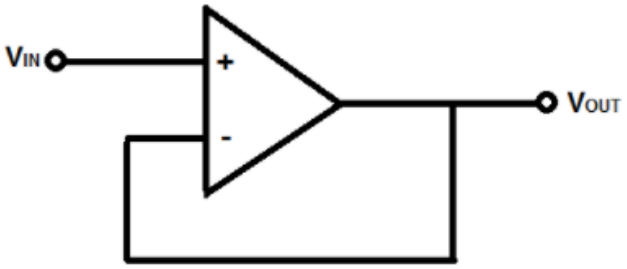


Figure 1: Circuit diagram of the voltage follower

The relationship between V_{in} and V_{out} as follows,

$$V_{in} = V_{out}$$

2. Integrator:

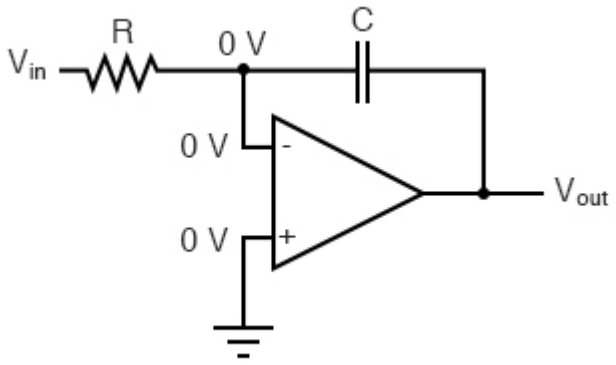


Figure 2: Circuit diagram for an integrator circuit

The relationship between V_{in} and V_{out} as follows,

$$\boldsymbol{V_{out} = \frac{-1}{RC} \int V_{in} dt}$$

3. Differentiator:

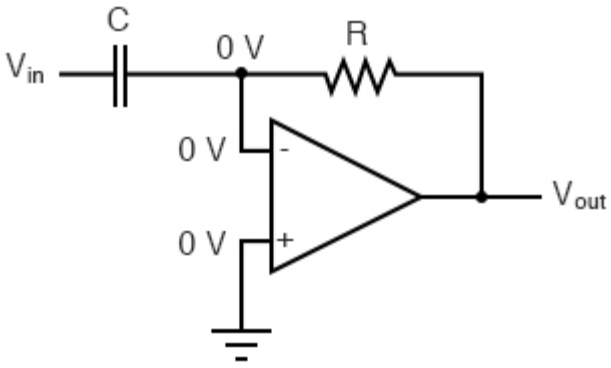


Figure 3: Circuit diagram for the differentiator circuit

The relationship between V_{in} and V_{out} as follows,

$$\boldsymbol{V_{out} = -RC \frac{dV_{in}}{dt}}$$

4. Summing amplifier:

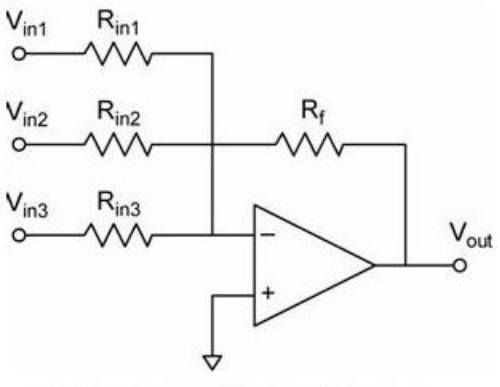


Figure 4:Circuit diagram of summing amplifier

The relationship between V_{in} and V_{out} as follows,

$$V_{out} = -R_f \left[\frac{V_{in1}}{R_{in1}} + \frac{V_{in2}}{R_{in2}} + \frac{V_{in3}}{R_{in3}} \right]$$

5. Inverter:

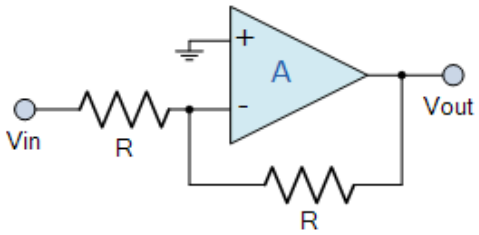


Figure 5: Circuit diagram of the inverter

The relationship between V_{in} and V_{out} as follows,

$$-V_{in} = V_{out}$$

2.

- The second order system is designed using Simulink and the circuit is simulated.
- The step input was given by usual step input in Simulink.
- Using the scope, the observations were taken.

3.

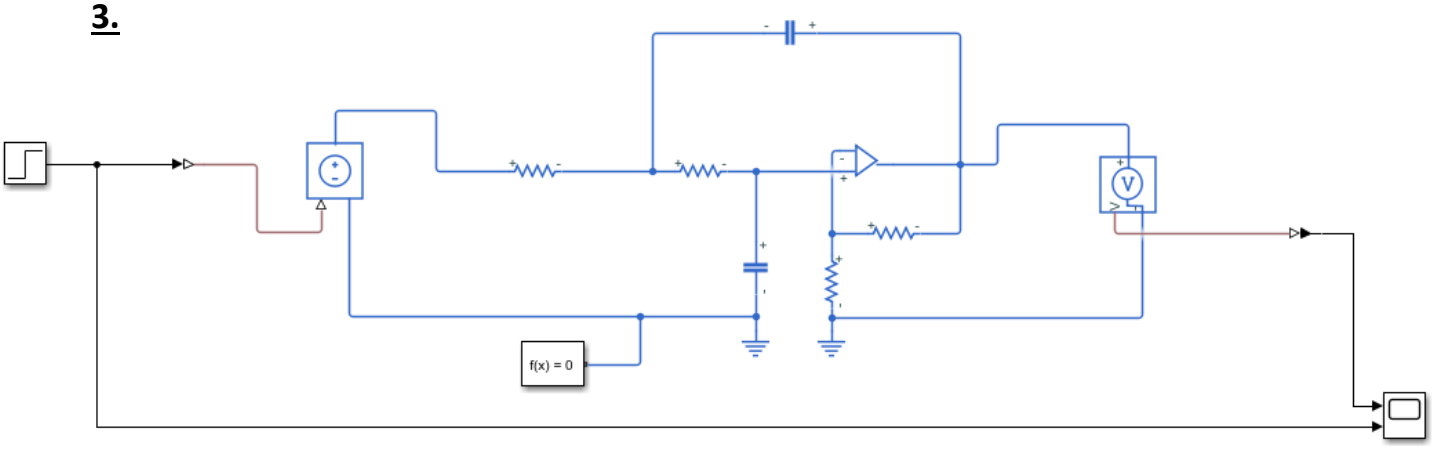


Figure 6: Second order system designed by Simulink

4.

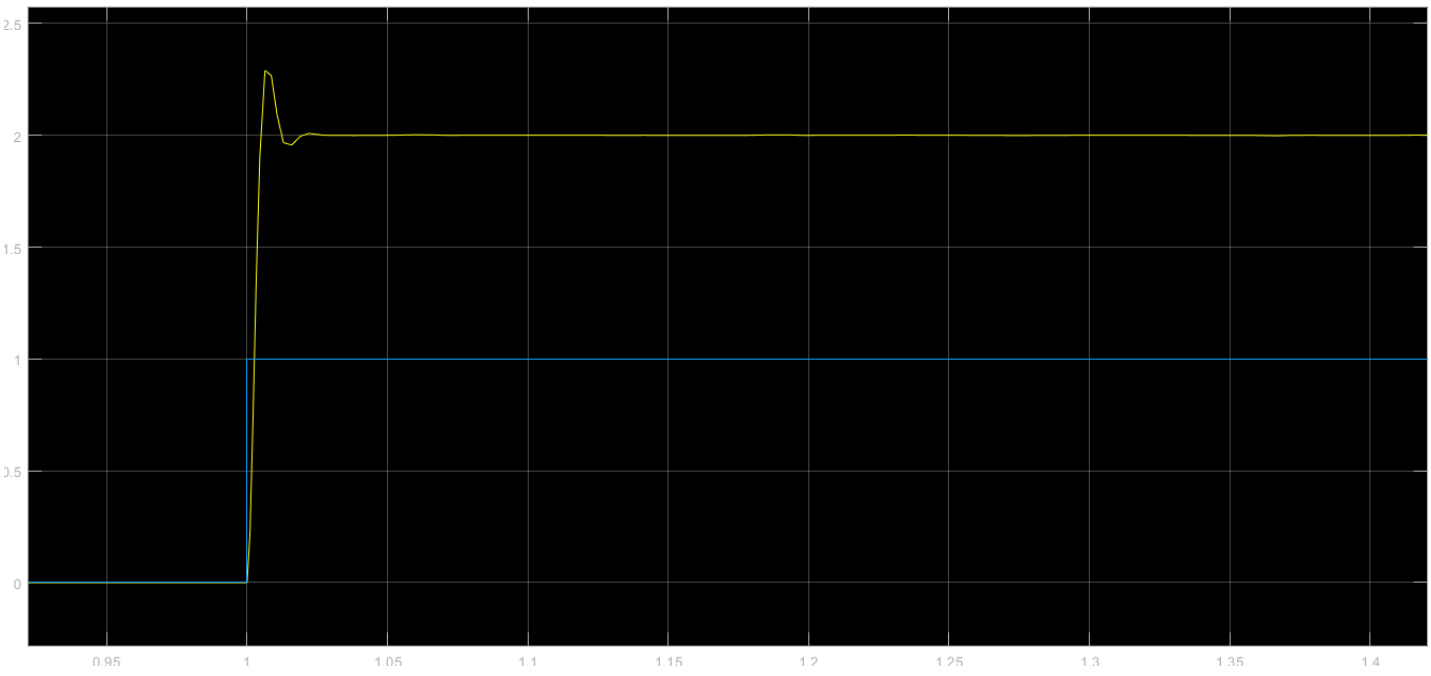


Figure 7: Step response of the Second order system

5.

Maximum peak overshoot	= 0.289 V
Maximum peak overshoot percentage	= 14.45%
Rise time	= 3.366 ms
Settling time	= 29.992 ms

DESIGN 2 – DESIGN OF A SECOND ORDER SYSTEM WITH PID CONTROLLER.

- The PID controller was designed using Simulink software. Each block represented subsystems which are actually Proportional controller, Integrator and differentiator.
- The Second order system is connected to the PID controller via a closed loop connection as shown in the circuit diagram.
- The Switching mechanism between P, PI, PD and PID is achieved by a rotary switch. (In Simulink it is replaced by a SPMT switch.)
- The change of Integral, Differential and Proportional constants is achieved via variable resistors inside each controller as shown in following figures.

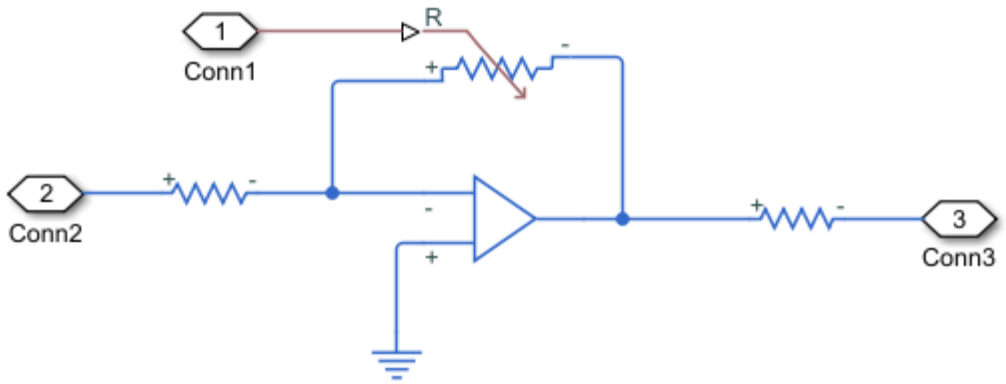


Figure 8: Inside circuit of the proportional controller subsystem block.

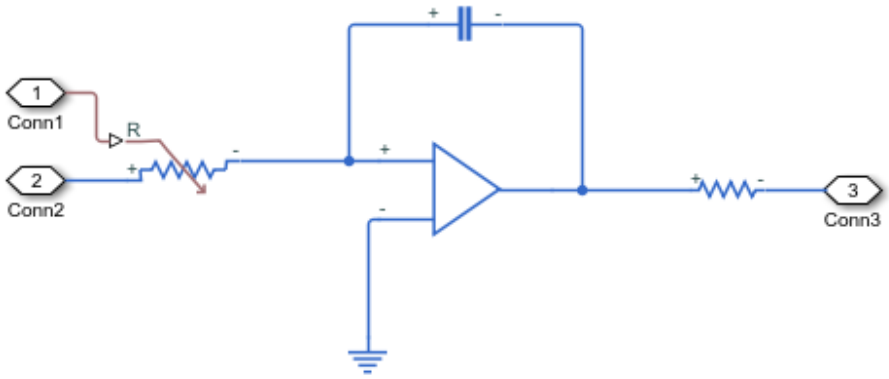


Figure 9: Inside circuit in the integrator subsystem block

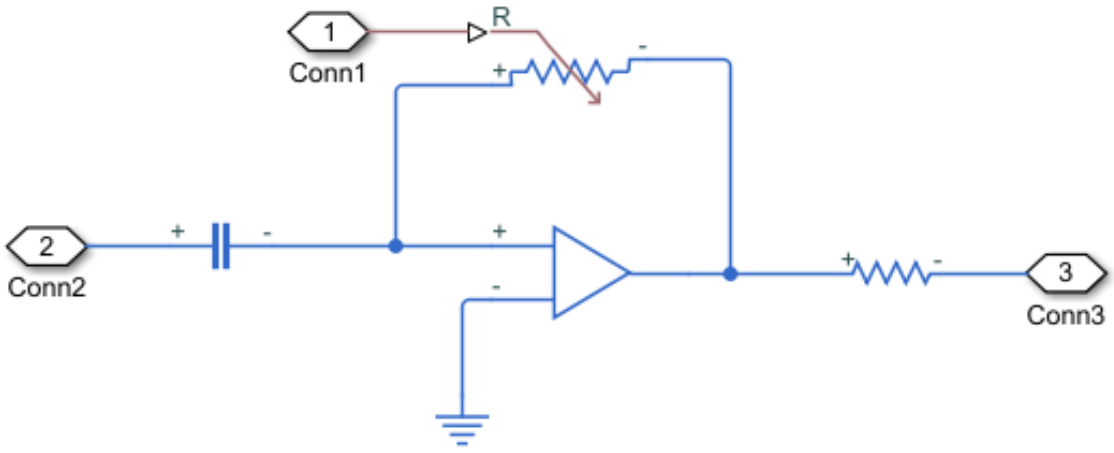


Figure 10: Inside circuit of the differentiator subsystem block

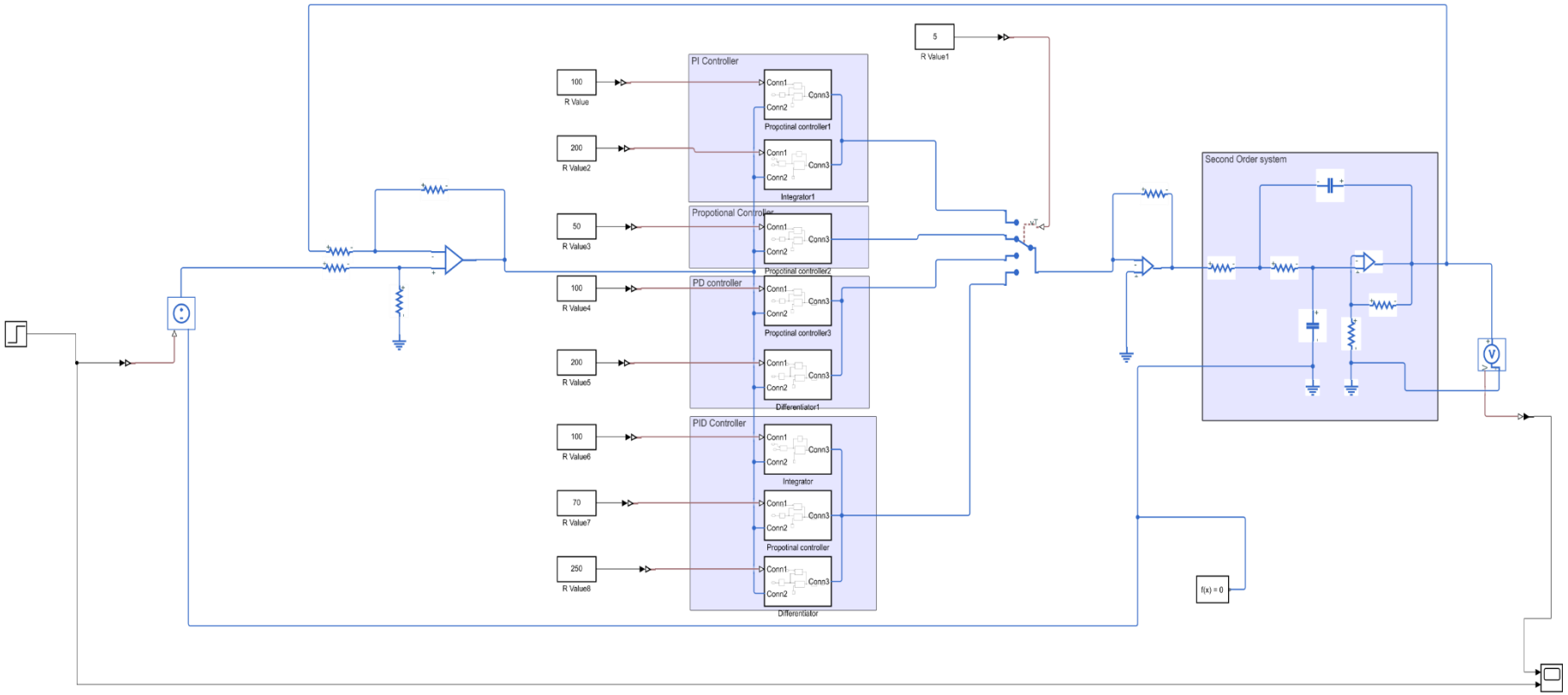
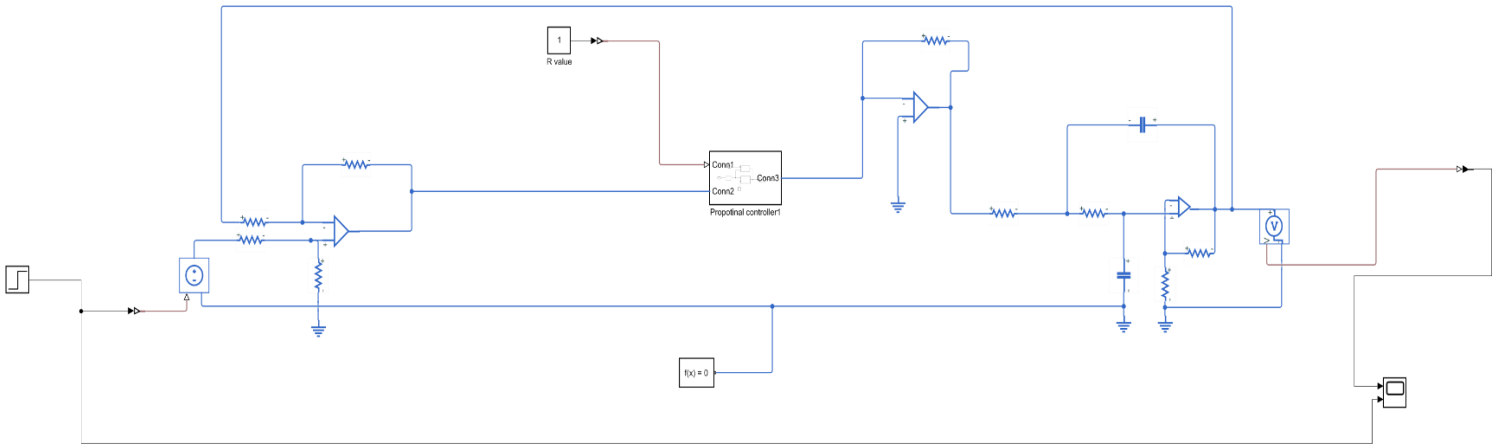


Figure 11: Designed PID controller connected to the system with closed loop connection

- All the resistor values of the summing circuit and subtractor circuits are 1Kohms resistors.

Task 1 – Design of a second order system with proportional controller

- The connection to the Proportional controller established using the SPMT switch.
- The Closed loop circuit diagram as follows. (only showing connected elements)



- Inside circuit of the proportional controller subsystem block the normal resistors' values were kept at 1 kOhms and the Kp value is changed by changing the value of the variable resistor inside.
- $K_p = \frac{R_{variable}}{R(1Khoms)}$
- The Kp values were changed and simulated the circuit and observations were tabulated.

Variable resistance(kOhms)	Kp Value	Max. peak overshoot(mV)	Max. peak overshoot (%)	Rise time(µs)	Settling time(ms)
25	25	786	80.2	304.15	26.36
50	50	845	85.35	213.7	27.34
100	100	889	89.35	148.93	33.44
200	200	921	92.37	104.38	34.01

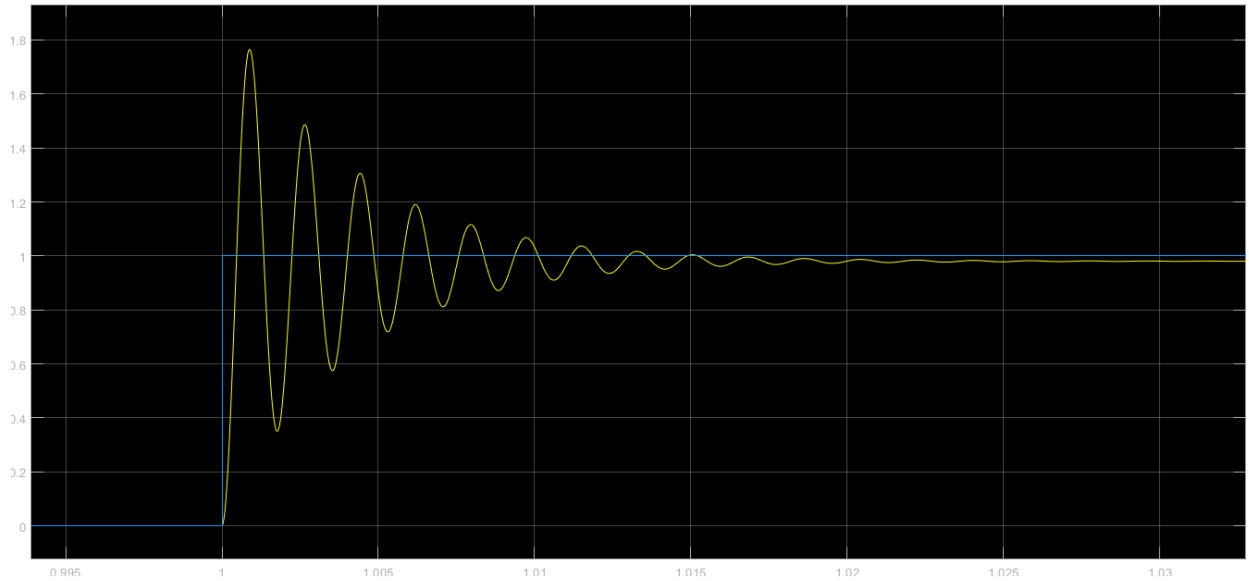


Figure 14: Step response of the second order system when Kp = 25

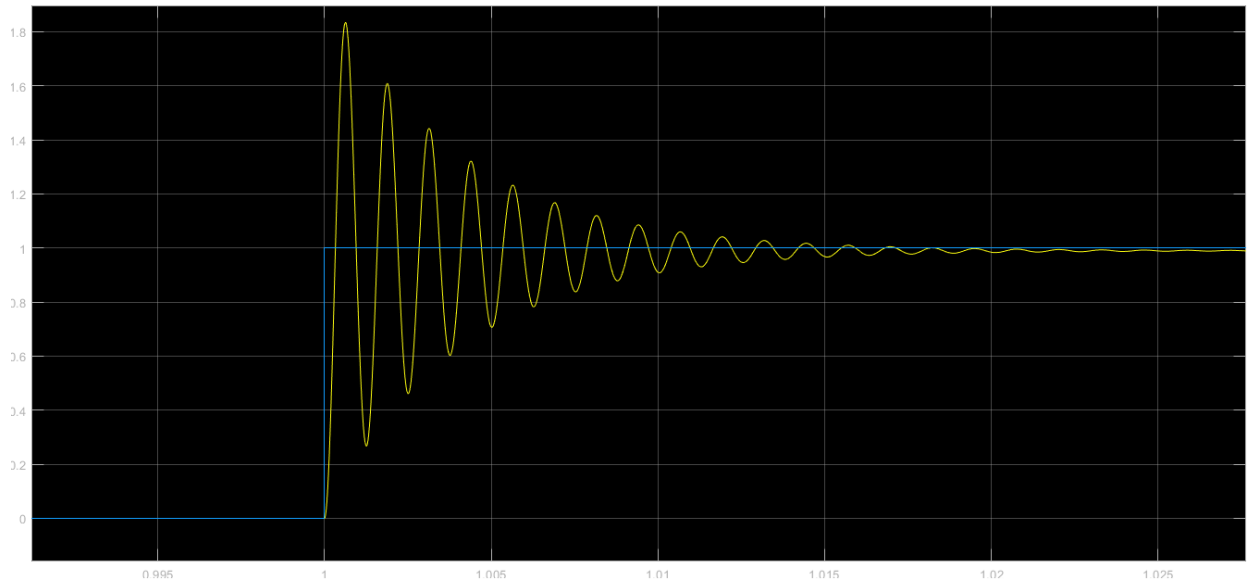


Figure 13: Step response of the system when Kp =50

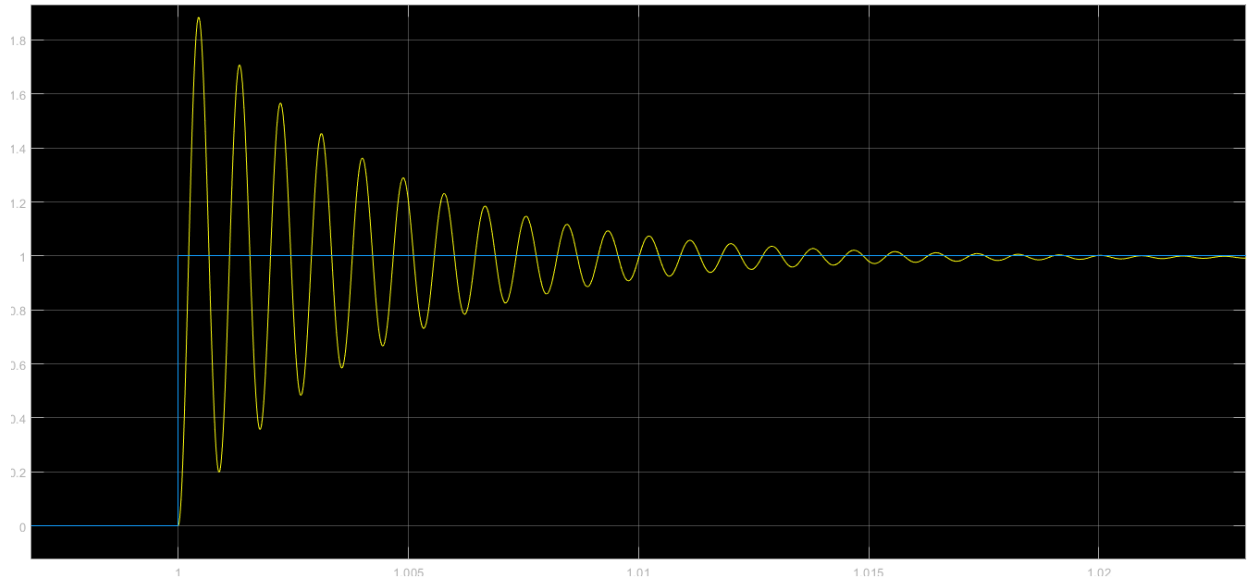


Figure 12: Step response of the system when Kp = 100

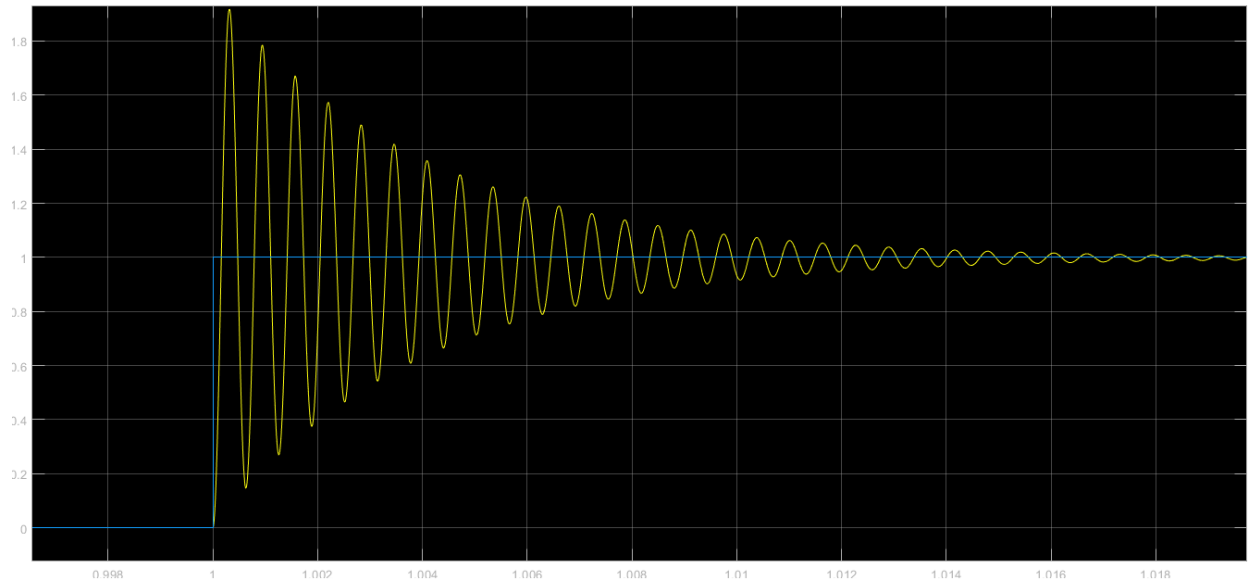


Figure 15: Step response of the system when Kp =200

Task 2 – Design of a second order system with PI controller

- The connection to the PI controller established using the SPMT switch.
- The Closed loop circuit diagram as follows. (only showing connected elements)

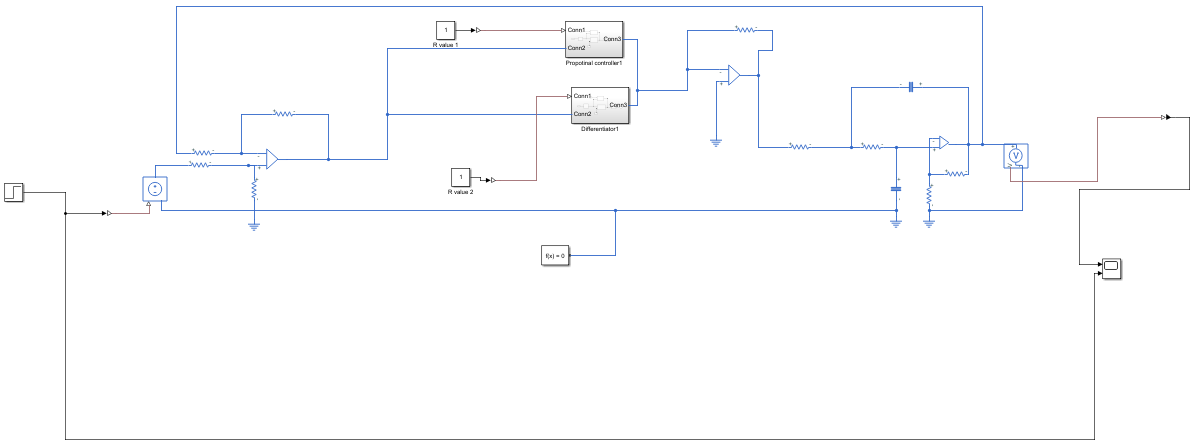


Figure 16: Circuit diagram of the PI controller connected to the system

- The internal capacitor of the Integrator block was kept at 1µF and Ki value was changed by changing the variable resistor inside the Integrator block.

- Throughout the simulation process, the proportional constant Kp was kept at 25 by keeping its variable resistor at 25kOhms.
- For different Ki values, the simulation was conducted and the observations were tabulated as follows,
- $K_I = \frac{1}{R_{variable} * C(1\mu F)}$

Variable resistance(kOhms)	Ki value	Max. Peak overshoot(mV)	Max. Peak overshoot (%)	Rise time(µs)	Settling time(ms)
20	50	767	76.8	307.98	35.01
10	100	768	76.8	307.46	38.35
5	200	769	76.9	308.3	40.2

- The step responses as follows for each Ki value.

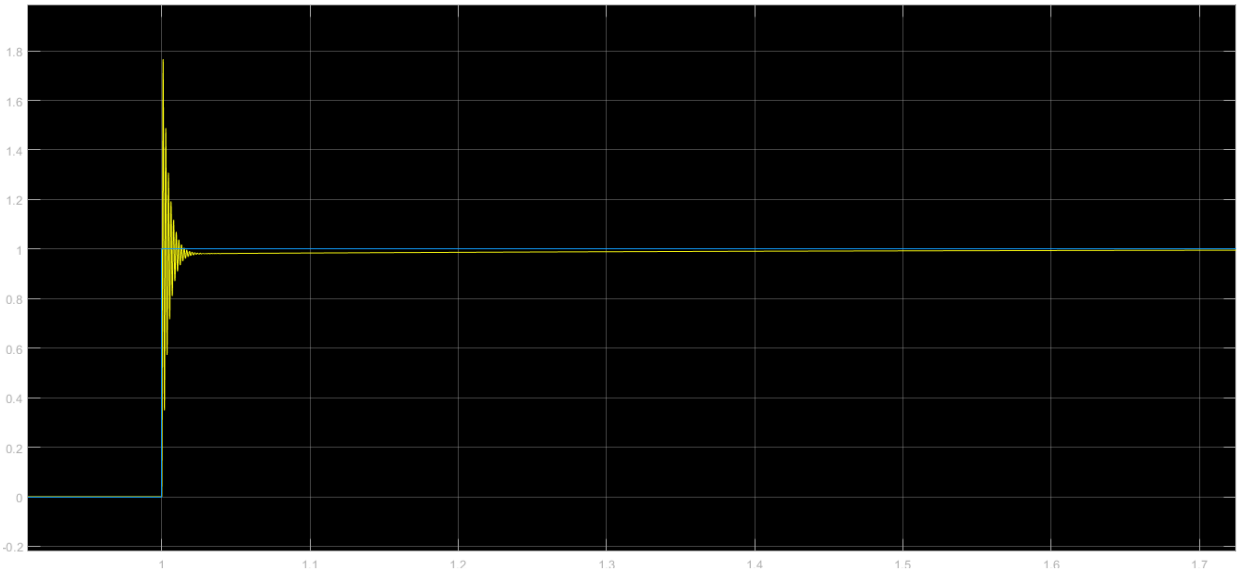


Figure 17: Step response of the system for Ki = 50 & Kp =25

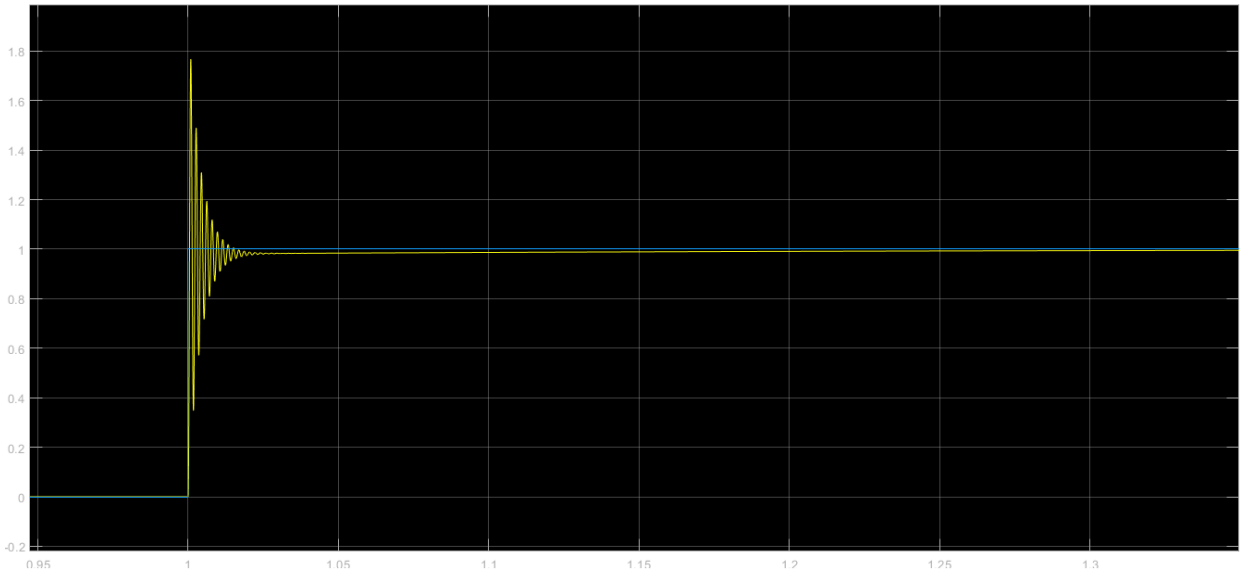


Figure 18: Step response of the system for Ki = 100 & Kp = 25

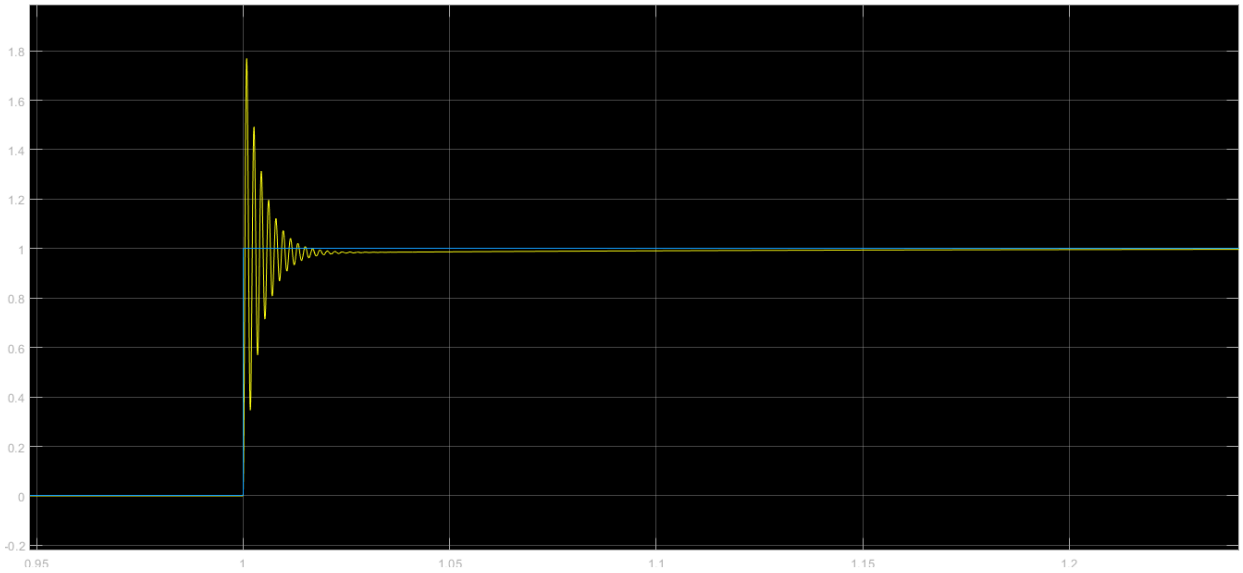


Figure 19: Step response of the system for Ki = 200 & Kp = 25

Task 3 – Design of a second order system with PD controller

- The connection to the PD controller established using the SPMT switch.
- The Closed loop circuit diagram as follows. (only showing connected elements)

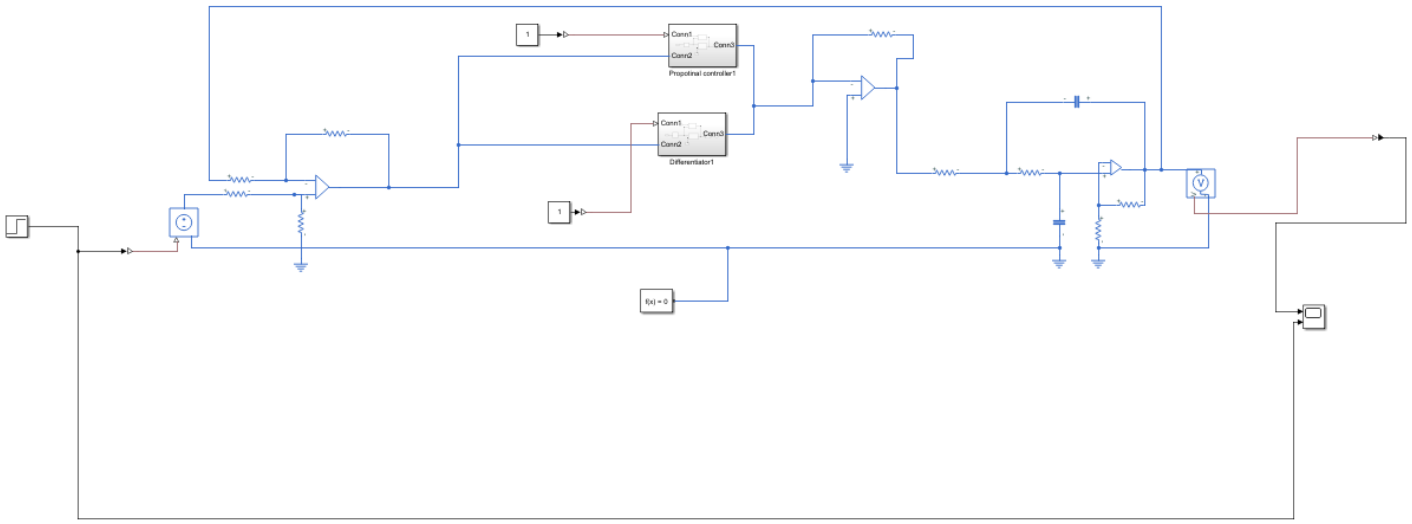


Figure 20: Circuit diagram of the PD controller connected to the system

- The capacitor value inside the differentiator was kept at constant 100µF throughout entire simulation process and the Kd value was changed by changing the resistance value of the variable resistor inside the Differentiator.
- The other resistor inside the differentiator was kept at 1 kOhms.
- The Kp value was kept at constant 200 value by keeping its variable resistance as 200kOhms.
- Then the Kd value is changed and simulated system for each Kp value and the results were tabulated.
- $K_d = R_{variable} * C(100\mu F)$

Variable resistance(kOhms)	Kd value	Max. peak overshoot(mv)	Max. peak overshoot (%)	Rise time(ns)	Settling time(s)
100	10	19	1.94	437.8	2.79
200	20	20	2.04	202.8	2.58
400	40	20	2.04	101.3	1.81

- The step response was taken for each Kd values from the scope as follows.

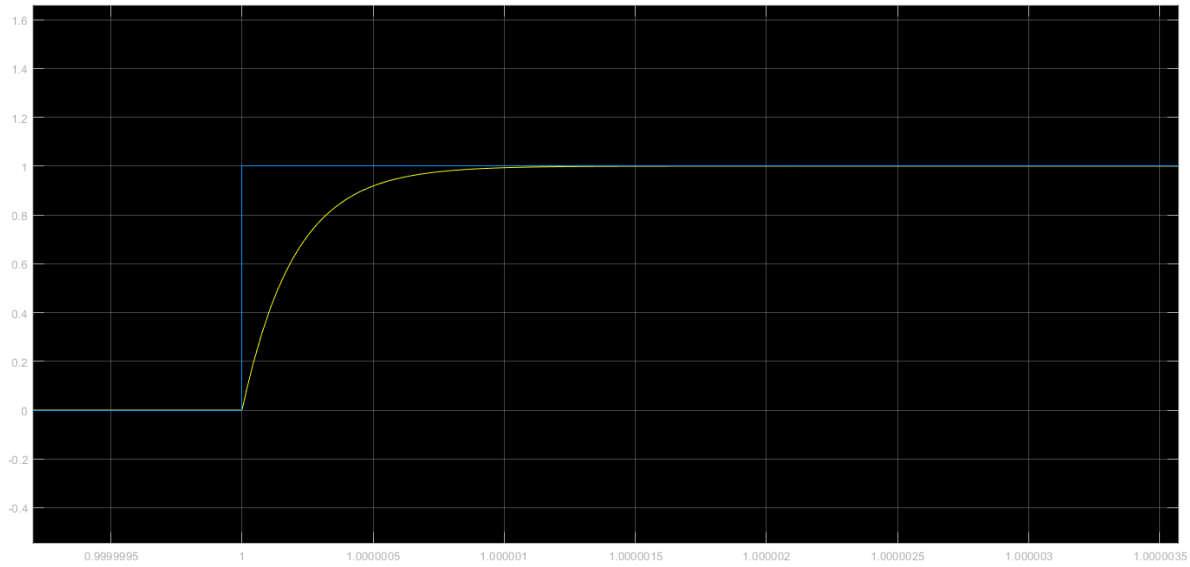


Figure 23: Step response of the system for Kd =10 & Kp =200(Zoomed)

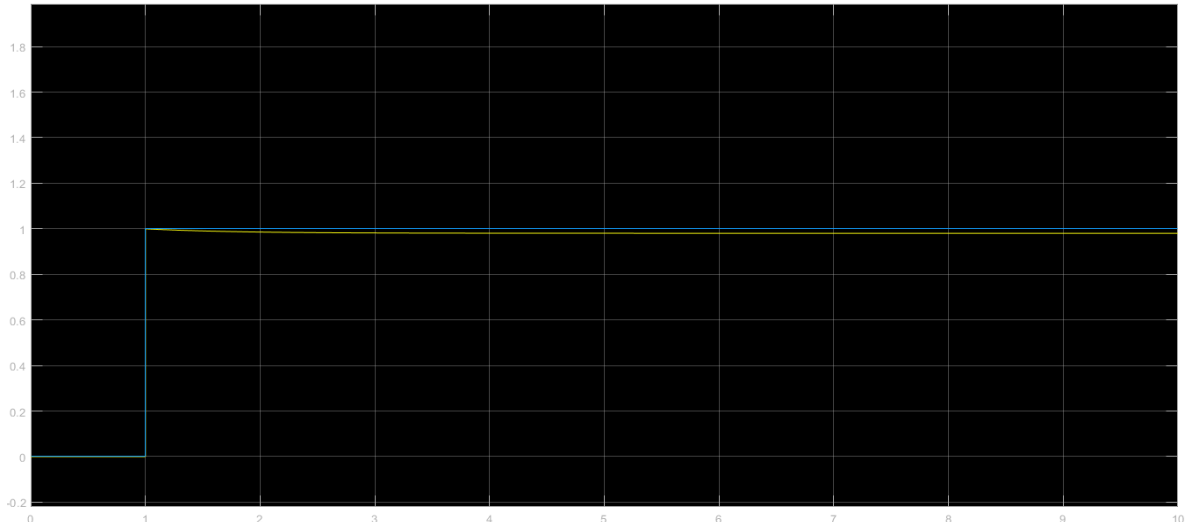


Figure 21:Step response of the system for Kp = 200 and Kd =20(Not zoomed)

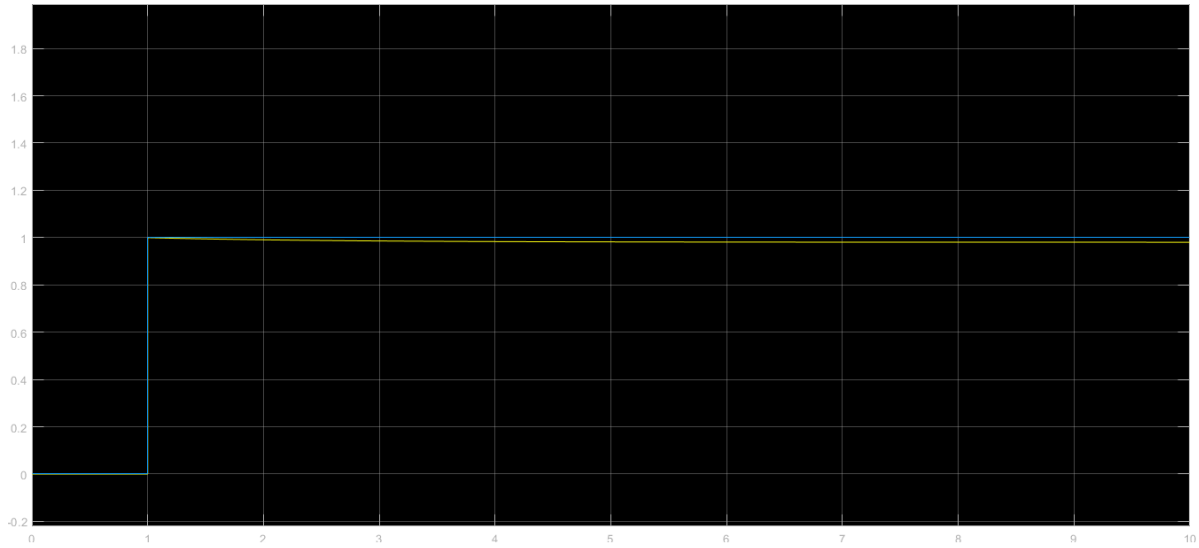


Figure 22: Step response of the system for Kp = 200 and Kd = 40(not Zoomed)

Task 4 – Design of a second order system with PID controller

- The connection to the PID controller established using the SPMT switch.
- The Closed loop circuit diagram as follows. (only showing connected elements)

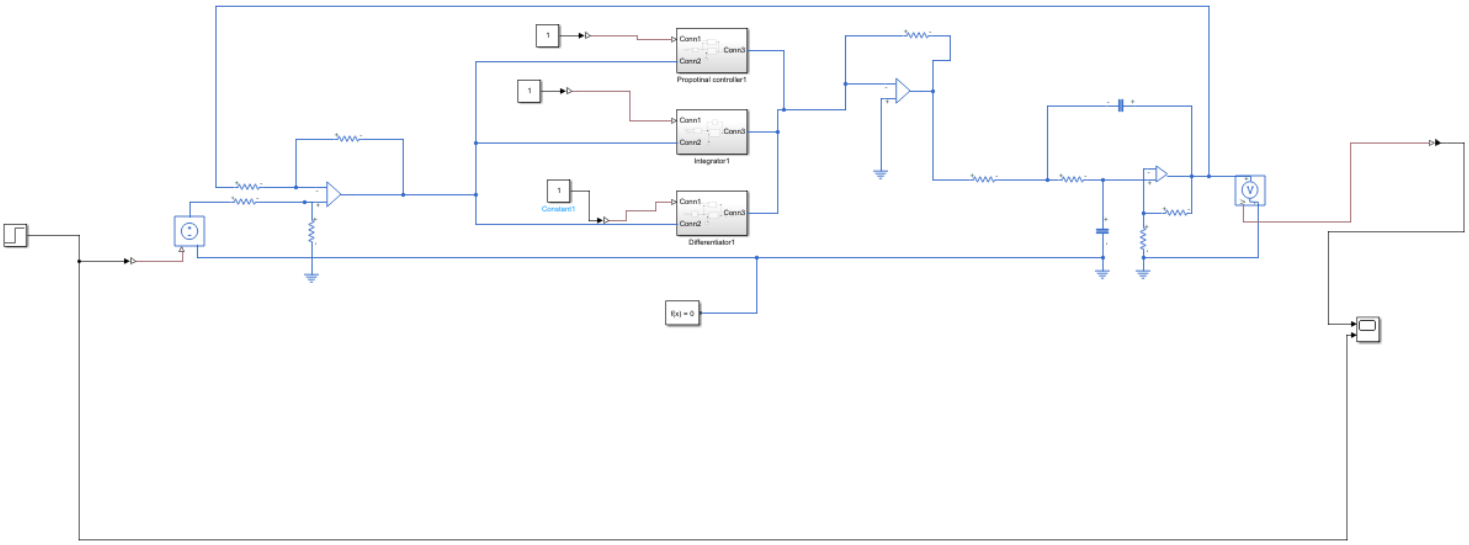


Figure 24: Circuit of PID controller connected to the system

- In the proportional controller block, all normal resistors were 1 kOhms and the value of the variable resistor was 50 kOhms and Kp value was 50.
- In the Integrator block, the capacitor was kept at 1uF and normal resistor value was 1 kOhms. And the variable resistor value was selected as 5 kOhms to keep Ki value as 200.
- In the Differentiator block, the capacitor value was kept as 100 uF and normal output resister was kept at 1 kOhms. By adjusting the variable resistor value to 400 kOhms, the Kd constant was set as 40.
- Then for Kp = 50, Ki = 200 and Kd = 40 the system was simulated and the results were observed as follows.
    - Max peak overshoot = 1 mV
    - Max peak overshoot (%) = 0.1%
    - Rise time = 109.76 ns
    - Settling time = 34.68 ms
- And also, for Kp = 100 (variable resistor = 100kOhms), Kd = 20 (variable resistor = 200kOhms) and Ki = 100 (variable resistor = 5kOhms) the circuit was simulated and the results as follows.
    - Max peak overshoot = 1 mV

- Max peak overshoot (%) = 0.1%
- Rise time = 109.84 ns
- Settling time = 32.17 ms

- The step response for the system was observed via the scope as showed in following figures.

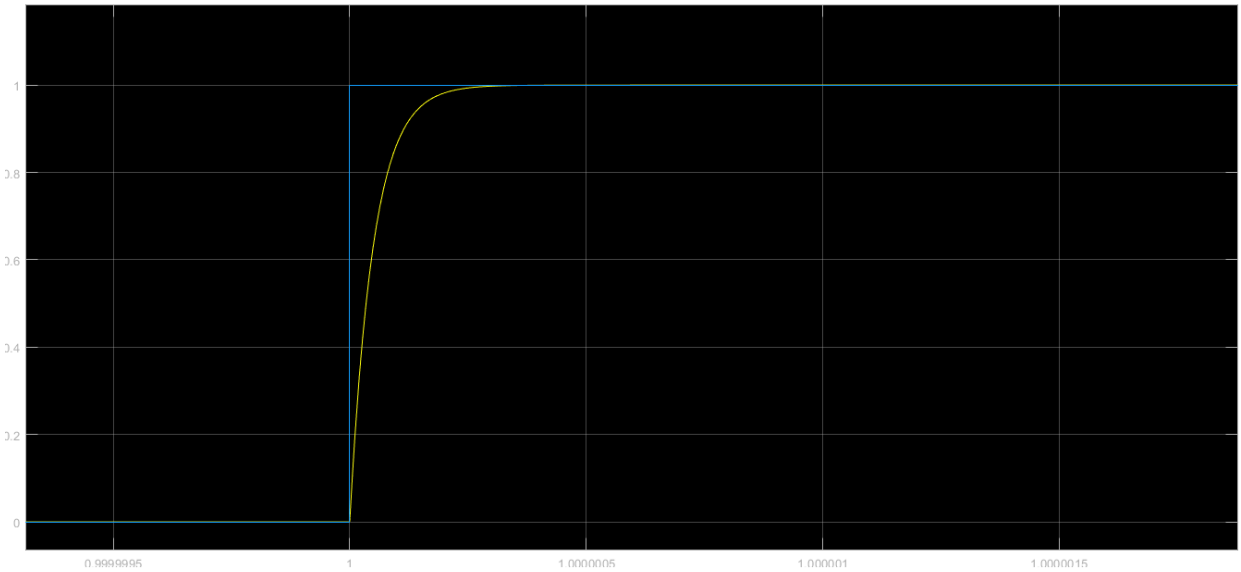


Figure 26: Step response of the system for Kp = 50, Ki = 200 and Kd = 40

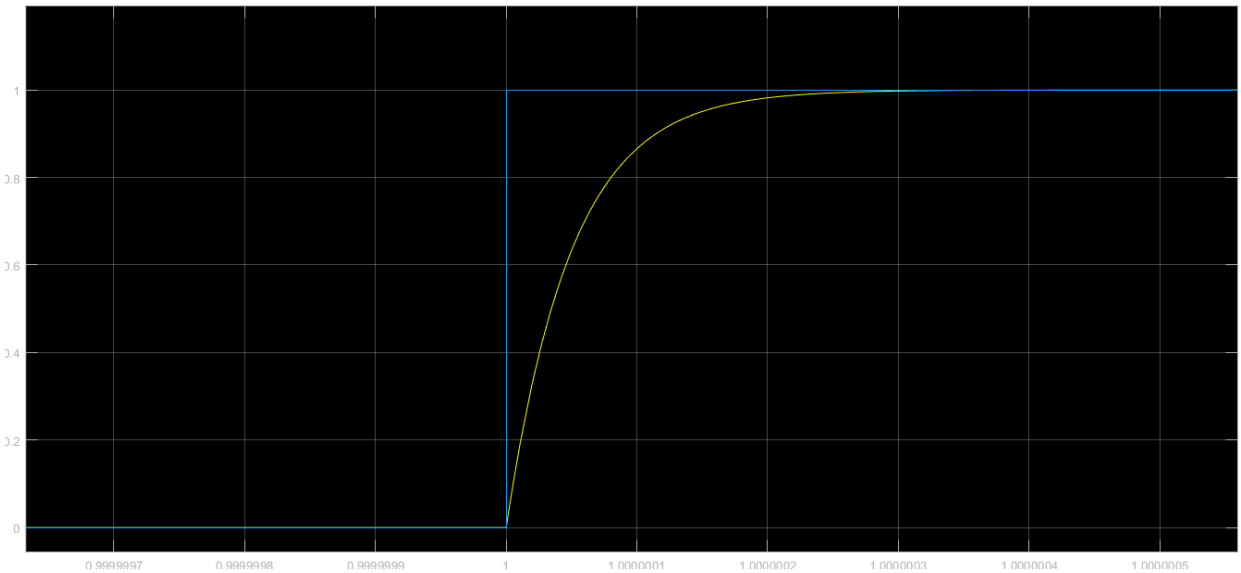


Figure 25: Step response of the system for Kp = 100, Ki = 100 and Kd = 40