EE-309 PROJECT 1

TEAM MEMBERS

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ADD/NDU

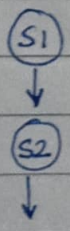
S1 R7 → MemA, ALUA
MemD → IR
+1 → ALUB
ALUOUT → PC

S2 I_{8-6} → RF-A1
RFD1 → T1
I_{5-3} → RFA2
RFD2 → T2

S3 T1 → ALUA
T2 → ALUB
ALUOUT → T3
PC → RFD3
111 → RFA3

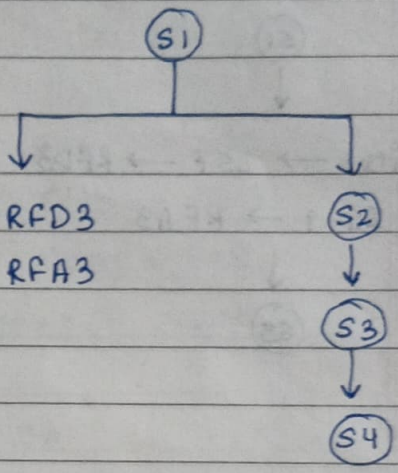
S4 T3 → RFD3
I_{11-9} → RFA3

ADI

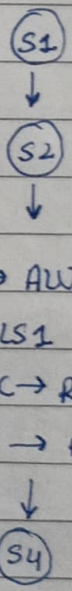


S7 T1 → ALUA
Imm(6 Bits) → SE → ALUB
ALUOUT → T3
PC → RFD3
111 → RFA3

ADC/ADZ/NDC/NDZ



ADL



S6 T1 → ALUA
T2 → LS1 → ALUB
PC → RFD3
111 → RFA3

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LHI

S1

S8 Imm(9Bits) → LS7 → RFD3
I_{11-9} → RFA3

S5

LW

S1

S9 I_{8-6} → RFA1
RFD1 → T1
I_{11-9} → RFA2
RFD2 → T2

S10 T3 → Mem A
Mem D → T1

S11 T1 → RFD3
I_{11-9} → RFA3

SW

S1

S9

S12 T3 → Mem A
T2 → Mem D

LM

S1

S13 I_{11-9} → RFA2
RFD2 → T3
I_{7-0} → TC

S14 T3 → Mem A
Mem D → T1

S15 T1 → RFD3
PEOUT2 → RFA3
TC → PE
RE T3 → ALU A
+1 → ALU B
ALUOUT → T3 PEOUT1 → TC

S16 ~~PEOUT1 → TC~~
~~T3 → T2~~
PC → RFD3
111 → RFA3

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SM

S1 → S18 → S17: TC → PE; PEOUT 2 → RFA2; RFD1 → T2

S18: ~~RFA1 → ALU~~; T3 → MemA; T2 → MemD

S19: T3 → ALUA; +1 → ALUB; ALUOUT → T3

S20: ~~T3 → T3~~; PC → RFD3; 111 → RFA3

JAL

S1 → S23: PC → RFD3; I11-9 → RFA3; A7 → ALUA; Imm(9Bits) → SE → ALUB; ALUOUT → T3

S24: T3 → RFD3; 111 → RFA3

BEQ

S1 → S21: I8-6 → RFA1; RFD1 → EQU; I11-9 → RFA2; RFD2 → EQU

COM = 1: S22: R7 → ALUA; Imm(6Bits) → SE → ALUB; ALUOUT → PC → S5

COM = 0: S5

JLR

S1 → S25: I8-6 → RFA1; RFD1 → T3; I11-9 → RFA3; PC → RFD3

S24: T1 → RFD3; 111 → RFA3

JRI

S1 → S26: I11-9 → RFA2; RFD2 → ALUA; Imm(9Bits) → SE → ALUB; ALUOUT → PC → S5

Level 1 Merge States

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S1 RF → MemA, AWA
MemD → IR
+1 → AWB
ALWOUT → PC

S2 I_{8-6} → RFA1
RFD1 → T1
I_{5-3} → RFA2
RFD2 → T2

S3 T1 → AWA
T2 → AWB
ALWOUT → T3
PC → RFD3
111 → RFA3

S4 T3 → RFD3
I_{11-9} → RFA3

S5 PC → RFD3
111 → RFA3

S6 T1 → AWA
T2 → LS1 → AWB
ALWOUT → T3
PC → RFD3
111 → RFA3

S7 T1 → AWA
Imm(6Bits) → SE → AWB
ALWOUT → T3
PC → RFD3
111 → RFA3

S8 Imm(9Bits) → LS7 → RFD3
I_{11-9} → RFA3

S9 I_{8-6} → RFA1
RFD1 → T1, EQU
I_{11-9} → RFA2
RFD2 → T2, EQU, T3

S10 T3 → MemA
MemD → T1

S11 T1 → RFD3
I_{11-9} → RFA3

S12 T3 → MemA
T2 → MemD

S13 T1 → ~~MemA~~ RFD3
PEOUT2 → RFA3
TC → PE
T3 → AWA
+1 → AWB
ALWOUT → T3, PEOUT1 → TC

S14 ~~PEOUT1 → TE~~
~~I2 → T3~~
PC → RFD3
111 → RFA3

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S15 TC → PE
PEOUT2 → RFA2
RFD1 → T2, POUT1 → TC

S16 ~~POUT1 → TC~~
T3 → ALUA
+1 → ALUB
ALUOUT → T3

S17 R7 → ALU A
Imm(6 Bits) → SE → ALUB
ALUOUT → PC

S18 PC → RFD3
I_{11-9} → RFA3
R7 → ALU A
Imm (9 Bits) → SE → ALUB
ALUOUT → T3

S19 T3 → RFD3
111 → RFA3

S20 I_{8-6} → RFA1
RFD1 → T3
I_{11-9} → RFA3
PC → RFD3

S21 I_{11-9} → RFA2
RFD2 → ALUA
Imm(9 Bits) → SE → ALUB
ALUOUT → PC

S15 PC → RFD3
I_{11-9} → RFA3
R7 → ALUA
Imm(9Bit) → SE → ALUB
ALUOUT → T3

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⇒ S2 And S9 Both are Merged

S2 I_{8-6} → RFA1
RFD1 → T1, EQU
I_{11-9}, I_{5-3} → RFA2 [signal of MUX decides RFA2]
RFD2 → T2, EQU, T3

⇒ S4, S5, and ~~S8~~ can be Merged

S5 PC → RFD3
111 → RFA3
R7 → ALUA
Imm(9 Bits) → SE → ALUB
ALUOUT → T3

⇒ S3, S6 And S7 can be Merged
T1 → ALU A
LS1, SE<<1, T2 → ALU B [signal of MUX decides ALU B]
ALUOUT → T3
PC → RFD3
111 → RFA3

⇒ S7, S8 and S20 can be Merged
~~T3~~, T3, PC, LSF → RFD3 [signal of MUX decides RFD3]
I_{11-9} → RFA3
I_{8-6} → RFA1
RFD1 → T3

** And Signals of MUX are decided by op-code and Funcode-code.

Level 2 Merged States

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S1 R7 → MemA, ALUA
Mem D → IR
+1 → ALUB
ALUOUT → PC

S2 I_{8-6} → RFA1
RFD1 → T1, EQU
I_{5-3}, I_{11-9} → RFA2
RFD2 → T2, EQU, T3

S3 T1 → ALUA
LS1, SE_{6-16}, T2 → ALUB
ALUOUT → T3
PC → RFD3
111 → RFA3

S4 T3, PC, LS7 → RFD3
I_{11-9} → RFA3
I_{8-6} → RFA1
RFD1 → T31

S5 T3, PC → RFD3
111 → RFA3
R7 → ALUA
Imm (9 Bits) → SE → ALUB
ALUOUT → T3

S6 T3 → Mem A
Mem D → T1

S7 T1 → RFD3
I_{11-9} → RFA3

S8 T3 → Mem A
T2 → Mem D

S9 T1 → RFD3
PEOUT2 → RFA3
TC → PE
T3 → ALUA
+1 → ALUB
ALUOUT → T3
PEOUT1 → TC

S10 TC → PE
PEOUT2 → RFA1
RFD2 → T2
POUT1 → TC

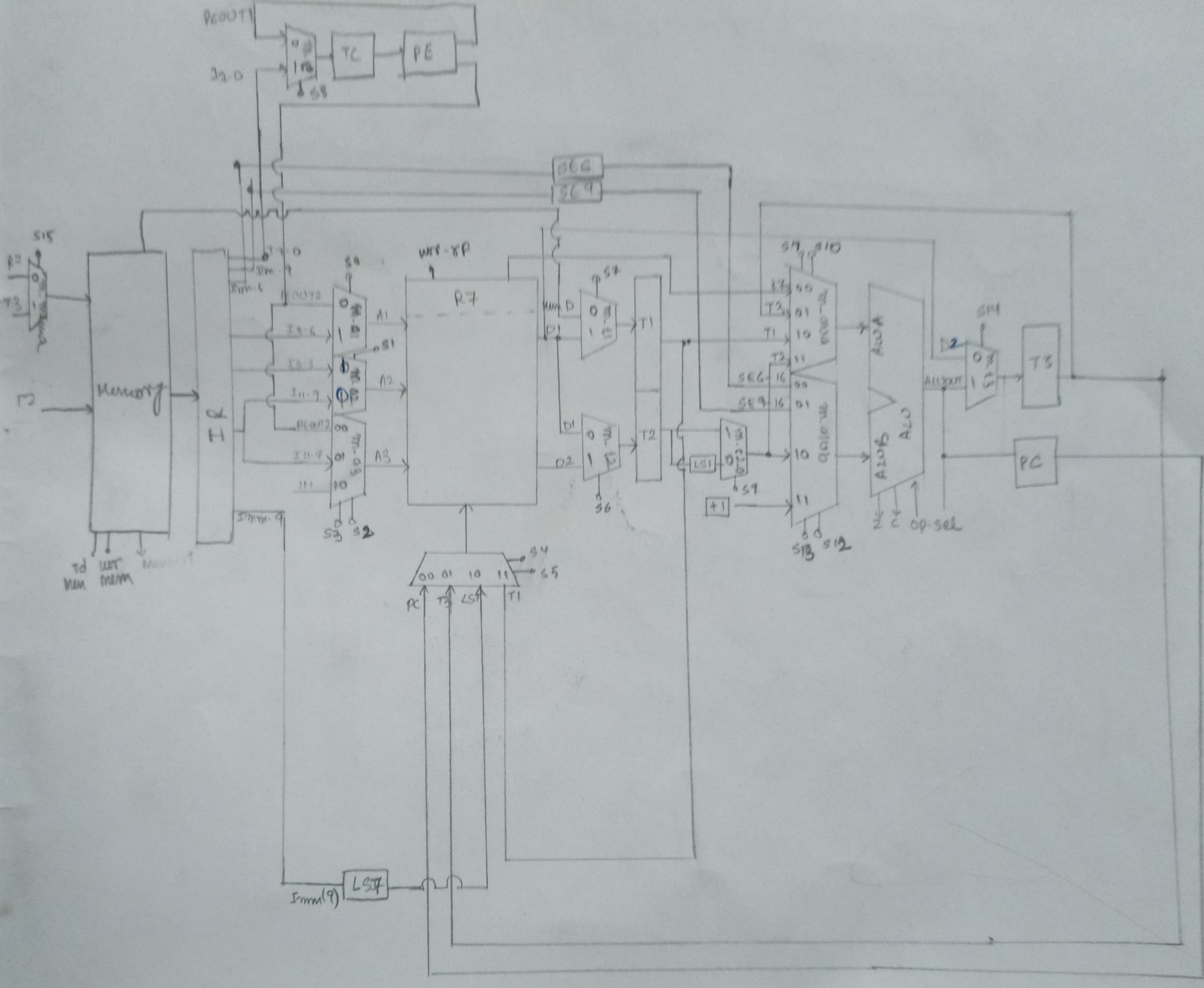
S11 T3 → ALUA
+1 → ALUB
ALUOUT → T3

S12 R7 → ALUA
Imm(6 Bits) → SE → ALUB
ALUOUT → PC

S13 I_{11-9} → RFA2
RFD2 → T2

S14 T2 → ALUA
Imm (9 Bits) → SE → ALUB
ALUOUT → PC

S15 on Previous page



PCOUT1
TC
PE
S8
SE6
SE9
S15
Memory
IR
rd mem
wr mem
wr-RF
R7
A1
A2
A3
D1
D2
S2
S4
S5
PC
T3
LS7
T1
Imm(9)
S7
S6
T2
LS1
+1
S10
SE6-16
SE9-16
S12
ALU
Z
C
op-sel
ALUOUT
S14
PC

Multiplexers

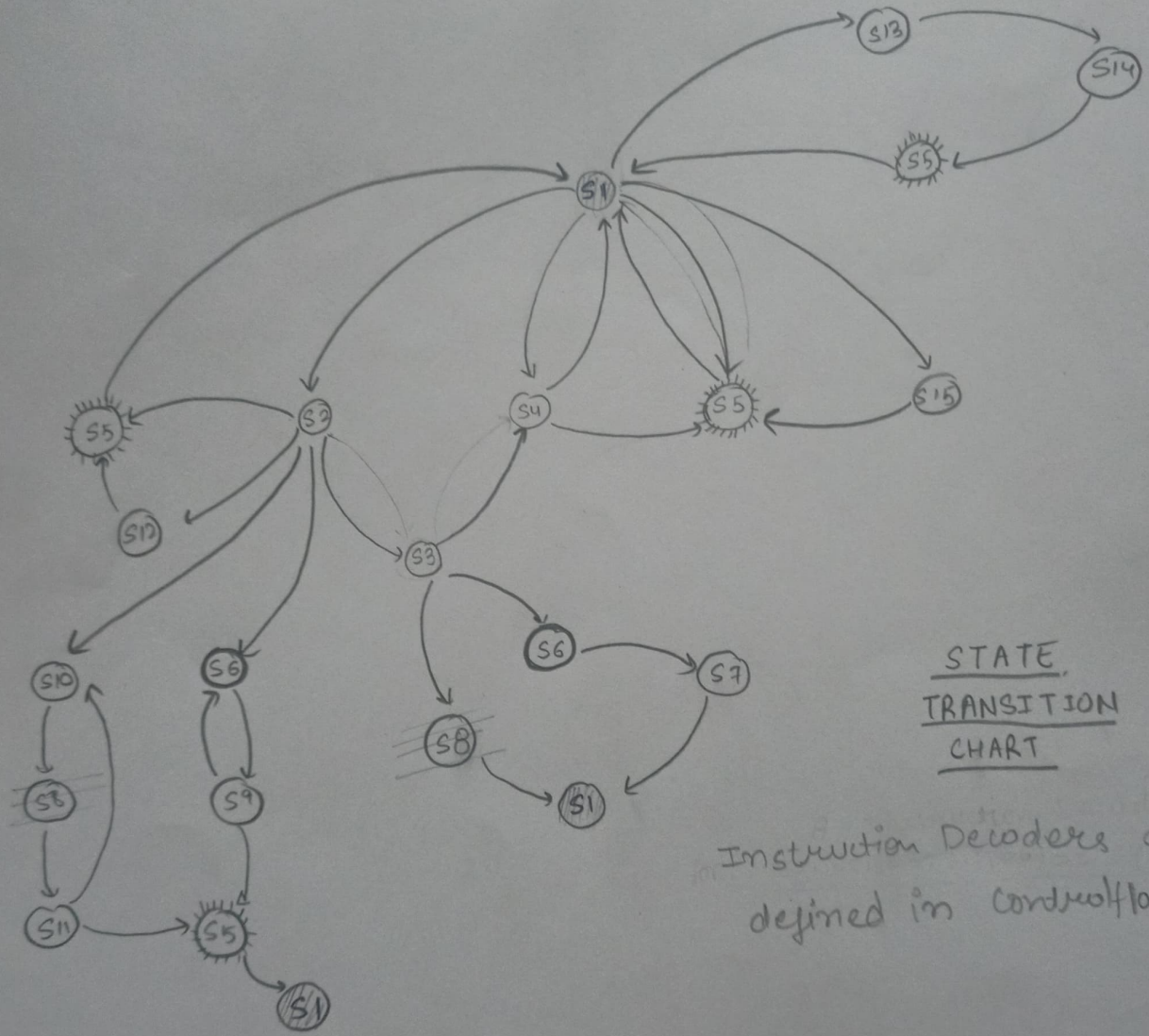
Total Multiplexers used are 12

	MUX NAME	CONTROL SIGNALS
1	m_a1	S0
2	m_a2	S1
3	m_a3	S2, S3
4	m_d3	S4, S5
5	m_t2	S6
6	m_t1	S7
7	m_tc	S8
8	m_t2_0	S9
9	m_alua	S10, S11
10	m_alub	S12, S13
11	m_t3	S14
12	m_mema	S15

15 control signals for Multiplexers

#

wr_mem - Memory write signal
rd_mem - Memory read signal
en_t1 - enable deregister t1
en_t2 - enable deregister t2
en_t3 - enable deregister t3
en_pc - enable deregister pc
wr_rf - Register file write signal
en_tc - enable deregister TC
op-sel - operational - selector for ALU
op-code - Ir (15 down to 12)
condition_code - Ir (1 down to 0)



STATE TRANSITION CHART

Instruction Decoders are defined in Controlflow in VHDL.

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⇒ ADD/NDU

S1 # S15 = 0

↓

S2 # S0 = 1, S1 = 1, S7 = 1, S6 = 1

↓

S3 # S10 = 0, S11 = 1, S9 = 1, S12 = 0, S13 = 1, S14 = 1, S4 = 0, S5 = 0

Also, if op-code (2-0) = 01, op-sel = '0' for Addition

If op-code (1-0) = 10, op-sel = '1' for AND

↓

S4 # S4 = 1, S5 = 0, S2 = 1, S3 = 0

⇒ ADC/ADZ/NDC/NDZ

S1

C/Z = 0 | C/Z = 1

↓ ↓

S5 Same As (ADD/NDU)

S4 = 0, S5 = 0

S2 = 0, S3 = 1

⇒ ADL

S1

↓

S2 # S0 = 1, S1 = 1, S7 = 1, S6 = 1

↓

S3 # S10 = 0, S11 = 1, S9 = 0, S12 = 0, S13 = 1, S14 = 1

op-sel = '0' for ADDITION

↓

S4 # S4 = 1, S5 = 0, S2 = 1, S3 = 0

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⇒ ADI

(S1) # S15 = 0

↓

(S2) # S0 = 1, S1 = 1, S7 = 1, S6 = 1

↓

(S3) # S10 = 0, S11 = 1, S12 = 0, S13 = 0, S14 = 1, S4 = 0, S5 = 0

↓ op-sel = 0

(S4) # S4 = 1, S5 = 0, S2 = 1, S3 = 0

⇒ LHI

(S1) # S15 = 0

↓

(S4) # S4 = 0, S5 = 1, S2 = 1, S3 = 0

↓

(S5) # S4 = 0, S5 = 0, S2 = 0, S3 = 1

⇒ LW

(S1) # S15 = 0

↓

(S2) # S0 = 1, S7 = 1, S1 = 0, S6 = 1,

↓

(S3) # S10 = 0, S11 = 1, S12 = 0, S13 = 0, S14 = 1, S4 = 0, S5 = 0

↓ op-sel = 0

(S6) # S15 = 1

↓

(S7) # S4 = 1, S5 = 1, S2 = 1, S3 = 0

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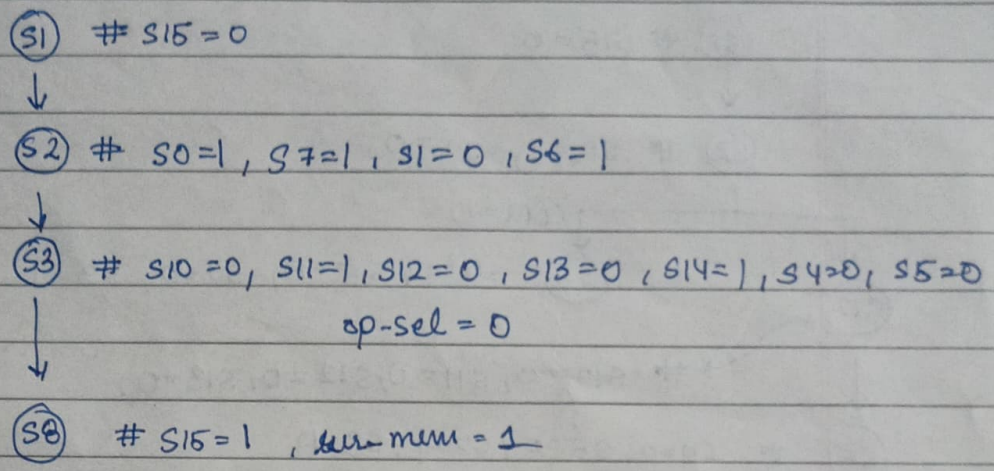
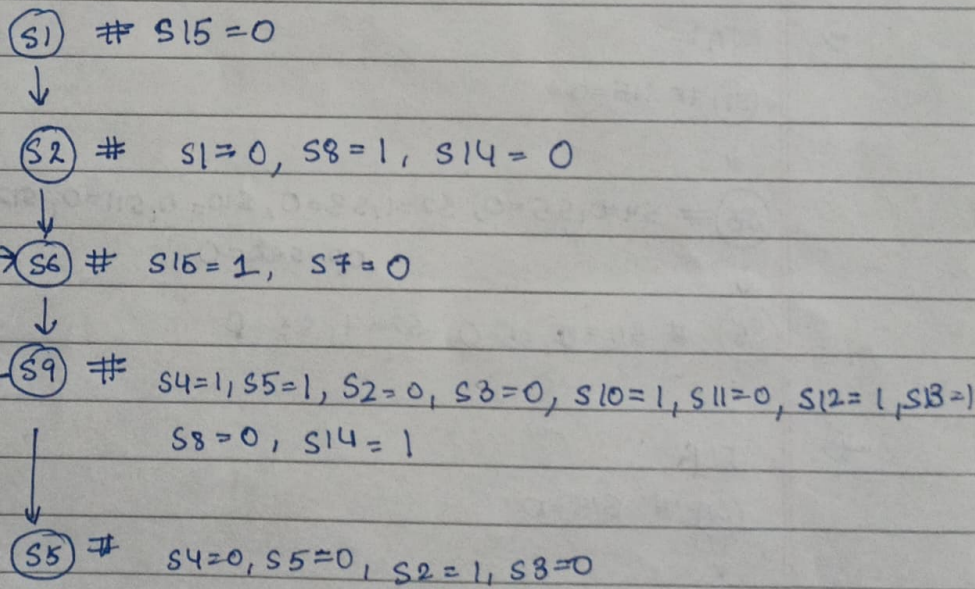
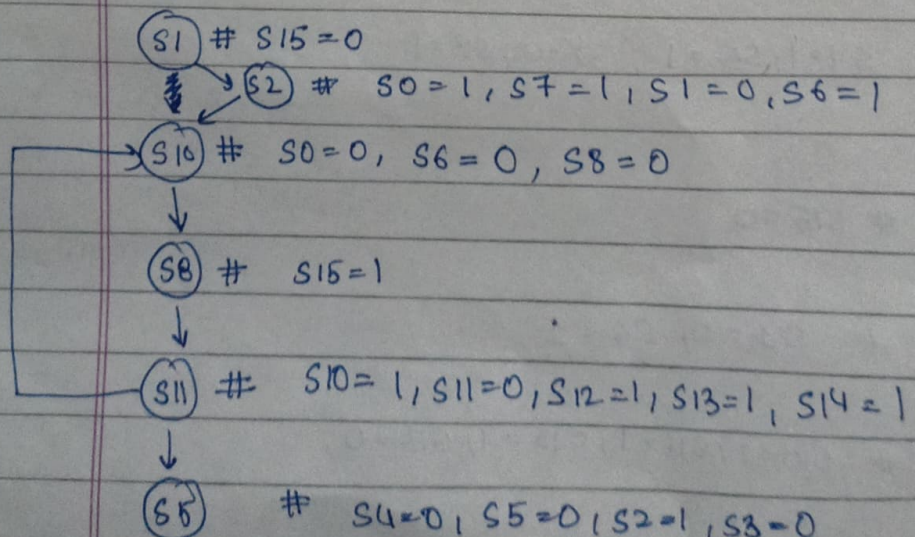
⇒ SW



⇒ LM



⇒ SM



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⇒ BEQ

(S1) # S15=0

↓

(S2) # S0=1, S1=0,

COM=0 → (S5) S4=0, S5=0, S2=0, S3=1

(S12)

↓

(S5) # S4=0, S5=0, S2=0, S3=0

S10=0, S11=0, S12=0, S13=0,

⇒ JAL

(S1) # S15=0

↓

(S5) # S4=0, S5=0, S2=1, S3=0, S10=0, S11=0, S12=1, S13=0, S14=1

op-sel=0

↓

(S5) # S4=0, S5=0, S2=1, S3=0

⇒ JLR

(S1) # S15=0

↓

(S4) # S0=1, S1=1, S2=0, S3=0, S4=0, S5=0

↓

(S5) # S4=1, S5=1, S2=0, S3=1

⇒ JRI

(S1) # S15=0

↓

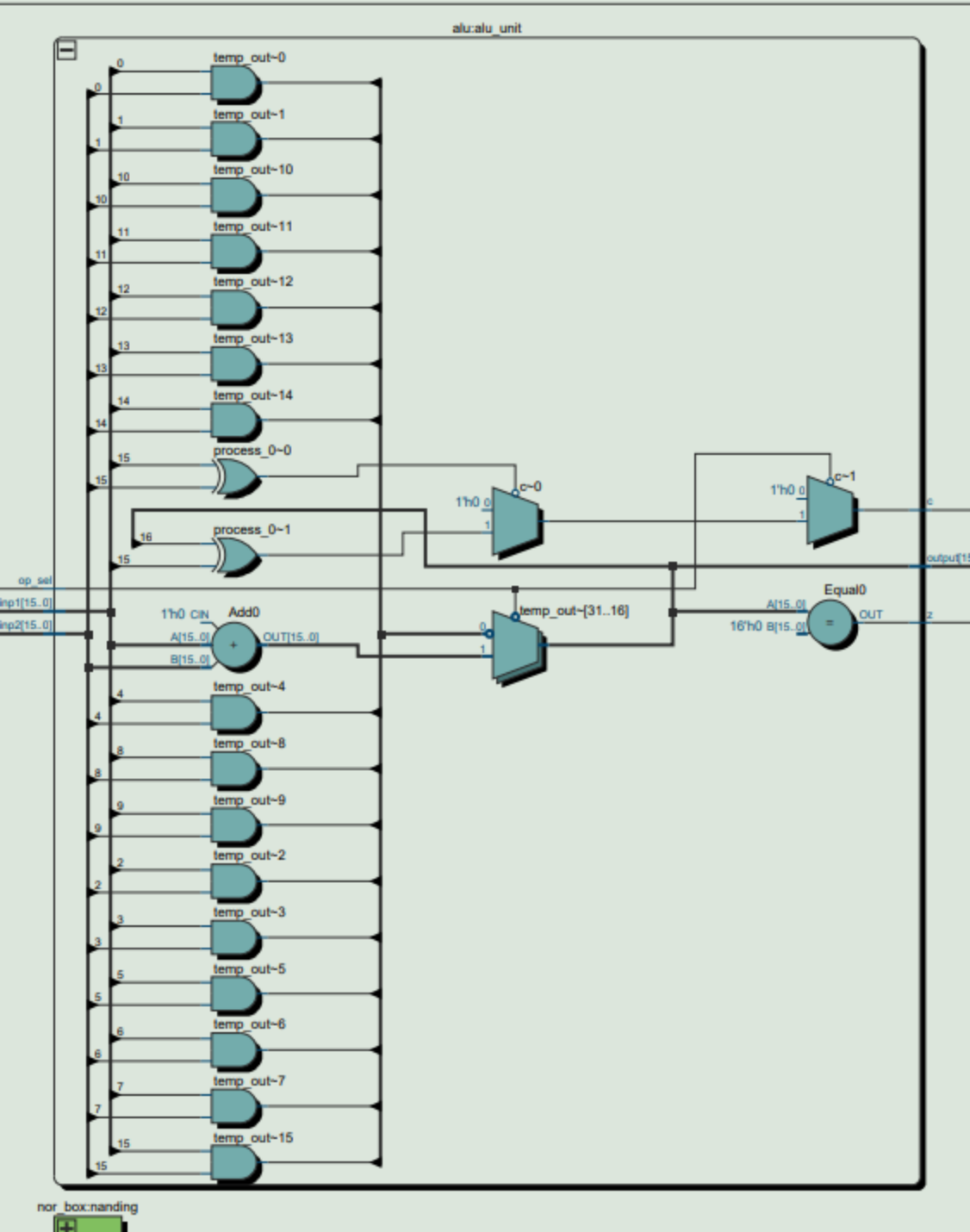
(S13) # S1=0, S6=1

↓

(S14) # S10=1, S11=1, S12=1, S13=0,

↓

(S5) # S4=0, S5=0, S2=0, S3=1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temp_out~0
temp_out~1
temp_out~10
temp_out~11
temp_out~12
temp_out~13
temp_out~14
process_0~0
process_0~1
c~0
c~1
1'h0
op_sel
inp1[15..0]
inp2[15..0]
1'h0 CIN
Add0
A[15..0]
B[15..0]
OUT[15..0]
temp_out~[31..16]
Equal0
16'h0 B[15..0]
OUT
output[15
temp_out~4
temp_out~8
temp_out~9
temp_out~2
temp_out~3
temp_out~5
temp_out~6
temp_out~7
temp_out~15
nor_box:nanding