:: Unit-2- Non-linear Wave Shaping ::

PART-A: CLIPPING CIRCIUTS SUMMARY

- When non-linear circuit elements such as diodes, transistors and FETs are used in waveshaping applications, the resultant circuit is called a "non-linear waveshping circuit".
- A semiconductor diode is used as a switch; when forward-biased, it is an ON switch and when reverse-biased it is an OFF switch.
- Due to diffusion and transition capacitances, a diode does not respond instantaneously for a given excitation and there results some delay in switching the device from one state to the other state.
- The reverse recovery time of a diode is defined as the time taken for the diode reverse current to fall to 10 per cent of its forward current value when the diode is suddenly switched from the ON state into the OFF state.
- ***R*** in a clipping circuit is normally chosen as the geometric mean of the diode forward and reverse resistances, i.e., $R = \sqrt{R_f R_r}$.
- A high-frequency sine wave can be converted to a near square wave by using a limiter.
- A slicer is a clipping circuit that clips the input signal at two levels, either during the positive or the negative going period.
- A comparator tells us the time instant at which the input reaches a reference level.
- In a simple diode comparator, there is a sudden change in slope at the break point. However, the variation of the signal at the output is similar to the variation of the signal at the input after the break point.
- To improve the sharpness of a break region, an amplifier may be provided either before or after the comparator.
- In certain comparators—called regenerative comparators—like Schmitt trigger (which will be discussed later), the variation at the output does not follow the variation at the input; the output abruptly changes amplitude when the input reaches the reference level.

MULTIPLE CHOICE QUESTIONS

1. In a shunt diode clipper, the signal will be transmitted when the diode is:
    1. In the ON state
    2. In the OFF state
    3. In any one of the state
    4. None of the above
2. Clipping circuits transmit _____ the input signal.
    1. a part of
    2. whole of

3. negative portion of
4. no part of

3. The value of R in a clipper is chosen as:
   1. R_f/R_r
   2. R_r/R_f
   3. $R_f\ R_r$
   4. $\sqrt{R_f R_r}$
4. The slope of the transfer characteristic in a series diode clipper is _____ when the diode is ON.
   1. 1
   2. 1/2
   3. 1/3
   4. 2
5. In series diode clipper the signal is transmitted when the diode is:
   1. In the ON state
   2. In the OFF state
   3. In any one of the states
   4. None of the above
6. Transfer characteristic of a clipping circuit is drawn between:
   1. Input voltage and output current
   2. Output voltage and input current
   3. Input voltage and output voltage
   4. Output voltage and output current
7. Which of the following circuits is used to measure accurate time delays?
   1. Comparator
   2. Clipping circuits
   3. Slicer

4. Limiter

8. An example of a regenerative comparator is:

   1. Schmitt trigger
   2. Limiter
   3. Slicer
   4. Simple diode comparator

9. The following circuit can also be used as an amplitude comparator:

   1. Clipping circuit
   2. Slicer
   3. Both slicer and clipper
   4. None of the above

10. An emitter-coupled transistor clipper is a:

   0. Two-level clipper
   1. One level clipper
   2. One and two-level clipper
   3. None of the above

SHORT ANSWER QUESTIONS

1. What is a clipping circuit?
2. Draw the circuit of a negative peak clipper.
3. Compare series and shunt clippers.
4. Explain the working of a limiter.
5. Draw a slicer circuit that slices the given sinusoidal input signal during the negative going half-cycle.
6. What is a comparator? Explain a simple diode comparator.
7. Specify three applications of comparator.
8. What is an emitter-coupled clipper?

LONG ANSWER QUESTIONS

1. Explain the working of a diode shunt clipper as an amplitude comparator. What are the limitations? Suggest methods to improve the sharpness of the break region.
2. With the help of waveforms, explain how a comparator is used for:
   (a) Measurement of time delays (b) Measurement of phase and (c) Generating timing markers.
3. Give the circuits of different types of shunt clippers and explain their operation with the help of their transfer characteristic.
4. Draw the circuit diagram of an emitter-coupled clipping circuit and draw its transfer characteristic indicating all intercepts, slopes and voltage levels.
5. Draw the circuit diagram of a limiter using Zener diodes and explain its operation with the help of its transfer characteristics.

SOLVED PROBLEMS

Example 1: For the two-level clipper in Fig.2.1(a), the input varies linearly from 0 to 150 V. Plot the transfer characteristic and obtain the output voltage. Assume ideal diodes.

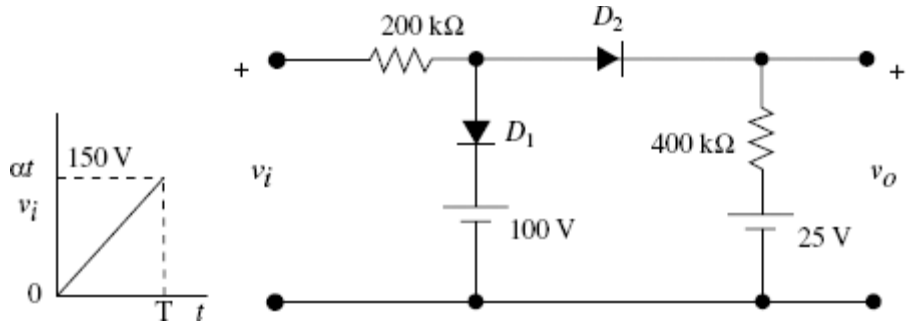


FIGURE 2.1(a) The given two-level clipper circuit

Solution: For ideal diodes $R_f = 0$, $R_r = \infty$, $V_\gamma = 0$

1. $0 \le v_i < 25$ V then D_1 and D_2 are OFF.
   The resultant circuit is as shown in Fig. 2.1(b).

   $v_o = 25$ V, ***i.e.***, till v_i rises to 25 V, $v_o = 25$ V.

2. $25 \text{ V} \le v_i \le 100$ V
   D_1 is OFF and D_2 is ON and the resultant circuit is shown in Fig. 2.1(c).

   Using the superposition theorem:

$$v_o = v_i \times \frac{400}{200 + 400} + 25 \times \frac{200}{200 + 400}$$

$$v_o = \frac{2}{3} v_i + \frac{25}{3} \qquad (1)$$

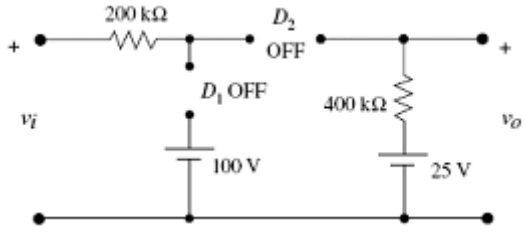


FIGURE 2.1(b) Circuit when $\boldsymbol{D}_1$ is OFF and $\boldsymbol{D}_2$ is OFF

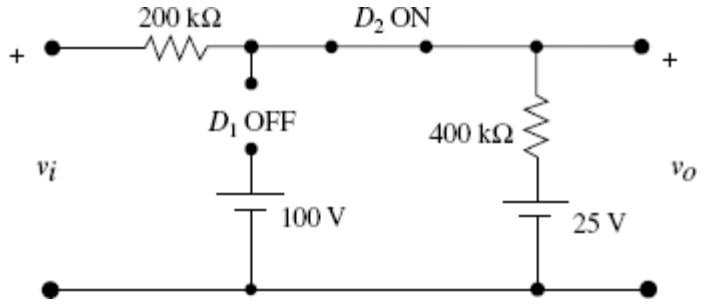


FIGURE 2.1(c) Circuit when $\boldsymbol{D}_1$ is OFF and $\boldsymbol{D}_2$ is ON

Since $\boldsymbol{v_i}$(min) = 25 V,

$$v_O = \frac{50}{3} + \frac{25}{3} = \frac{75}{3} = 25 \text{ V}$$

To find $\boldsymbol{v_{i(\max)}}$ that satisfies above relation (1)

Put $\boldsymbol{v_o}$ = 100 V

$$v_O = \frac{2}{3}v_i + \frac{25}{3} \quad 100 \text{ V} = \frac{2}{3}v_i + \frac{25}{3} \quad \frac{2}{3}v_i = \left(100 - \frac{25}{3}\right) = \frac{275}{3}$$

$$v_i = \frac{275}{3} \times \frac{3}{2} = 137.5 \text{ V}$$

3. for $\boldsymbol{v_i}$ > 137.5 V both $\boldsymbol{D}_1$ and $\boldsymbol{D}_2$ conduct and $\boldsymbol{v_o}$ = 100 V

We thus have,

For 0 < $\boldsymbol{v_i}$ < 25V, $\boldsymbol{v_o}$ = 25 V

25 V < $\boldsymbol{v_i}$ < 137.5 V, $\boldsymbol{v_o} = \frac{2}{3}v_i + 8.333$ $\boldsymbol{v_i}$ > 137.5 V, $\boldsymbol{v_o}$ = 100 V

The transfer characteristic is presented in Fig. 2.1(d).

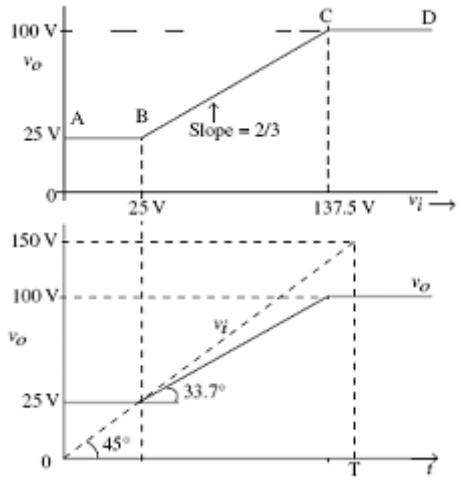


FIGURE 2.1(d) Transfer characteristic and output of the circuit in Fig. 2.1(a)

Example 2: For the circuit shown in Fig. 2.2(a), plot the transfer characteristic for v_i varying from 0 to 150 V linearly.

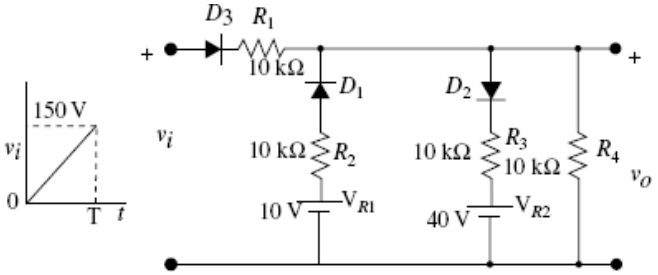
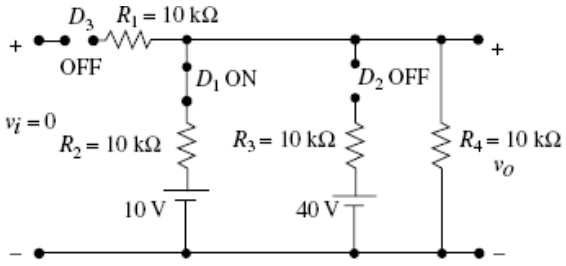


FIGURE 2.2(a) Clipping circuit with input

Solution:

1. When $v_i = 0$, D_1 is ON and D_2 and D_3 are OFF, the equivalent circuit to compute the output is as shown in Fig. 2.2(b).



2.

FIGURE 2.2(b) Equivalent circuit of Fig. 2.2(a) when D_1 is ON and D_2 and D_3 are OFF

$$v_O = \frac{10\text{ V} \times 10\text{ k}\Omega}{10\text{ k}\Omega + 10\text{ k}\Omega} = 5\text{ V}$$

From this it is clear that for D_3 to conduct v_i should rise to 5 V.

Till v_i = 5 V, v_o = 5 V.

3. For $5 < v_i < 10$

D_1, and D_3 are ON and D_2 is OFF. The corresponding circuit is shown in Fig. 2.2(c).

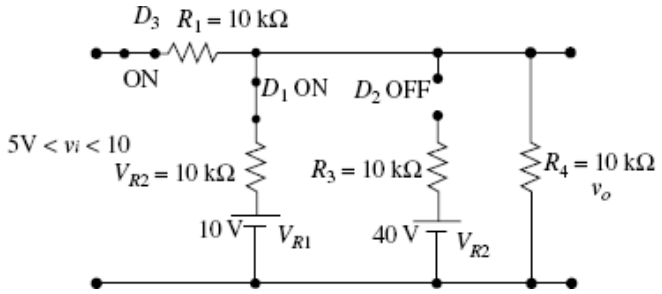


FIGURE 2.2(c) Circuit of Fig. 2.2(a) when $\boldsymbol{D}_1$, and $\boldsymbol{D}_3$ are ON and $\boldsymbol{D}_2$ is OFF

Using the superposition theorem:

$$v_o = V_{R1} \times \frac{R_4||R_1}{R_2 + (R_4||R_1)} + v_i \times \frac{R_2||R_4}{R_1 + (R_2||R_4)}$$

$$v_o = 10 \times \frac{5}{10+5} + v_i \times \frac{5}{10+5} = \frac{10}{3} + \frac{v_i}{3}$$

For $\boldsymbol{v_o}$ = 10 V

$$v_o = \frac{10}{3} + \frac{v_i}{3} \qquad \frac{v_i}{3} = 10 - \frac{10}{3} = \frac{20}{3}\ \text{V}$$

$\boldsymbol{v_i}$ = 20 V

Therefore, for 5 V < $\boldsymbol{v_i}$ < 20 V.

$$v_o = \frac{v_i}{3} + \frac{10}{3}$$

4. For $\boldsymbol{v_i}$ > 20 V and $\boldsymbol{v_o}$ < 40 V

$\boldsymbol{D}_3$ conducts and $\boldsymbol{D}_1$ and $\boldsymbol{D}_2$ are OFF. The resultant circuit is shown in Fig. 2.2(d).

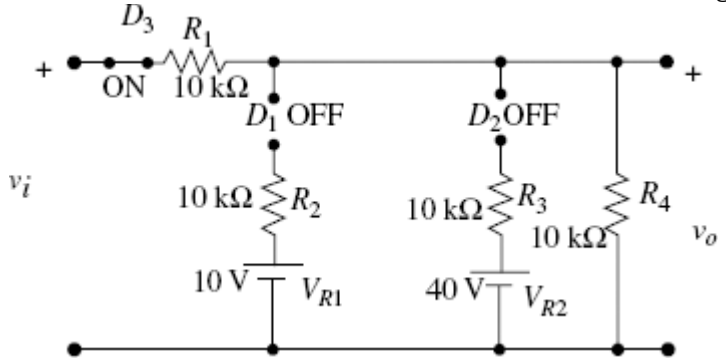


FIGURE 2.2(d) Equivalent circuit to compute the output when $\boldsymbol{D}_3$ is ON and $\boldsymbol{D}_1$ and $\boldsymbol{D}_2$ are OFF

$$v_o = v_i \times \frac{10}{10+10} = \frac{v_i}{2}$$

For $\boldsymbol{v_o}$ = 40 V, $\boldsymbol{v_i}$= 2 × $\boldsymbol{v_o}$ = 2 × 40 V = 80 V

For 20 V < $\boldsymbol{v_i}$ < 80 V, $\boldsymbol{v_o} = \frac{v_i}{2}$

5. For $\boldsymbol{v_i}$ > 80, $\boldsymbol{D}_3$ and $\boldsymbol{D}_2$ conduct and $\boldsymbol{D}_1$ is OFF, the circuit is in Fig. 2.2(e).

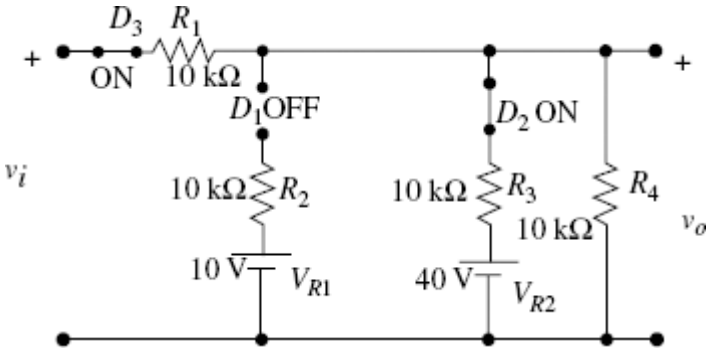


FIGURE 2.2(e) Equivalent circuit when D_3 and D_2 are ON and D_1 is OFF

$$v_O = v_i \times \frac{5}{10+5} + 40 \times \frac{5}{10+5}$$

$$v_O = \frac{v_i}{3} + \frac{40}{3} = \frac{v_i + 40}{3}$$

At $v_i = 150$, $v_o = \frac{150+40}{3} \approx 63.33$V

$0 < v_i < 5$V, $v_o = 5$ V $5 < v_i < 20$ V, $v_o = \frac{v_i}{3} + \frac{10}{3}$ 20 V $< v_i <$ 80 V, $v_o = \frac{v_i}{2}$

$v_i > 80$ V, $v_o = \frac{v_i}{3} + \frac{40}{3}$

The transfer characteristic is presented in Fig. 2.2(f).

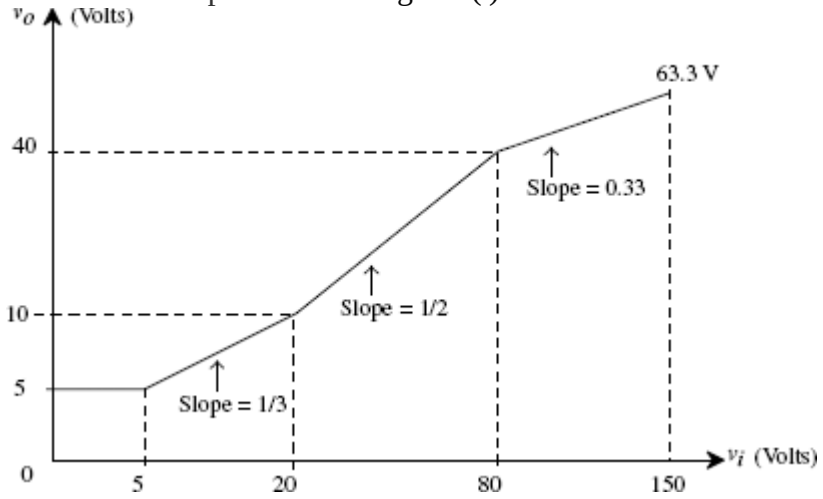


FIGURE 2.2(f) Transfer characteristic of Fig. 2.2 (a) for the given input

UNSOLVED PROBLEMS

1. For the clipper circuit shown in Fig. 2p.1, the input v_i = 100 sinωt. Plot the transfer characteristic and the input and output waveforms. Assume ideal diodes.

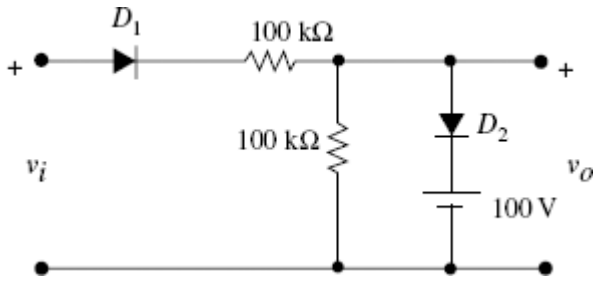


FIGURE 2p.1 The given clipping circuit for problem 1

2. For the clipper circuit shown in Fig. 2p.2, the input v_i = 50 sin ωt. Plot the transfer characteristic and the input and output waveforms. Assume ideal diodes.

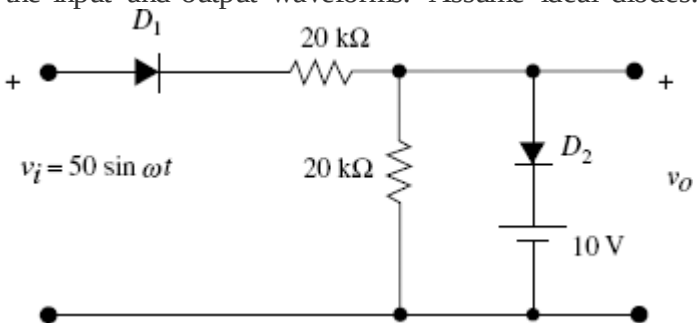


FIGURE 4p.2 Clipping circuit

3. The input to the two-level clipper shown in Fig. 2p.3, varies linearly from 0 to 100 V. Plot the transfer characteristic and obtain the output voltage. Assume ideal diodes.

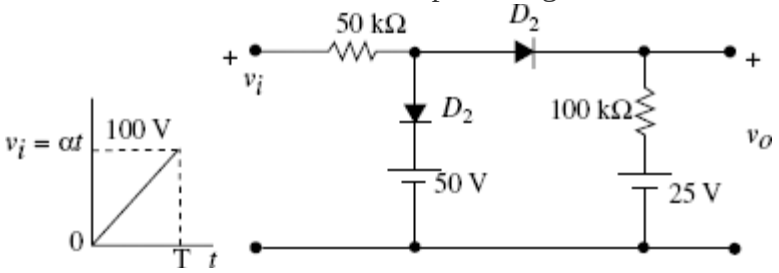


FIGURE 2p.3 The given Clipping circuit for problem 2

4. For the circuit shown in Fig. 2p.4, with v_i varying linearly up to 150 V, obtain the transfer characteristic and the output.

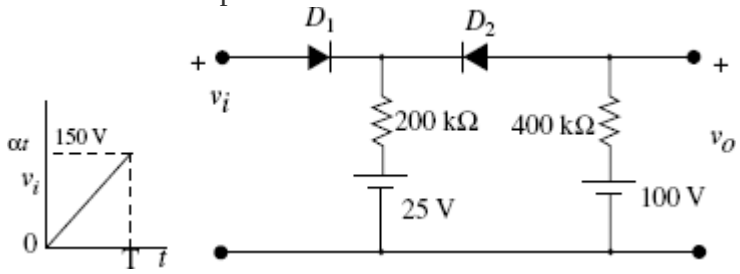


FIGURE 2p.4 Clipping circuit with input

5. For the circuit shown in Fig. 2p.5, v_i varies linearly up to 100 V. Obtain the transfer characteristic and the output.

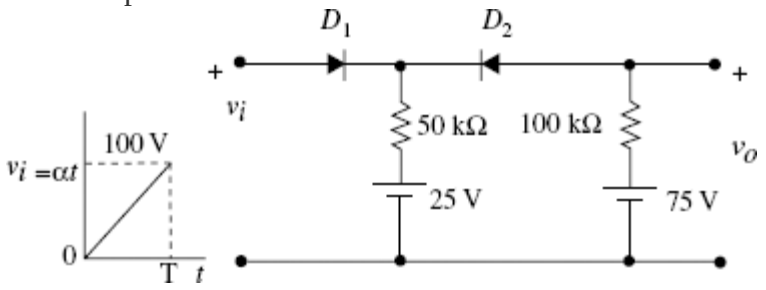


FIGURE 2p.5 The clipping circuit for problem 3

6. For the circuit shown in Fig. 2p.6, plot the transfer characteristic for v_i varying from 0 V to 75 V linearly.

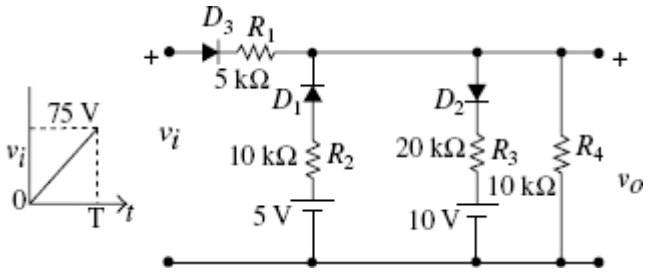


FIGURE 2p.6 The clipping circuit for problem 4

7. For the circuit shown in Fig. 2p.7, R_f = 200 Ω, R = 20 kΩ, V_γ = 0 V. Sketch the output waveform for the given input.

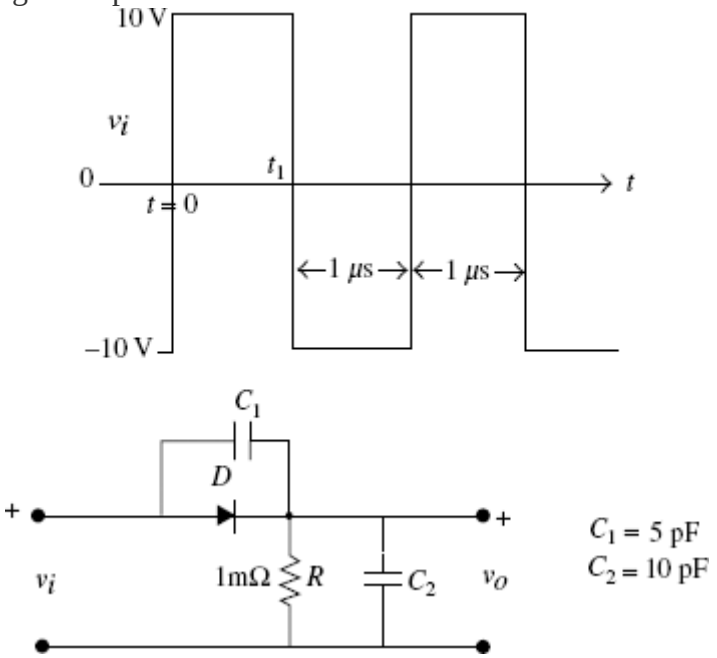


FIGURE 2p.7 Clipping circuit for problem 5

8. For the circuit shown in Fig. 2p.8, R_f = 100 Ω, R = 10 kΩ, V_γ = 0. Sketch the output waveform for the specified input.

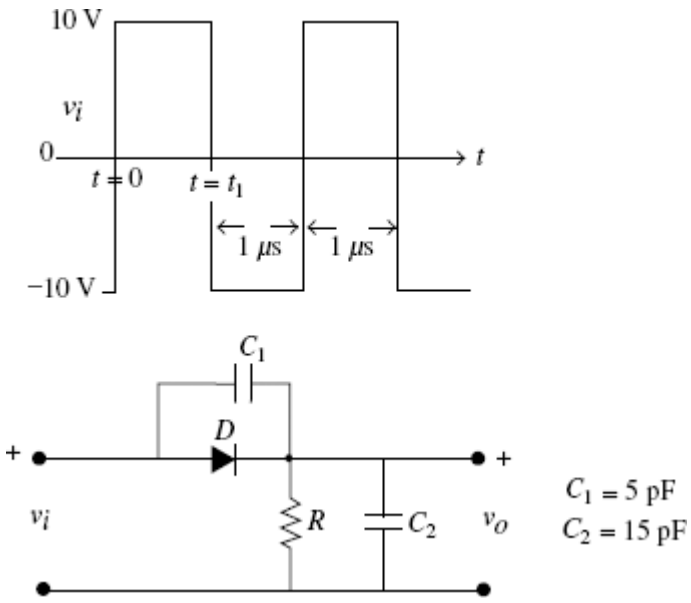


FIGURE 2p.8 The given clipping circuit with input.

PART-B: CLAMPING CIRCUITS SUMMARY

- The dc component that is blocked when a signal passes through a capacitive coupling network can again be restored using a clamping circuit.
- A clamping circuit, generally, is called a dc restorer and dc re-inserter, meaning that it reintroduces exactly the same amount of dc voltage lost. However, it is a dc inserter, which means that it introduces any desired dc voltage.
- A simple clamping circuit consists of a signal source, a capacitor of appropriate value and a diode connected across the output terminals.
- The positive or negative extremity of an input signal can be clamped to a zero level or to an arbitrarily chosen reference level by using a clamping circuit.
- The dc level associated with the input signal has absolutely no say in determining the steady-state response of the clamping circuit.
- The clamping circuit theorem states that for any input waveform under steady-state conditions $\boldsymbol{A_f/A_r = R_f/R}$.
- A synchronized clamping circuit is one in which the time of clamping is not determined by the signal but by a control signal which is in synchronization with the signal.

MULTIPLE CHOICE QUESTIONS

1. Strictly speaking, a clamping circuit should be called:

    1. dc restorer
    2. dc reinserter
    3. dc eliminator
    4. dc inserter

2. A positive clamping circuit is one that clamps:

    1. The positive extremity of the signal to the zero level
    2. The positive extremity of the signal to a positive dc voltage
    3. The negative extremity of the signal to the zero level
    4. None of the above

3. A negative clamping circuit is one that clamps:

    1. The positive extremity of the signal to the zero level
    2. The positive extremity of the signal to a positive dc voltage
    3. The negative extremity of the signal to the zero level
    4. None of the above

4. The clamping theorem states that:

    1. $\frac{A_f}{A_r} = \frac{R_f}{R}$
    2. $\frac{A_f}{A_r} = \frac{R}{R_f}$
    3. $\frac{A_f}{A_r} = \frac{R_r}{R_f}$
    4. $\frac{A_f}{A_r} = \frac{R_r}{R}$

5. In a clamping circuit, the tilts in the forward and reverse directions are related by:

    1. $\Delta f = \frac{R_f}{R_f + R_S} \times \frac{R + R_S}{R} \times \Delta r$
    2. $\Delta f = \frac{R_r}{R + R_S} \times \frac{R_f + R_S}{R} \times \Delta r$
    3. $\Delta f = \frac{R_f}{R} \times \Delta r$
    4. None of the above

SHORT ANSWER QUESTIONS

1. What is a clamping circuit?

2. Why do we call a clamping circuit a dc inserter?
3. What do you understand by positive clamping and negative clamping?
4. State the clamping circuit theorem.
5. What is synchronized clamping?
6. If $\Delta f = \frac{R_f}{R_f + R_S} \times \frac{R + R_S}{R} \times \Delta r$, show that $\Delta f = \Delta r$ when R_S is small
7. What do you understand by biased clamping?

LONG ANSWER QUESTIONS

1. A sinusoidal signal is applied as an input to a negative clamping circuit and suddenly the amplitude of the input signal falls. Explain how clamping is restored in the circuit?
2. State and prove the clamping circuit theorem.
3. Consider the steady-state output waveform of a clamping circuit for a square-wave input and derive the relation between the tilt in the forward direction to that in the reverse direction.
4. Explain the principle of synchronized clamping.
5. Discuss the influence of the diode characteristics on the clamping voltage.

SOLVED PROBLEMS

Example 1: The input in Fig. 2.9(a) is applied to the practical clamping circuit in Fig. 2.9(b). Compute the output till it reaches the steady-state. Given that f = 5 kHz, R_s = 0.1 kΩ, R_f = 0.1 kΩ, $R_r = \infty$.

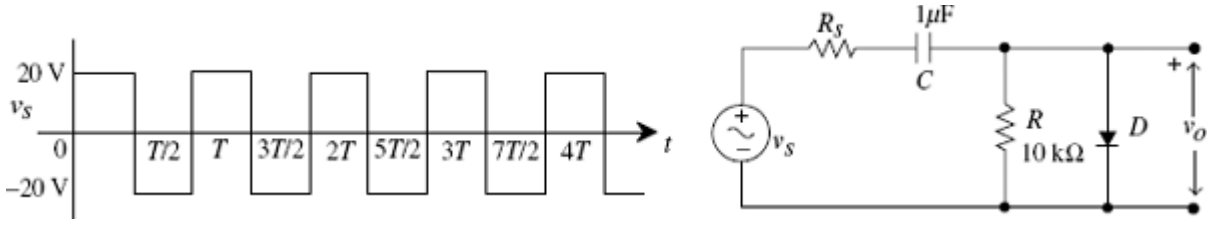


FIGURE 2.9(a) The Input, (b) the given practical clamping circuit

Solution: Assume that initially the capacitor is uncharged. The input to the circuit is a symmetric square wave whose amplitude varies from −20 V to 20 V. When the diode is conducting, using the circuit shown in Fig. 2.9(c), the output voltage can be calculated. Using Fig. 2.9(c):

$$v_o(0+) = 20\,\text{V} \times \frac{0.1\text{k}\Omega}{0.1\text{k}\Omega + 0.1\text{k}\Omega} = 10\,\text{V}$$

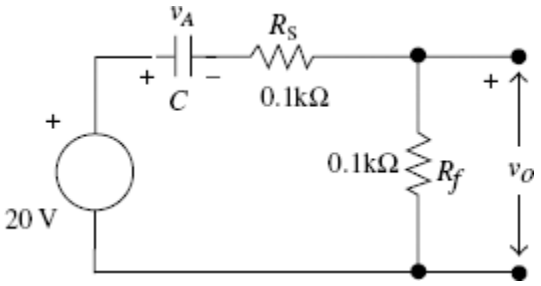


FIGURE 2.9(c) The circuit to calculate the output when ***D*** is ON

When the input abruptly changes by 20 V, the output also jumps by 10 V. As the input is constant during the period 0 to $T/2$, the output decays exponentially with time constant τ.

$\tau = (R_f + R_S)C = 0.2 \times 10^3 \times 1 \times 10^{-6} = 0.2$ ms

As

$f = 5$ kHz, $\quad T = \frac{1}{f} = 0.2$ ms $\quad T/2 = 0.1$ ms, $T = \tau$

Hence,

$$v_o\left(\frac{T}{2}\right) = 10\,e^{-T/2\tau} = 10\,e^{-1/2} = 6\,\text{V}$$

Using Fig. 2.9(d), we can calculate the voltage v_A across C. The voltage across capacitor v_A is:

$v_A = 20\text{ V} - (6\text{ V} + 6\text{ V}) = 8\text{ V}$

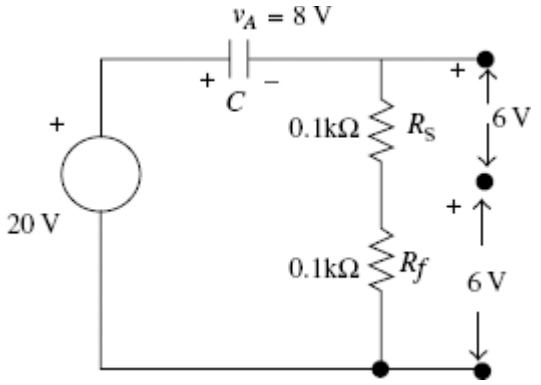


FIGURE 2.9(d) Circuit to calculate v_A

At $t = T/2$, the input falls to −20 V, the diode is in the OFF state and the equivalent circuit of Fig. 2.9(e) is used.

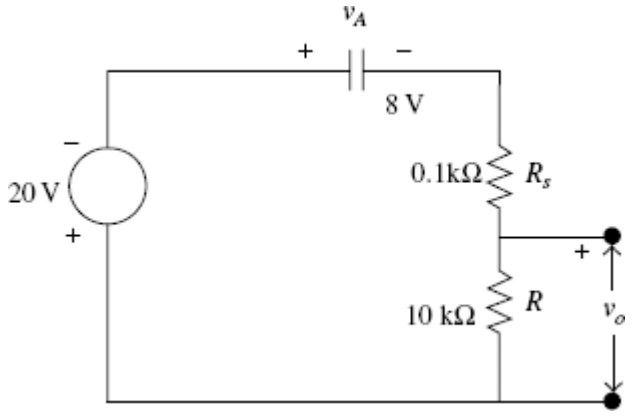


FIGURE 2.9(e) Circuit to calculate the output when D is OFF

As $R >> R_S$, the drop across R_S is negligible. This circuit is redrawn as shown in Fig. 2.9(f).

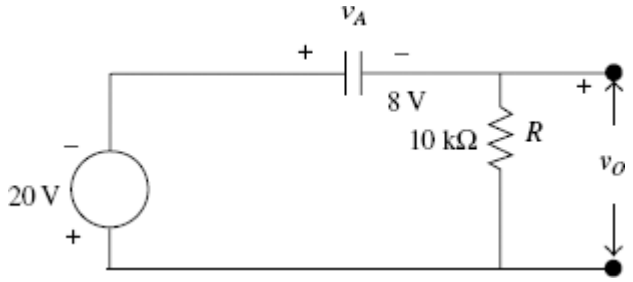


FIGURE 2.9(f) The simplified circuit to calculate the output voltage v_o

$\therefore v_o = -20\text{ V} - 8\text{ V} = -28\text{ V}$

The output falls to −28 V suddenly. As the input remains constant from $T/2$ to T, the output decays with time constant $\tau' = 10.1\ \text{k}\Omega \times 1\mu\text{F} = 10.1$ ms. Thus, $T/2$ is 0.1 ms and $\tau' = 10.1$ ms, which implies that $T/2 << \tau$. Hence, there is no appreciable decay of the output when,

$$v_o(T) = -28\, e^{-T/\tau'} \approx -28\text{ V}$$

In other words, the output remains constant. In the interval $T/2$ to T, as the output remains constant, the voltage across the capacitor remains unchanged. At $t = T$, the input abruptly rises to 20 V. At that instant, D is ON, as the voltage across C is 8 V, $v_o = 6$ V and in the interval T to $3T/2$ the output voltage decays exponentially.

$$v_o\left(\frac{3T}{2}\right) = 6\, e^{-1/2} = 3.6\text{ V}$$

Voltage across $C = v_A = 20 - (3.6 + 3.6) = 12.8$ V and at $t = 3T/2$, $v_o = -20\text{ V} - 12.8\text{ V} = -32.8$ V

As the voltage does not change much during the interval $3T/2$ to $2T$, at $t = 2T$, the output again returns to 3.6 V.

At $t = 5T/2$

$$v_o = 3.6\, e^{-1/2} = 2.2\text{ V}$$

$\therefore v_A = 20 - (2.2 + 2.2) = 15.6$ V

$v_o = -20$ V $- 15.6$ V $= -35.6$ V

The output remains at -35.6 V during the interval $5T/2$ to $3T$. This again returns to 2.2 V at $t = 3T$ and decays during the interval $3T$ to $7T/2$.

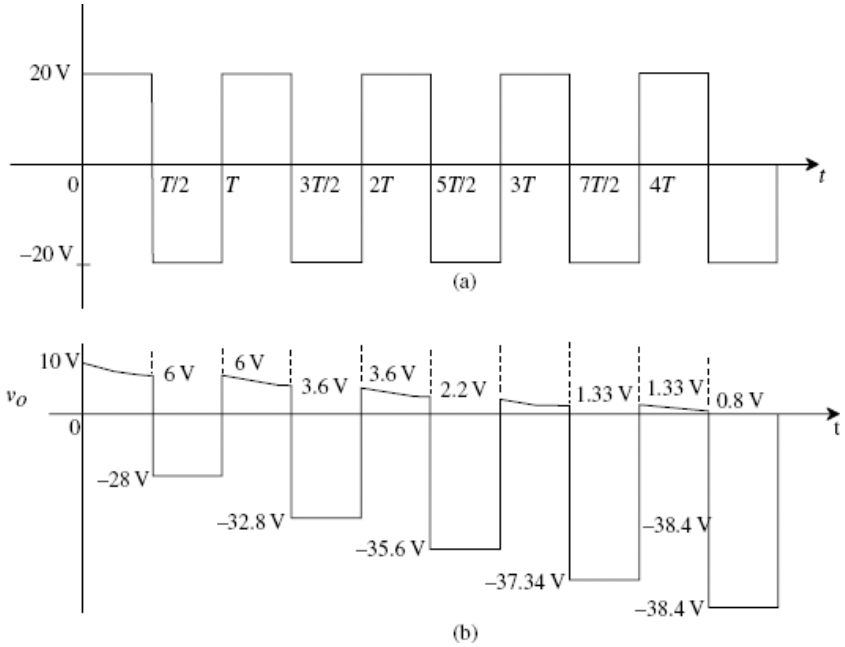


FIGURE 2.10(a) The given waveforms; (b) the output waveforms

$v_O\left(\frac{7T}{2}\right) = 2.2\,e^{-1/2} = 1.33$ V $\quad v_A = 20 - (1.33 + 1.33) = 20 - 2.66 = 17.34$ V

$v_o = -20$ V $- 17.34$ V $= -37.34$ V

This procedure is repeated. It is seen that the output reaches the steady state in a few cycles, wherein the positive peaks of the input are clamped to a zero level (strictly speaking, to V_γ) at the output (see Fig. 2.10).

Example 2: For the clamping circuit shown in Fig. 2.11(a) from the given input, calculate and plot the steady-state output. Given $C = 0.1\,\mu$F, R = 100 kΩ, $V_R = 5$ V, $f = 5000$ Hz.

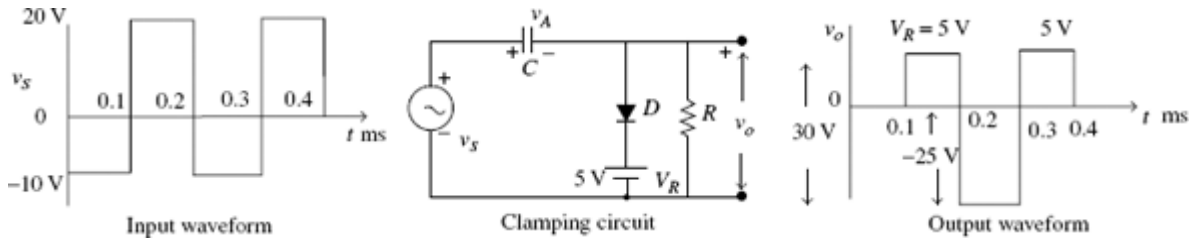


FIGURE Fig. 2.11(a) The given biased clamping circuit with input and output waveforms

Solution: Given $f = 5000$ Hz. Therefore, $T = \frac{1}{5000} = 0.2$ ms.

$\frac{T}{2}$ = 0.1 ms, $\tau = RC = 100 \times 10^3 \times 0.1 \times 10^{-6} = 10$ ms.

$\tau >> T/2$, hence the voltage on C remains unchanged during the period D is OFF.

Step 1: During the interval 0 to 0.1ms, as v_s is -10 V D is OFF and $v_o = 0$.

Step 2: During the interval 0.1 to 0.2 ms, v_s is 20 V, hence D is ON. The circuit of Fig. 2.11(a)) is drawn as shown in Fig. 2.11(b) , v_o = 5 V

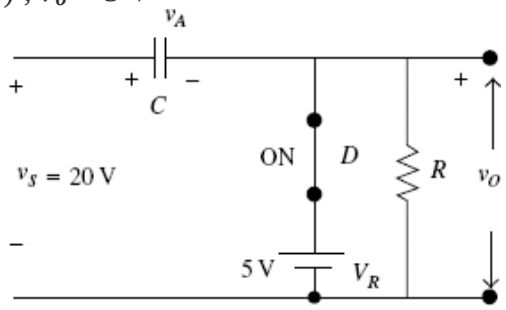


FIGURE 2.11(b) The circuit when D is ON during 0.1 to 0.2 ms

Step 3: Now applying the KVL equation around the input loop, we have: $v_A = v_s - V_R = 20-5 = 15$ V. The assumption is that v_A remains unchanged.

Step 4: During 0.2 to 0.3 ms, D is OFF. v_A = 15 V, v_s = −10 V. The circuit is as shown in Fig. 2.11(c).

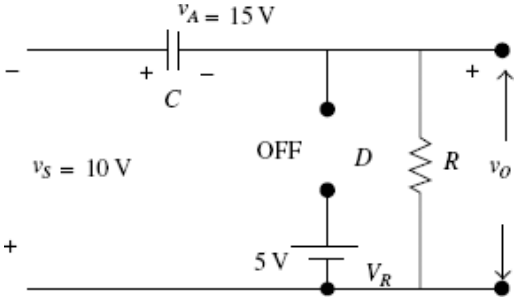
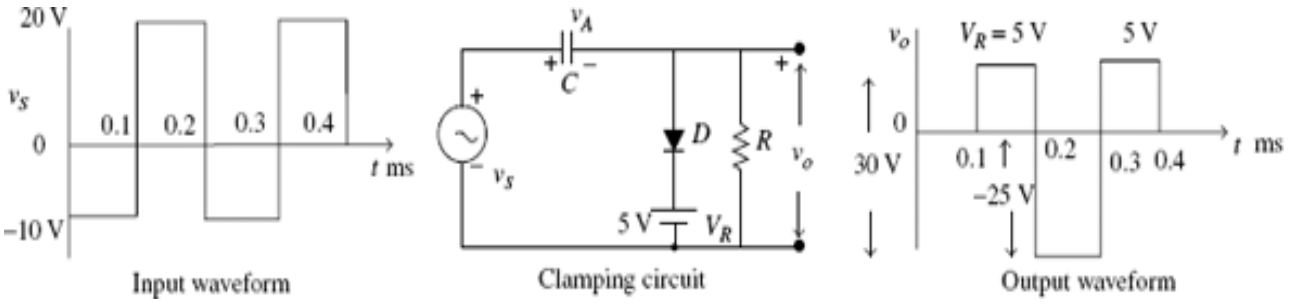


FIGURE 2.11(c) The circuit during 0.2 and 0.3 ms when D is OFF

Thus: $v_o = -v_s - v_A = -10 - 15 = -25$ V.

The output waveform is plotted as shown in Fig. 2.11(a).



The positive peak of the input is clamped to +5 V. The peak-to-peak swing at the input is 30 V. It remains the same in the output.

Example 3: Working with the same circuit and inputs, repeat Example 2.2, using a Si diode with V_{AK} = 0.7 V, when ***D*** is ON.

Solution:

Step 1: During the interval 0 to 0.1ms, as v_s is −10 V, ***D*** is OFF and v_o = 0.

Step 2: During the interval 0.1 to 0.2 ms, v_s is 20 V, hence ***D*** is ON. The circuit of Fig. 2.11(a) is drawn as shown in Fig. 2.11(d). v_o = 5.7 V

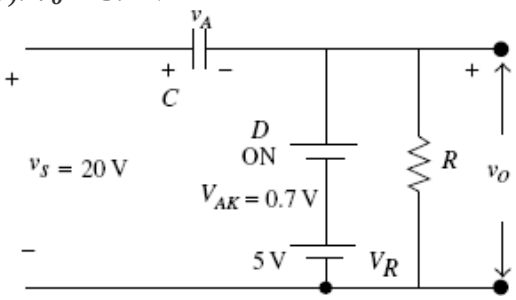


FIGURE 2.11(d) Circuit when ***D*** is ON during 0.1 to 0.2 ms

Step 3: Now applying the KVL equation around the input loop, we have:

$v_A = v_s - V_R - V_{AK} = 20 - 5 - 0.7 = 14.3$ V

Step 4: During 0.2 to 0.3 ms, ***D*** is OFF, v_A = 14.3 V, v_s = −10 V. The circuit is shown in Fig. 2.11(e). . Thus:

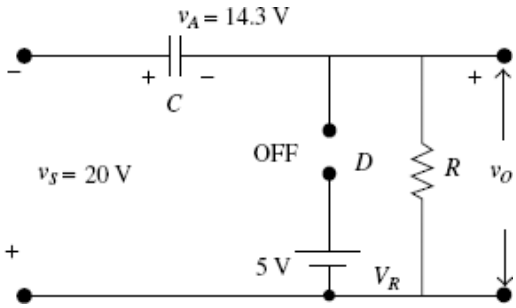


FIGURE 2.11(e) The circuit during 0.2 and 0.3 ms when ***D*** is OFF

$v_o = -v_s - v_A = -10 - 14.3 = -24.3$ V.

The output waveform is plotted in Fig. 2.11(f). .

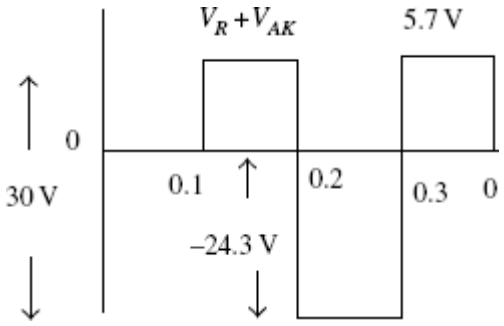


FIGURE 2.11(f) The output waveform

The positive peak of the input is clamped to +5.7 V. The peak-to-peak swing at the input is 30 V. It remains the same in the output also.

Example 4: Draw the steady-state output waveform for the given biased clamping circuit shown in Fig. 2.12, when the input is a square-wave signal of amplitude ±10 V. Assume that C is large.

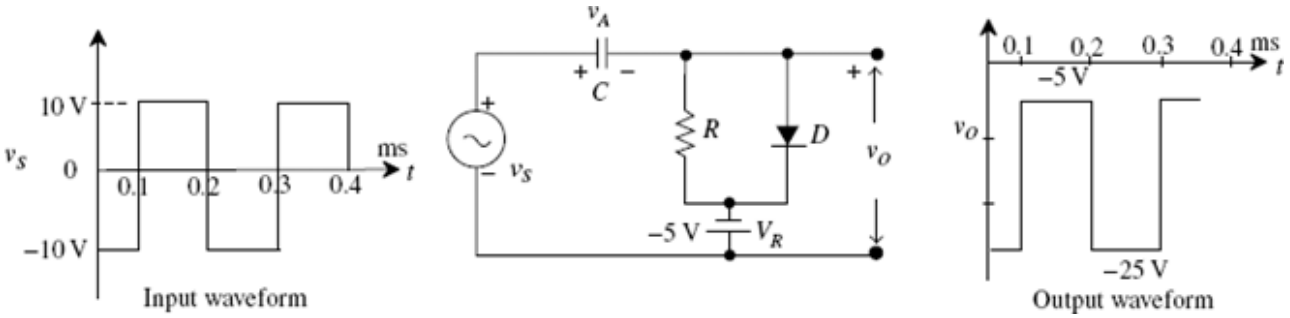


FIGURE 2.12 The given biased negative clamper with $V_R = -5$ V

Solution: The diode D conducts, when the input changes to +10 V, $V_o = -5$ V Then the capacitor charges to $(v_s - v_o) = 15$ V.

Under steady-state conditions $v_o = v_s - v_A = v_s - 15$ V

When $v_s = 10$ V, $v_o = 10 - 15 = -5$ V

When $v_s = -10$ V, $v_o = -10 - 15 = -25$ V

The positive peak is clamped to $V_R = -5$ V, in the output, as shown in Fig. 2.12.

Example 5: Draw the steady-state output waveform for the given biased clamping circuit shown in Fig. 2.13, when the input is ± 10 V square wave. Assume that C is large.

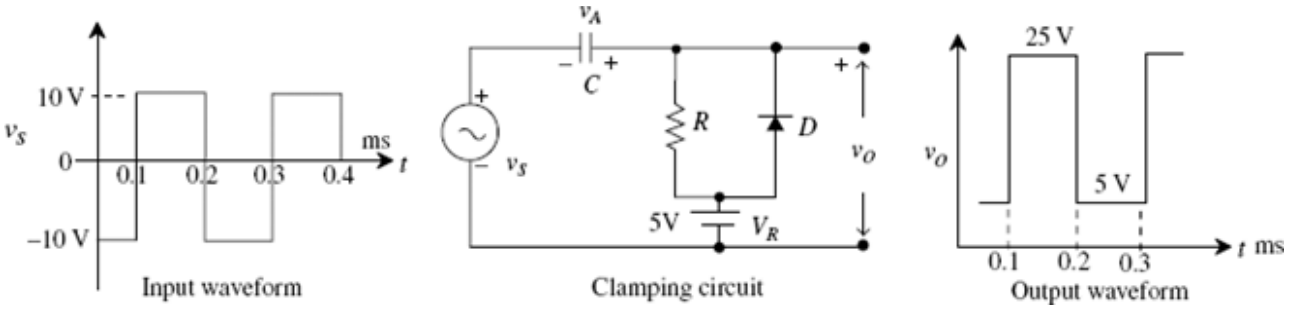


FIGURE 2.13 The given biased positive clamper with $V_R = 5$ V

Solution: The diode D conducts, when v_s changes to −10 V, then the capacitor charges to $v_A = -15$ V.

Under steady-state conditions $v_o = v_s - (-v_A) = v_s + v_A = v_s + 15$ V

When $v_s = 10$ V, $v_o = 10 + 15 = 25$ V

When $v_s = -10$ V, $v_o = -10 + 15 = 5$ V

The negative peak is clamped to V_R = 5 V in the output, Fig. 2.13.

Example 6: Draw the steady state output waveform for the given biased clamping circuit shown in Fig. 2.14, when the input is ± 10 V square wave. Assume that C is large.

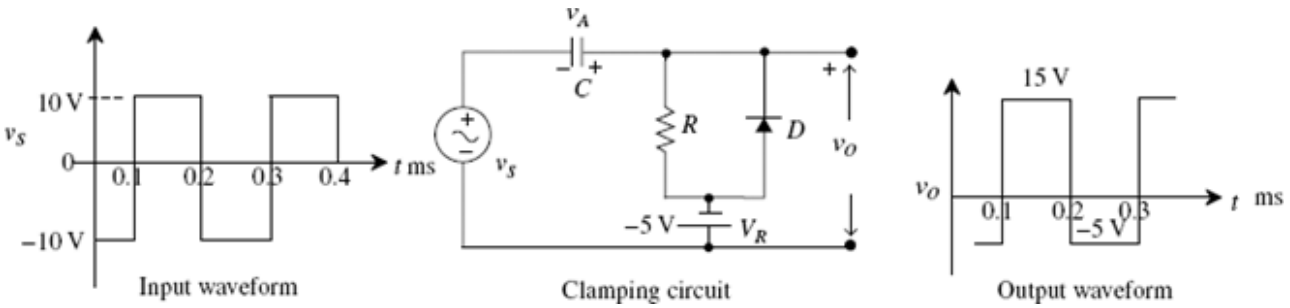


FIGURE 2.14 The given biased positive clamper with $V_R = -5$ V

Solution: The diode D conducts, when v_s changes to −10 V. Then the capacitor charges to $v_A = v_S - V_R = -10 - (-V_R) = -5$ V.

Under steady-state conditions, $v_o = v_s - (-v_A) = v_s + v_A = v_s + 5$ V.

When v_s = 10 V, v_o = 10 + 5 = 15 V.

When $v_s = -10$ V, $v_o = -10 + 5 = -5$ V.

The negative peak is clamped to $V_R = -5$ V in the output, as shown in Fig. 2.14.

Example 7: Design a clamping circuit to clamp the negative peaks to 5 V given that R_f = 0.1 kΩ, R_r = 1000 kΩ, V_{R1} = 5 V, f = 2 kHz and k = 10, V_D = 0.7 V.

Solution: Using the relation:

$$R = \sqrt{R_f R_r} = \sqrt{0.1 \times 1000} = 10\,\text{k}\Omega$$

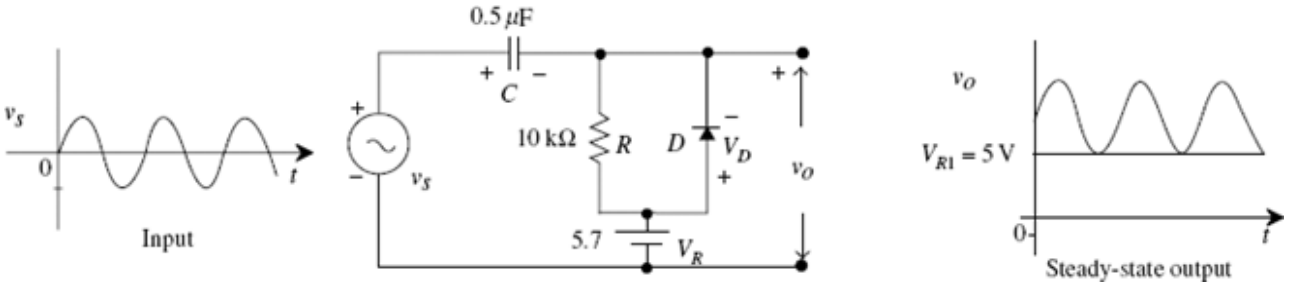


FIGURE 2.15 The given biased positive clamping circuit and the steady-state output

Using:

$$C = \frac{10T}{R} = \frac{10 \times 0.5 \times 10^{-3}}{10 \times 10^{3}} = 0.5\,\mu\text{F}$$

As the negative peak is required to be clamped to +5 V, the reference voltage source is chosen using as:

$V_R = V_{R1} + V_D = 5 + 0.7 = 5.7$ V

The circuit with input and output waveforms is shown in Fig.2.15.

Example 8: The input shown in Fig. 2.16(a) is applied to the clamping circuit [see Fig. 2.16(b)]. Plot the output waveform. Given that $R_s = R_f = 50\ \Omega$, $R = 10$ kΩ, $R_r = \infty$, C = 1μF

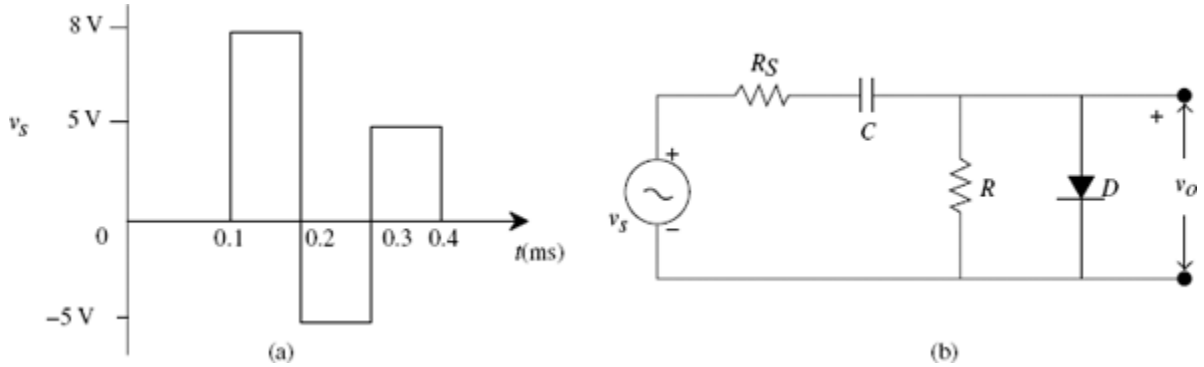


FIGURE 2.16(a) The given Input; and (b) the given clamping circuit

Solution: The equivalent circuit, when the diode conducts, is shown in Fig. 2.17(a). When the diode does not conduct, the equivalent circuit is as shown in Fig. 2.17(b).

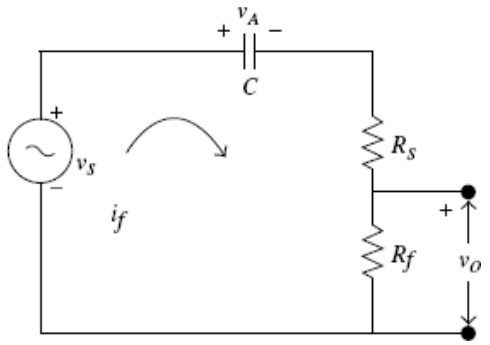


FIGURE 2.17(a) The equivalent circuit when ***D*** is ON

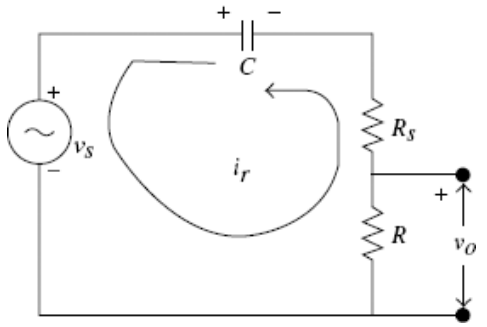


FIGURE 2.17(b) The equivalent circuit when ***D*** is OFF

1. At t = 0.1 ms, v_s abruptly rises to 8 V. As the capacitor cannot allow sudden changes in the voltage it behaves as a short circuit.

$$v_O = \frac{8 \times 50}{100} = 4\,\text{V}$$

2. The input remains constant at 8 V from 0.1 to 0.2 ms. So $\boldsymbol{v_o}$ decays exponentially with time constant $(\boldsymbol{R_s} + \boldsymbol{R_f})\,\boldsymbol{C}$.

   At $\boldsymbol{t}$ = 0.2 ms

   $\boldsymbol{v_o} = 4\,\boldsymbol{e}^{-0.1\times10-3/(50+50)(1\times10-6)} = 4\boldsymbol{e}^{-1} = 1.47152$ V

   Voltage across the capacitor = $\boldsymbol{v_A} = 8 - 2 \times 1.47152 = 5.05696$ V

3. At $\boldsymbol{t}$ = 0.2 ms, $\boldsymbol{v_s}$ abruptly falls to −5 V. The resultant circuit is as shown in Fig. 2.17(c).

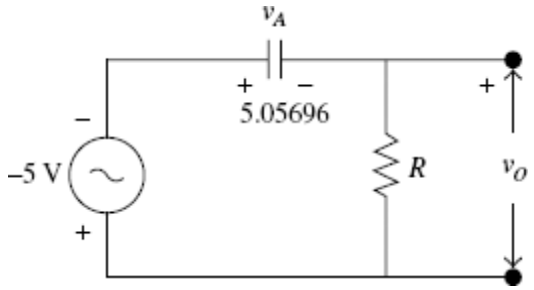


FIGURE 2.17(c) The circuit to calculate the output

$\boldsymbol{v_o} = -5 - 5.05696 = -10.05696$ V

4. From $\boldsymbol{t}$ = 0.2 ms to 0.3 ms, $\boldsymbol{v_s}$ remains at −5 V. Hence, the output voltage should decay exponentially with a time constant $(\boldsymbol{R} + \boldsymbol{R_s})\,\boldsymbol{C}$.

   At 0.3 ms,

   $\boldsymbol{v_o} = -10.05696\,\boldsymbol{e}^{-0.1\times10-3/(10000+50)(1\times10-6)} = -9.958$ V

   Voltage across $\boldsymbol{C} = \boldsymbol{v_A} = -5 + 9.958 = 4.958$ V

5. At $\boldsymbol{t}$ = 0.3 ms and $\boldsymbol{v_s}$ = 5 V. The equivalent circuit to be considered is shown in Fig. 2.17(d).

$$v_O = \frac{5 - 4.958}{2} = 0.0213\,\text{V}$$

As $\boldsymbol{v_s}$ remains constant, $\boldsymbol{v_o}$ decays exponentially from $\boldsymbol{t}$ = 0.3 ms to 0.4 ms.

At $\boldsymbol{t}$ = 0.4 ms $\boldsymbol{v_o} = 0.0213\,\boldsymbol{e}^{-1} \approx 0$ V. The output voltage now varies as shown in Fig. 5.34(e).

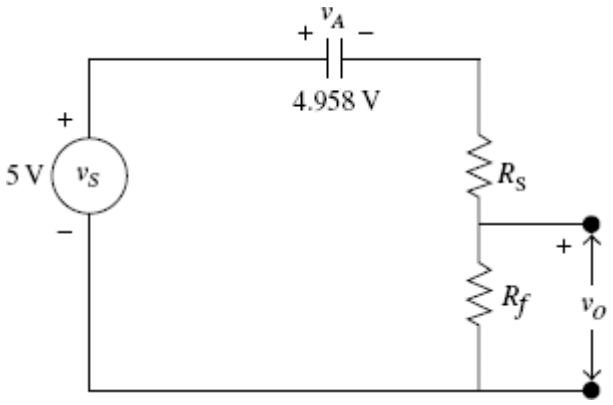


FIGURE 2.17(d) The circuit to calculate the output

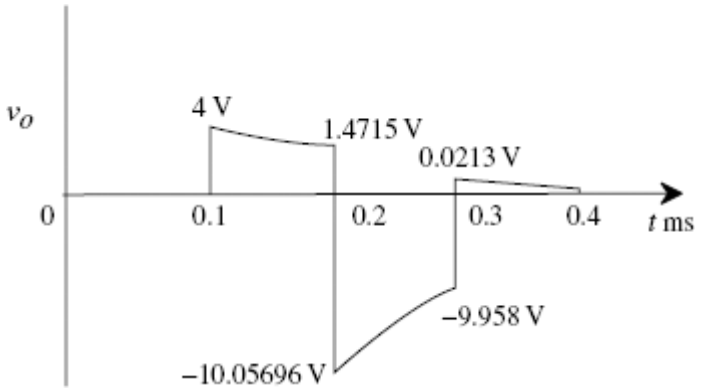


FIGURE 2.17(e) The steady-state output waveform

Example 9: A clamping circuit and the input applied to it are shown in Fig. 2.18(a) and (b). Calculate and plot to scale the steady-state output. Given that: $R_s = R_f = 100\ \Omega$, $T_1 = T_2 = 500\ \mu s$.

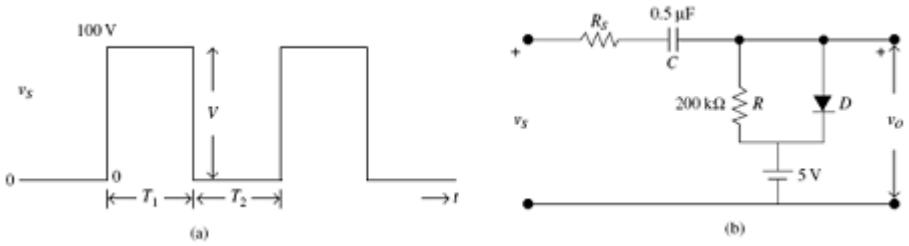


FIGURE 2.18(a) The given input; and (b) clamping circuit

Solution: To calculate the steady-state voltages, first calculate V_1, V_1', V_2 and V_2' by making $V_R = 0$. During the interval 0 to T_1, the charging time constant of the capacitor C is:

$\tau_f = (R_s + R_f)\,C = (100 + 100)0.5 \times 10^{-6} = 100\ \mu s$

The capacitor discharges during the interval T_1 to T_2 and the time constant, τ_r, is:

$\tau_r = (R_s + R)C = (100 + 200000)0.5 \times 10^{-6} = 100050\ \mu s = 100.050$ ms

$$V_1' = V_1\, e^{-T_1/\tau_f} = V_1\, e^{-500/100} = 0.00674\, V_1$$

$$V_1' = 0.00674 V_1 \qquad (1)$$

$$V_2' = V_2\, e^{-T_2/\tau_r} = V_2\, e^{-500/100050} = 0.995 V_2$$

$$V_2' = 0.995 V_2 \qquad (2)$$

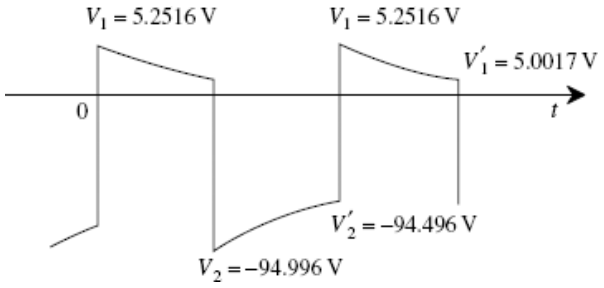


FIGURE 2.18(c) The steady-state output

$$V = \frac{R_f + R_s}{R_f} V_1 - \frac{R + R_s}{R} V_2' = \frac{100 + 100}{100} \times V_1 - \frac{200\ \text{k}\Omega + 100}{200\ \text{k}\Omega} \times V_2'$$

$$100 = 2V_1 - V_2' \qquad \textbf{(3)}$$

Also,

$$V = \frac{R_f + R_s}{R_f} V_1' - \frac{R + R_s}{R} V_2$$

$$100 = 2V_1' - V_2 \qquad \textbf{(4)}$$

Solving Eqs. (1), (2), (3) and (4):

$\boldsymbol{V}_1 = 0.2516$ V, $V_1' = 0.0017$ V $\boldsymbol{V}_2 = -99.996$ V $V_2' = -99.496$ V

To get the steady-state output, we add $\boldsymbol{V_R}$ to the values of $\boldsymbol{V}_1$, V_1', $\boldsymbol{V}_2$ and V_2' for the given circuit in Fig. 2.18(a. Therefore,

$\boldsymbol{V}_1 = 5.2516$ V $V_1' = 5.0017$ V $\boldsymbol{V}_2 = -94.996$ V $V_2' = -94.496$ V.

The steady-state output is as shown in Fig. 2.18(c).

Example 10: Draw the output waveform under the steady state for the given biased clamping circuit shown in Fig. 2.19, when the input is 10 V square wave. Assume that ***C*** is very large so that the change in the output voltages during the periods when ***D*** is ON and OFF is negligible.

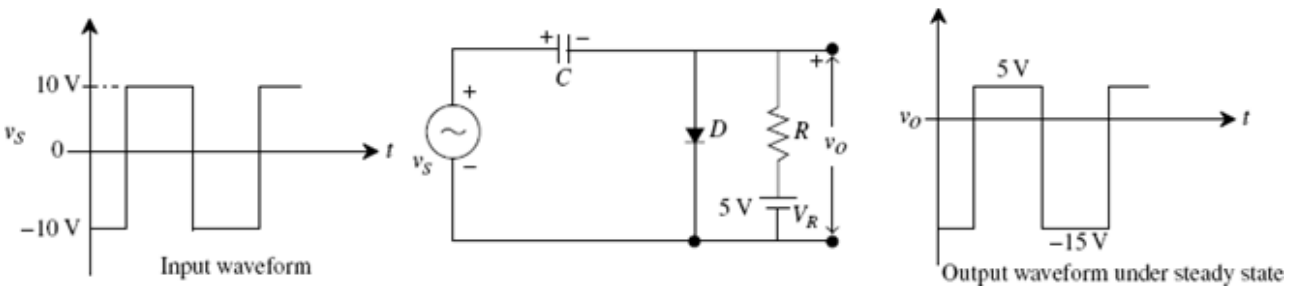


FIGURE 2.19 The given biased negative clamper with $\boldsymbol{V_R} = 5$ V and the corresponding input and output waveforms

Solution: The diode D conducts when the input changes to +10 V. Then capacitor charges to +5 V after few cycles.

Under steady-state conditions $v_o = v_s - v_A = v_s - 5$

When $v_s = 10$ V, $v_o = 10 - 5 = 5$ V

When $v_s = -10$ V, $v_o = -10 - 5 = -15$ V

The positive peak is clamped to V_R(= 5V), in the output.

UNSOLVED PROBLEMS

1. Design a diode clamper shown in Fig. 2p.1 to restore the positive peaks of the input signal to a voltage level to 5 V. Assume the diode cut-in voltage is 0.5 V, f = 1 kHz, R_f = 1 kΩ, R_r = 200 kΩ and RC = 20 T.

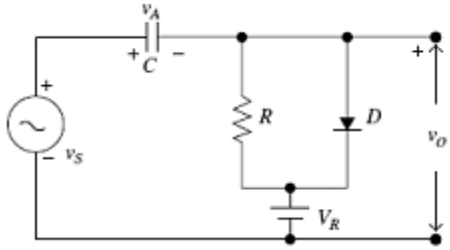


FIGURE 2p.1 The given clamping circuit with reference voltage V_R

2. For the excitation as shown in Fig. 2p.2(a) and the clamping circuit [see Fig. 2p.2(b)], calculate and plot to scale, the steady-state output.

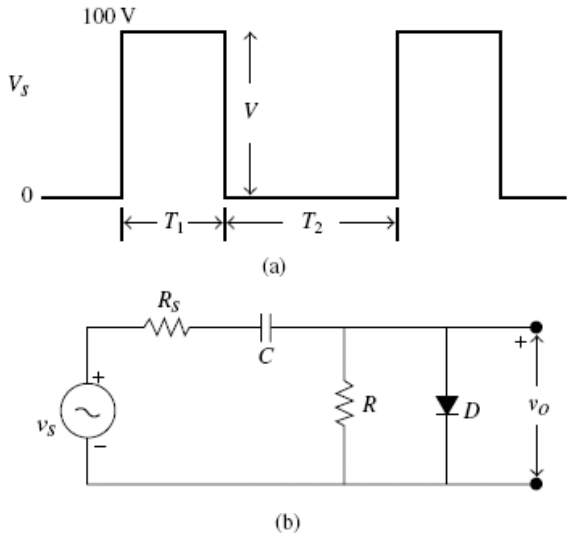


FIGURE 5p.2 The given Input, and (b) the clamping circuit

3. Sketch the steady-state output voltage for the clamper circuit shown in Fig. 2p.3 and locate the output dc level and the zero level. The diode used has R_f = 100 Ω, R_r = 500 kΩ, V_γ = 0.C is arbitrarily large and R = 20 kΩ. The input is a ±20V square wave with 50 per cent duty cycle.

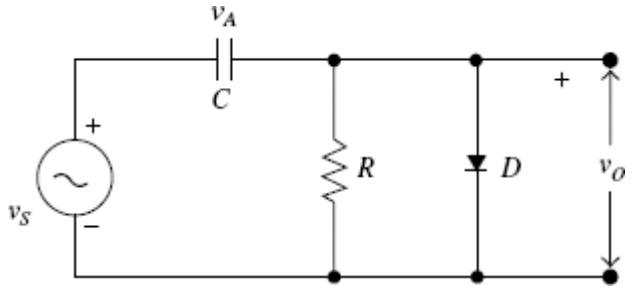


FIGURE 2p.3 The given clamping circuit for problem 2

4. For the circuit shown in Fig. 2p. 4(a), $\boldsymbol{R_s} = \boldsymbol{R_f} = 50\ \Omega$, $\boldsymbol{R} = 10\ \text{k}\Omega$, $\boldsymbol{R_r} = \infty$, $\boldsymbol{C} = 2.0\ \mu\text{F}$, the input varies as shown in Fig. 2p.4(b). Plot the output waveform.

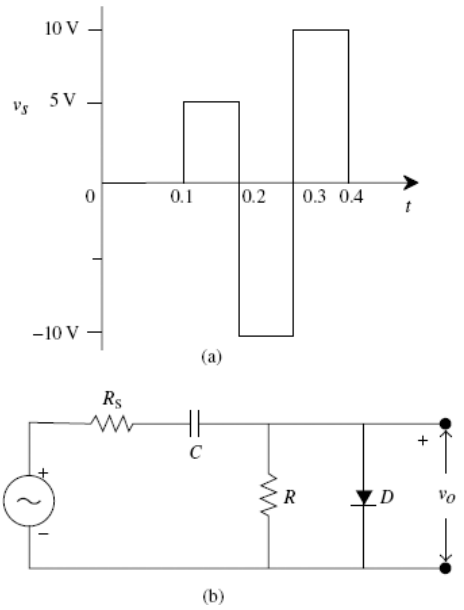


FIGURE 2p.4 The given input; and (b) the given clamping circuit

5. The input as shown in Fig. 2p.5(a), is applied to the clamping circuit shown in Fig. 2p.5(b), with $\boldsymbol{R_s} = \boldsymbol{R_f} = 100\ \Omega$, $\boldsymbol{R} = 10\ \text{k}\Omega$, $\boldsymbol{R_r} = \infty$, $\boldsymbol{C} = 1.0\ \mu\text{F}$; $\boldsymbol{V_\gamma} = 0$. Draw the output waveform and label all the voltages.

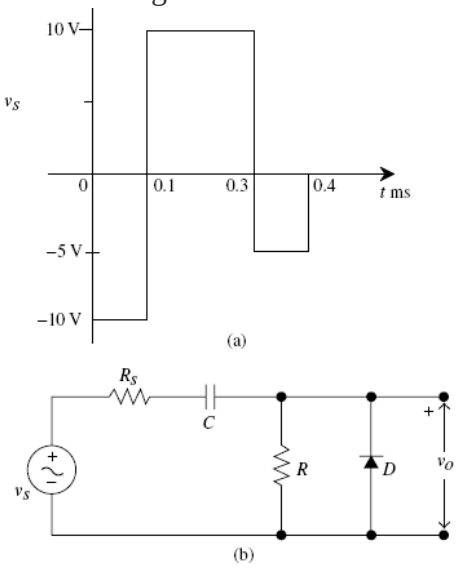


FIGURE 2p.5 The given input; and (b) the given clamping circuit

6. A clamping circuit and input applied to it are shown in Fig. 2p.6. Assume that C is quite large. Find at which voltage level the positive peak is clamped in the output if T_1 = 1 ms, T_2 = 1μs, R_f = 100 Ω and R = 100 kΩ.

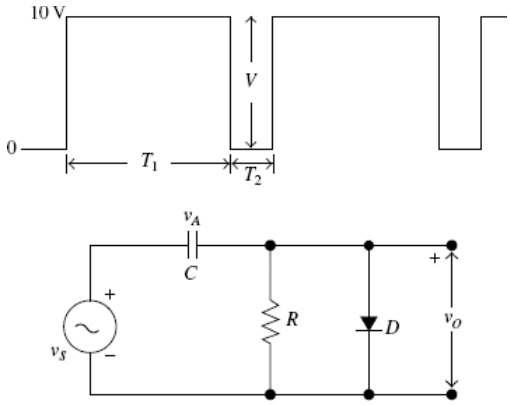


FIGURE 2p.6 The given input and clamping circuit for problem 3

(Hint: Use the clamping Theorem.)

7. Calculate and draw the steady-state output waveform of the circuit in Fig. 2p.7. Assume R_f = 50 Ω, R_r = 500 kΩ and T_1 = T_2 = 1 ms.

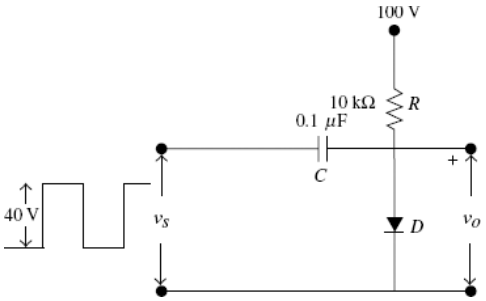


FIGURE 2p.7 The given clamping circuit with large

8. Design a biased clamping circuit to derive the output voltage as shown in Fig. 2p.8(b), given the input as shown in Fig. 2p.8(a) f = 1000 Hz, R_f = 100 Ω, R_r = 1MΩ and RC/T = 10. Assume that D is ideal.

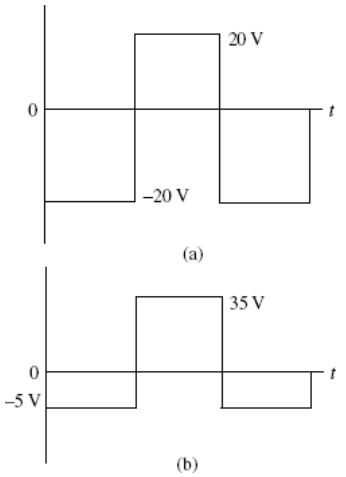


FIGURE 2p.8 (a) The given input to the clamping circuit; and (b) the required output