UNIT – II

Non Linear Wave Shaping

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Diode clippers, Transistor clippers, clipping at two independent levels, Transfer characteristics of clippers, Emitter coupled clipper, Comparators, applications of voltage comparators, clamping operation, clamping circuits using diode with different inputs, Clamping circuit theorem, practical clamping circuits, effect of diode characteristics on clamping voltage, Transfer characteristics of clampers.

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The previous chapter discussed about linear wave shaping and how a change of wave shape was brought about when a non-sinusoidal signal is transmitted through a linear network like *RC* low pass and high pass circuit. This chapter, discuss some aspects of nonlinear wave shaping like clipping and clamping. The circuits for which the outputs are non-sinusoidal for sinusoidal inputs are called nonlinear wave shaping circuits, for example clipping circuits and clamping circuits. Nonlinear wave shaping circuits may be classified as clipping circuits and clamping circuits. Clipping circuits may be single level clippers or two level clippers.

Clipping means cutting and removing a part. ***A clipping circuit is a circuit which removes the undesired part of the waveform and transmits only the desired part of the signal which is above or below some particular reference level, i.e. it is used to select for transmission that part of an arbitrary waveform which lies above or below some particular reference voltage or current level.*** Clipping circuits are also called *voltage* (or current) *limiters, amplitude selectors* or *slicers.*

Single level clippers may be series diode clippers with and without reference or shunt diode clippers with and without reference. Clipping circuits may use diodes or transistors.

Diodes, transistors and field-effect transistors (FETs) can be used as linear circuit elements if the operation is restricted to that limited region in the characteristic in which it can be approximated to a straight-line characteristic (small-signal conditions). However, when the input is increased further (under large-signal conditions), these devices no longer behave as linear circuit elements and the operation can go into the nonlinear region of the characteristic. ***When non-linear circuit elements are used in wave shaping applications, the resultant process is termed as non-linear wave shaping.*** Hence ***a non-linear network consists of a combination of both linear and non-linear elements i.e. resistors, capacitors, inductors, diodes and active devices like transistors etc.***

In communication systems, sometimes it becomes necessary to eliminate a portion of the input signal, either at a single level or at two independent levels. The circuits that accomplish this task are called clipping circuits. These circuits can also be used to eliminate the noise associated with an input signal. Such clipping circuits are called noise clippers. The parameters of these devices can change with variations in temperature. Thus, in applications

where precision is required, it becomes necessary to provide temperature compensation so that temperature variations do not influence the performance of the circuit.

Amplitude comparators (also called comparators) are circuits that compare an input with a reference signal and deliver a high output the moment the input reaches the reference level. A simple diode comparator circuit is discussed and possible techniques to improve the sharpness of the break region are presented in this chapter. A comparator circuit may be used to control other circuits with the help of its output; the instant the input reaches a predefined reference level.

Clamping circuits may be (a) negative clampers or positive peak clampers with and without reference and (b) positive clampers or negative peak clampers with and without reference.

When a signal is transmitted through a capacitive coupled network, the dc component associated with the input is lost in the output since the capacitor blocks the dc. If the dc component needs to be restored, a clamping circuit is used. Thus, ***clamping circuits reintroduce or reinsert or restore the dc component lost during transmission through a capacitive coupled network and hence are called either dc restorers or dc re-inserters.*** The output reaches the steady-state value in a few cycles after the application of the input to the clamping circuit (transient period). ***Circuits that clamp the positive peak of the signal to the zero level are called negative clampers and those that clamp the negative peak of the signal to the zero level are called positive clampers.*** In general, the output can be referenced to any arbitrarily chosen reference voltage. Circuits that clamp the output to zero or to any dc level are considered here. The necessary relations that enable us to plot the steady-state responses are then derived. The effect of the internal resistance of the source on the output and the influence of diode characteristics on the clamping voltage are also examined. In some applications, clamping is needed only for a finite duration and the time interval for which this is to be accomplished is determined by an external signal called the control signal. The circuit that performs this operation, called synchronized clamping circuit, is also discussed.

Learning Objectives:

After reading this chapter, you will be able to:

1. Describe various clamping circuits
2. Derive the necessary relations to plot steady-state output
3. Describe the effect of diode characteristics on the clamping voltage
4. Describe synchronized clamping
5. State and derive the clamping circuit theorem

2.1 Clipping Circuits:

Clipping circuits select that part of the signal which lies above and below a reference level. Depending on whether the diode is connected in series with the load or in shunt with the load, these circuits are called either series-clipping circuits or shunt-clipping circuits.

In general, there are three basic configurations of clipping circuits.

1. A series combination of a diode, a resistor and a reference voltage.

2. A network consisting of many diodes, resistors and reference voltages.

3. Two emitter coupled transistors operating as a differential amplifier.

2.2 Diode Clippers:

Figure 2 (a) shows the *v-i* characteristic of a practical diode. Figures 2 (b), (c), (d), and (e) Show the *v-i* characteristics of an idealized diode approximated by a curve which is piece-wise linear and continuous. The break point occurs at V_r , where V_r = 0.2 V for Ge and V_r = 0.6 V for Si. Usually V_r is very small compared to the reference voltage V_R and can be neglected.

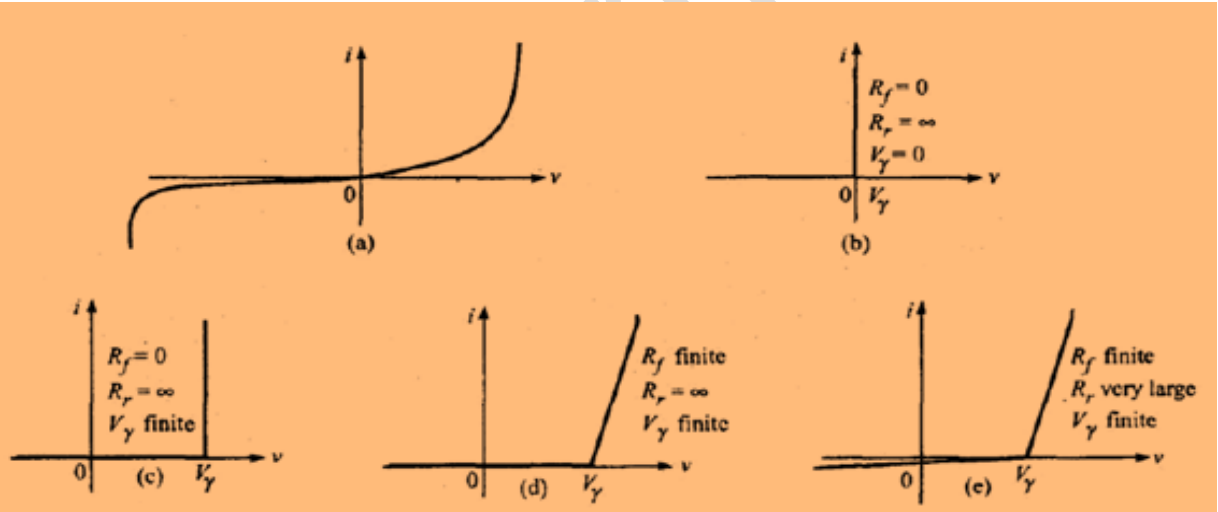


Figure 2 *v-i* Characteristics of a diode

2.3 Series Clippers:

Consider the series-clipping circuit shown in Figure 2.1(a) and its transfer characteristic (a plot that gives the relationship between the input and the output voltages) with input and output waveforms in Figure 2.1(b).

- When $v_i \geq 0$ is positive, D conducts and the input signal is transmitted to the output and is given by $v_O = v_i \frac{R}{R_f + R} \approx v_i \frac{R}{R} = v_i$. Here $R_f << R$. R_f is the diode forward resistance.
- When $v_i < 0$ is negative, D reverse biased and the output is given by $v_O = v_i \frac{R}{R_r + R} \approx 0$. Here $R_r >> R$. R_r is the diode reverse resistance.
- When $v_i \geq 0$ is positive, D conducts, $v_O = v_i \frac{R}{R_f + R} \approx v_i \frac{R}{R} = v_i$, slope = 1- (a)
- When $v_i < 0$ is negative, D reverse biased, $v_O = v_i \frac{R}{R_r + R} \approx 0$, slope = 0-----(b)
- The above equations (a) and (b) are known as the Transfer characteristic equations.
- Eq. (b) shows there is no transmission of the signal as the diode is assumed to be ideal. The output is in the form of half-cycles, similar to the output of a half-wave rectifier called as a half-wave rectifier.

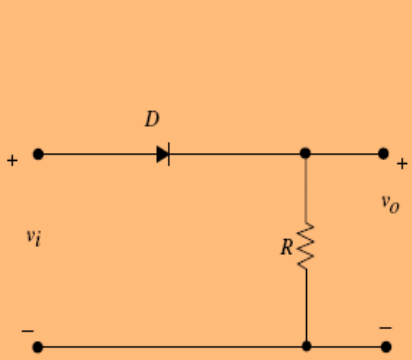


Figure 2.1(a) Series clipper that clips the negative half-cycles

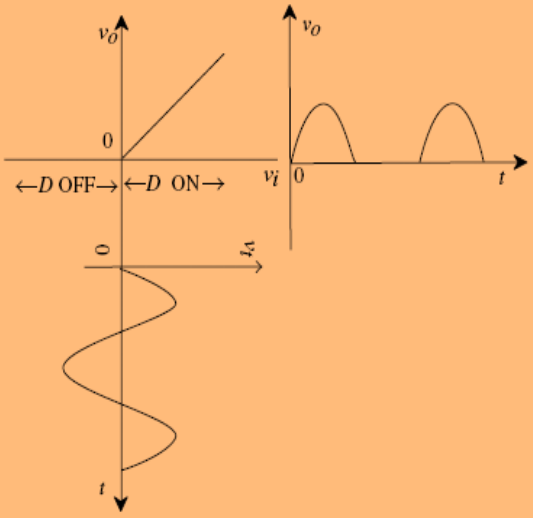


Figure 2.1(b) The transfer characteristic, input waveform and output waveform of a series clipper that clips negative half-cycles

- Consider another clipping circuit shown in Figure 2.2(a) and its transfer characteristic with input and output waveforms in Figure 2.2(b).
- When $v_i \leq 0$ is negative, D conducts, $v_O = v_i$, slope is 1 and the input v_i is transmitted to the output .

- When $v_i > 0$ is positive, D is OFF, $v_o = 0$ and slope is 0. The signal is not transmitted to the output.
- These two conditions are known as the Transfer characteristic equations. The output once again is in the form of half-cycles.

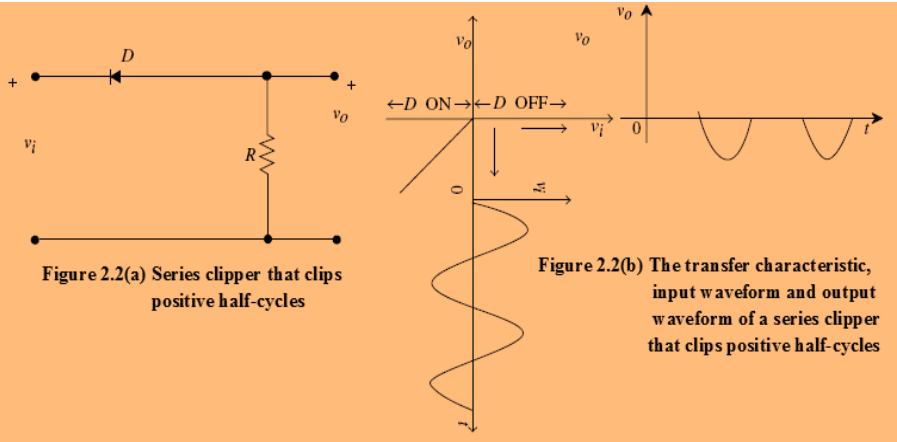


Figure 2.2(a) Series clipper that clips positive half-cycles

Figure 2.2(b) The transfer characteristic, input waveform and output waveform of a series clipper that clips positive half-cycles

In our discussion so far, we have assumed the diode to be ideal and have neglected the influence of the transition capacitance C_T that exists between the anode and the cathode of a reverse-biased diode. We now take into account this parameter to understand how this affects the output of a series clipper. Consider the circuit shown in Figure 2.2(a) when reverse-biased (during the positive half-cycle), to which, instead of a sinusoidal signal, a square-wave input is applied. So far we have assumed that during the period when the diode is OFF, there is no transmission. However, on account of the transition capacitance C_T being present, the circuit now behaves as a high-pass circuit [see Figure 2.2(c)] and the input can now be transmitted to the output, though with distortion. Also, even if a sinusoidal signal is applied as input, at high frequencies, the capacitor offers a smaller reactance due to which the input can be transmitted to the output. This is the major limitation of a series clipper. Thus, a series clipper works best at low frequencies.

Clipping circuits select that part of the signal which lies above and below a reference level. Depending on whether the diode is connected in series with the load or in shunt with the load, these circuits are called either series-clipping circuits or shunt-clipping circuits.

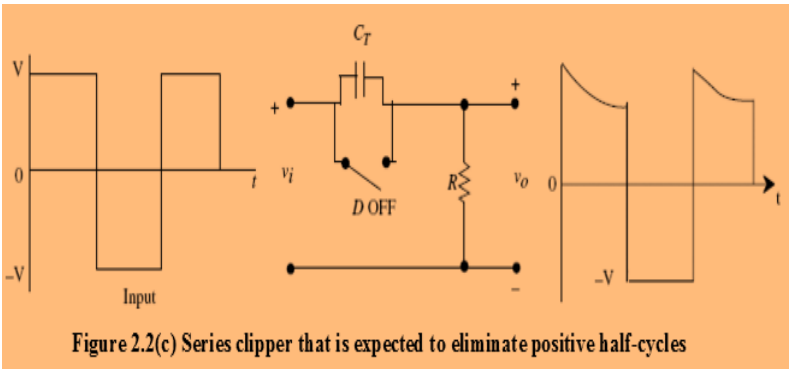


Figure 2.2(c) Series clipper that is expected to eliminate positive half-cycles

2.4 Base Clipper or Biased Clipper:

If a battery (V_R) is included in the series-clipping circuit, such that the diode is connected in series with the load, as shown in Figure 2.3(a), these circuits are called biased series clippers.

The circuit in Figure 2.3(a) clips the positive going input at its base, so it is also referred to as a base clipper.

Assume that the diode is ideal in the circuit shown in Figure 2.3(a).

- For $v_i < V_R$, D is OFF; hence, $v_o = V_R$. Slope is 0. The resultant circuit is shown in Figure 2.3(b).
- For $v_i \geq V_R$, D is ON; hence, $v_O = v_i$.Slope is 1. The resultant circuit is shown in Figure 2.3(c).
- These two equations are known as Transfer characteristic equations.

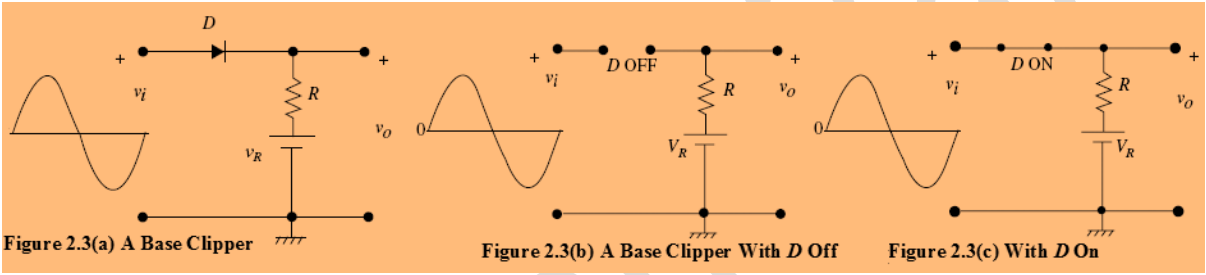


Figure 2.3(a) A Base Clipper

Figure 2.3(b) A Base Clipper With *D* Off

Figure 2.3(c) With *D* On

- The transfer characteristic is shown in Figure 2.3 (d).
- In the output of this circuit, the base portion of the input during the positive half-cycle is eliminated and only the positive peak is available when the input is either more than or equal to V_R, hence the name base clipper.
- The battery V_R is assumed to have zero internal resistance.
- However, in practice, any voltage source will have some internal resistance R_S which appears in series with the battery.
- Now, as this R_S in the present case appears in series with R, where $R >> R_S$, the performance of the circuit is not affected.
- This could be termed as an advantage of series clippers.

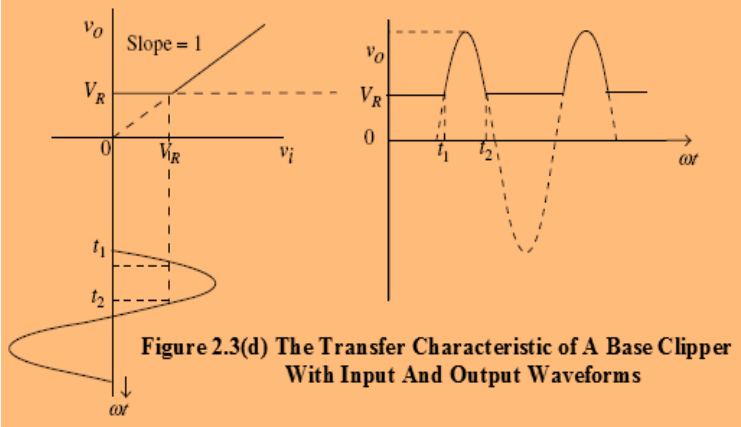


Figure 2.3(d) The Transfer Characteristic of A Base Clipper With Input And Output Waveforms

2.5 Positive-Peak Clipper:

- Consider the circuit shown in Figure 2.4 (a). As this circuit eliminates the positive peak of the input and present at the output, it is called as a positive peak clipper.
- For $v_i \le V_R$, D is ON and $v_O = v_i$. Slope is 1.
- The resultant circuit is shown in Figure 2.4 (b).

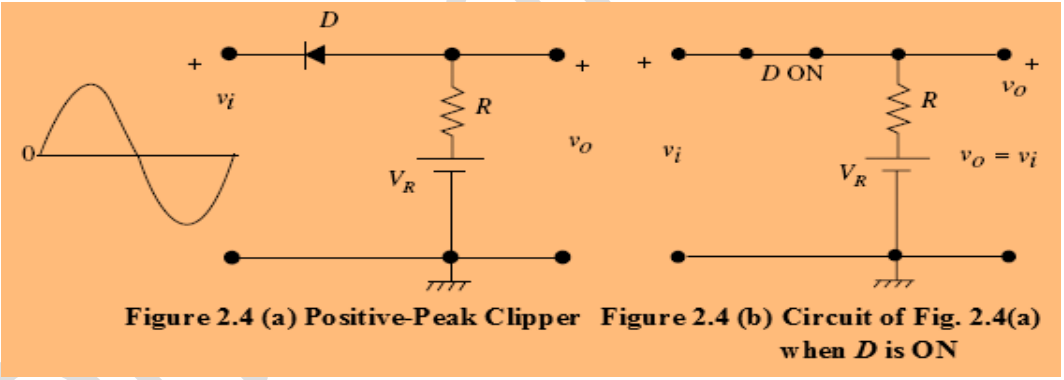


Figure 2.4 (a) Positive-Peak Clipper **Figure 2.4 (b) Circuit of Fig. 2.4(a) when *D* is ON**

- For $v_i > V_R$, D is OFF and $v_o = V_R$. Slope = 0.
- The resultant circuit is shown in Figure 2.4 (c).
- Thus the transfer characteristic i.e. the input and output waveforms are as shown in Figure 2.4 (d).
- In the output of the circuit, the positive peak of the input above V_R is eliminated.
- Hence, this circuit is called a positive peak clipper.

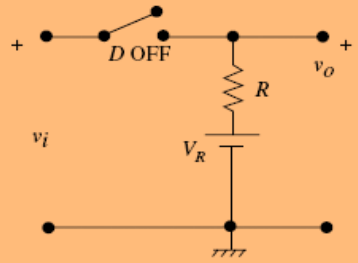


Figure 2.4 (c) Circuit of Fig. 2.4 (a) when *D* is OFF

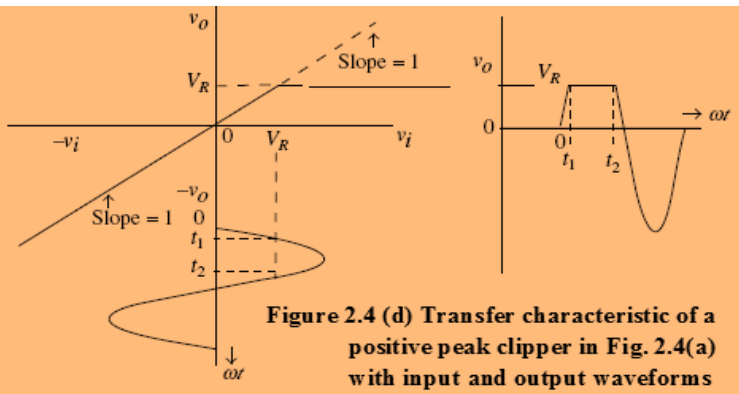


Figure 2.4 (d) Transfer characteristic of a positive peak clipper in Fig. 2.4(a) with input and output waveforms

2.6 Clipping above the Reference Voltage V_R:

- Figure 2.5(a) shows a series clipper circuit using a p-n junction diode. V_R is the reference voltage source.
- The diode is assumed to be ideal ($R_f = 0, R_r = \infty, V_\gamma = 0$) so that it acts as a short circuit when it is ON and as an open circuit when it is OFF.
- Since the diode is in the series path connecting the input and the output it is called a series clipper.
- The v_o versus v_i, characteristic called the *transfer characteristic* is shown in Figure 2.5(b).
- The output for a sinusoidal input is shown in Figure 2.5(c).
- The circuit works as follows
- Case:1. For $v_i \le V_R$, the diode D is forward biased because its anode is at a higher potential than its cathode. It conducts and acts as a short circuit and the equivalent circuit shown in Figure 2.5(d) results.
- The difference voltage between the input v_i and the reference voltage V_R i.e. ($v_i - V_R$) is dropped across *R*.
- Therefore $v_O = v_i$ and the slope of the transfer characteristic for $v_i \le V_R$ is 1. Since the input signal is transmitted to the output without any change, this region is called the ***transmission region.***

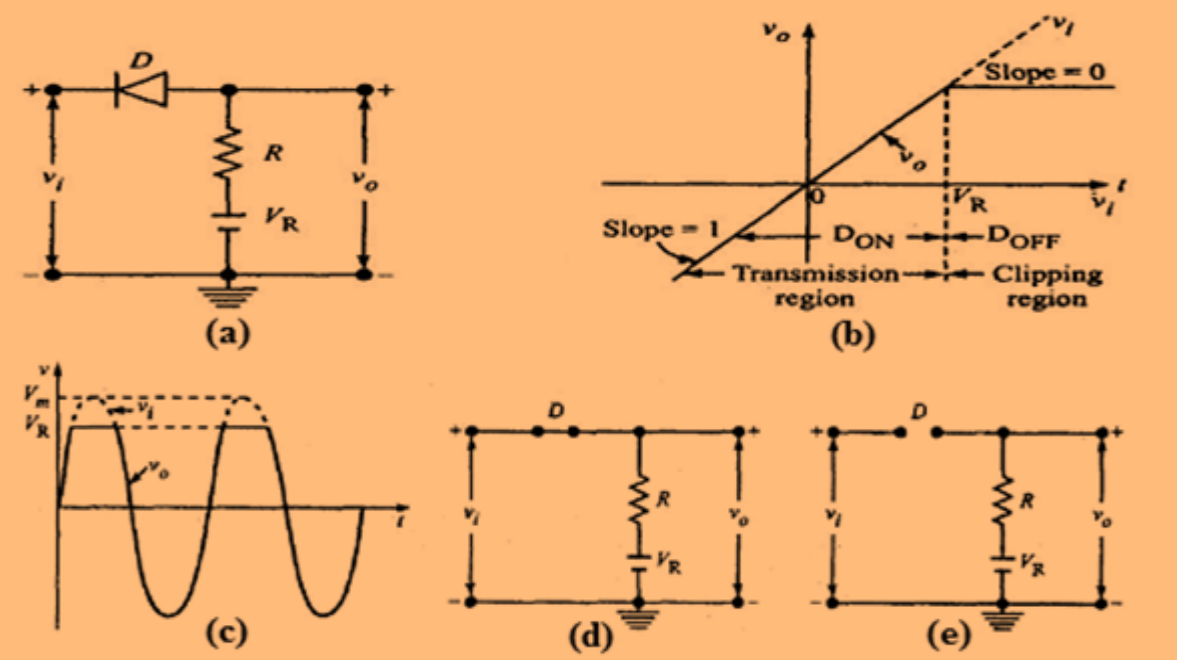


Figure 2.5 (a) Diode series clipper circuit diagram, (b) transfer characteristic, (c) output waveform for a sinusoidal input, (d) equivalent circuit for $v_i < V_R$, and (e) equivalent circuit for $v_i > V_R$.

- Case:2. For $v_i > V_R$, the diode is reverse biased because its cathode is at a higher potential than its anode, it does not conduct and acts as an open circuit and the equivalent circuit shown in Figure 2.5(e) results.
- No current flows through *R* and so no voltage drop across it.
- So the output voltage $v_o = V_R$ and the slope of the transfer characteristic is 0.
- Since the input signal above V_R is clipped OFF for $v_i > V_R$, this region is called the *clipping region*.
- The equations $v_o = v_i$ for $v_i \le V_R$ and $v_o = V_R$ for $v_i > V_R$ are called the ***transfer characteristic equations.***

2.7 Clipping below the Reference Voltage V_R:

- Figure 2.6(a) shows a series clipper circuit using a p-n junction diode and a reference voltage source V_R.
- The diode is assumed to be ideal ($R_f = 0, R_r = \infty, V_\gamma = 0$) so that it acts as a short circuit when it is ON and as a open circuit when it is OFF.

- Since the diode is in the series path connecting the input and the output it is called a series clipper.
- The transfer characteristic is shown in Figure 2.6(b). The output for a sinusoidal input is shown in Figure 2.6(c).The circuit works as follows:
- Case:1 For $v_i < V_R$, D is reversed biased because its anode is at a lower potential than its cathode.
- The diode does not conduct and acts as an open circuit and the equivalent circuit shown in Figure 2.6(d) results.
- No current flows through *R* and hence no voltage drop across *R* and hence $v_o = V_R$.
- So the slope of the transfer characteristic is zero for $v_i < V_R$. Since the input is clipped off for $v_i < V_R$, this region is called the clipping region.

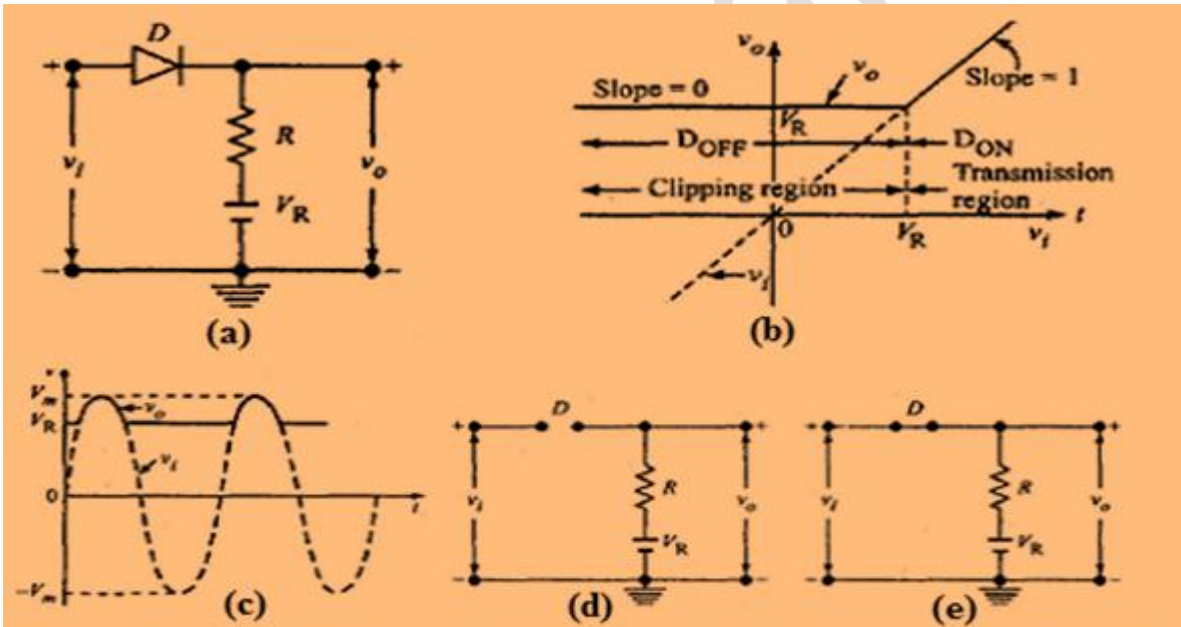


Figure 2.6 (a) Diode series clipper circuit diagram, (b) Transfer characteristics, (c) Output for a sinusoidal input, (d) Equivalent circuit for $v_i < V_R$, and (e) Equivalent circuit for $v_i > V_R$.

- Case:2. For $v_i \geq V_R$, the diode is forward biased because its anode is at a higher potential than its cathode.
- The diode conducts and acts as a short circuit and the equivalent circuit shown in Figure 2.6(e) results.

- Current flows through R and the difference voltage between the input and the output voltages $v_i - V_R$ drops across R and the output is $v_O = v_i$.
- The slope of the transfer characteristic for $v_i > V_R$ is unity. Since the input is transmitted to the output for $v_i \geq V_R$ this region is called the transmission region.
- The equations are called the transfer characteristic equations.

$v_O = V_R \quad for \; v_i < V_R$
$v_O = v_i \quad for \; v_i \geq V_R$

2.8 Shunt Clippers:

- A shunt clipper is one in which the diode is used as a shunt element. Consider a simple shunt clipper shown in Figure 2.7(a).
- As long as the input is positive, *D* conducts and the output *vo* = 0.
- When the input is negative, *D* is OFF and an open circuit. The input is transmitted to the output.
- The transfer characteristic, the input and output waveforms are shown in Figure 2.7(b). This circuit clips the positive half-cycle.
- The same thing is done by the circuit shown in Figure 2.2(a). The only difference is that the former is a series clipper and the latter a shunt clipper.
- Till now we assumed that the diode to be ideal, that is, forward resistance of the diode was taken to be zero.
- A practical diode, however, has typically R_f in the range of 50 Ω to 100 Ω.
- Therefore, when *D* is ON, with R_f taken into account, the circuit is as shown in Figure 2.5(c) and the output $v_O = \dfrac{v_i \; R_f}{\left(R_f + R\right)}$.
- This means that though the output is expected to be 0, there is a small sinusoidal swing at the output. This is one limitation of a shunt clipper.
- When *D* is OFF, it should ideally behave as an open circuit. But in a reverse-biased diode, we have transition capacitance C_T. Taking C_T into account Figure 2.7(a) can be redrawn as shown in Figure 2.7(d) and the output $v_O = \dfrac{v_i \; R_r}{\left(R_r + R\right)}$.

- Now, when the diode is OFF, with a square wave as the input, we ideally expect the negative half-cycle of the input only at the output.
- However, when C_T is considered, then the shunt clipper acts a low-pass circuit. Hence, the output would rise with a time constant RC_T. This is another limitation of a shunt clipper.

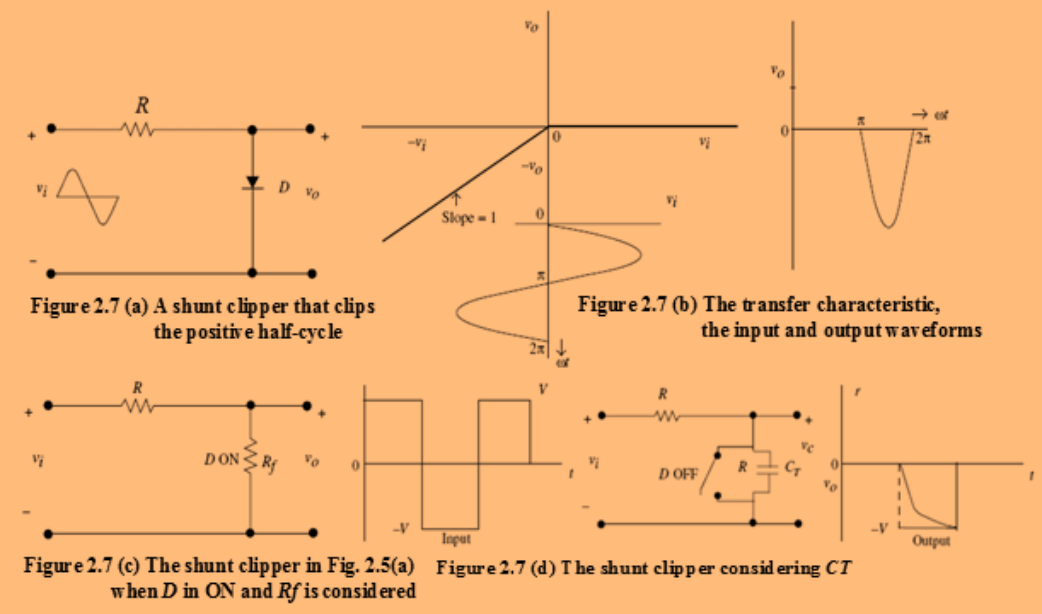


Figure 2.7 (a) A shunt clipper that clips the positive half-cycle

Figure 2.7 (b) The transfer characteristic, the input and output waveforms

Figure 2.7 (c) The shunt clipper in Fig. 2.5(a) when *D* in ON and *Rf* is considered

Figure 2.7 (d) The shunt clipper considering *CT*

- Consider an alternative form of the shunt clipper as shown in Figure 2.8(a).
- The transfer characteristic along with the input and output waveforms is shown in Figure 2.8(b). The negative half-cycle is completely eliminated.

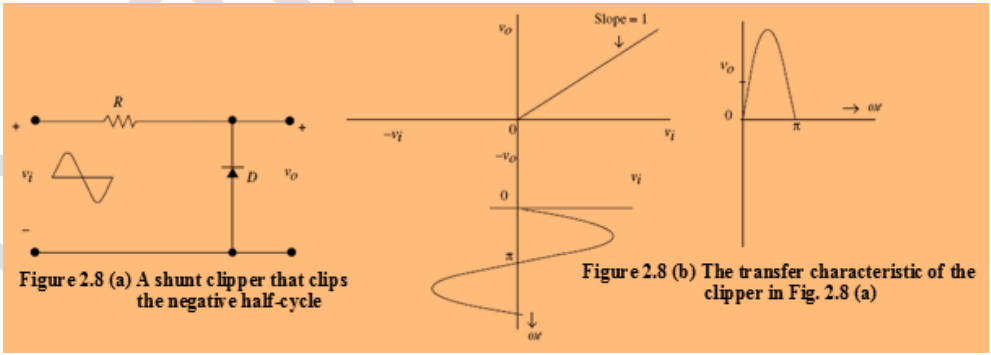


Figure 2.8 (a) A shunt clipper that clips the negative half-cycle

Figure 2.8 (b) The transfer characteristic of the clipper in Fig. 2.8 (a)

- Now let us consider a slightly different shunt clipper called a biased shunt clipper that clips the positive half-cycle of the input waveform at a reference level V_R [see Figure 2.9 (a)].
- When $v_i < V_R$, D is OFF, hence $v_o = v_i$. Slope is 1
- When $v_i \geq V_R$, D is ON, hence $v_o = V_R$. Slope is 0
- The transfer characteristic is drawn in Figure 2.9(b).

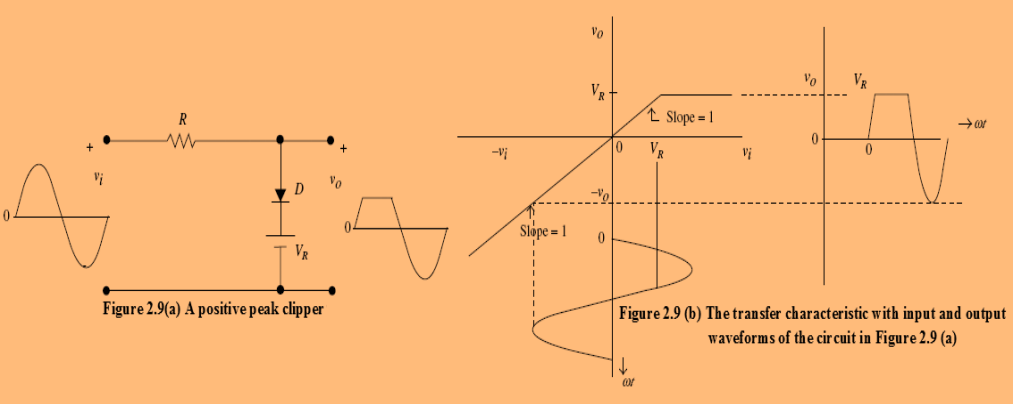


Figure 2.9(a) A positive peak clipper

Figure 2.9 (b) The transfer characteristic with input and output waveforms of the circuit in Figure 2.9 (a)

- To calculate and plot the output of the clipping circuit shown in Figure 2.9(a), consider a sinusoidal input signal varying as $V_m \sin \omega t$.
- **Case 1:** When the diode is ideal, its $R_f = 0, R_r = \infty, V_\gamma = 0$.
- When $v_i < V_R$, D is OFF, hence $v_O = v_i$. Slope is 1.
- When $v_i \geq V_R$, D is ON, hence, $v_o = V_R$. Slope is 0.
- **Case 2:** When the diode is not ideal and has finite forward and reverse resistances.
- 1. When $v_i \geq V_R$ the diode is ON, it has a forward resistance R_f.

The resultant circuit is as shown in Figure 2.10(a).

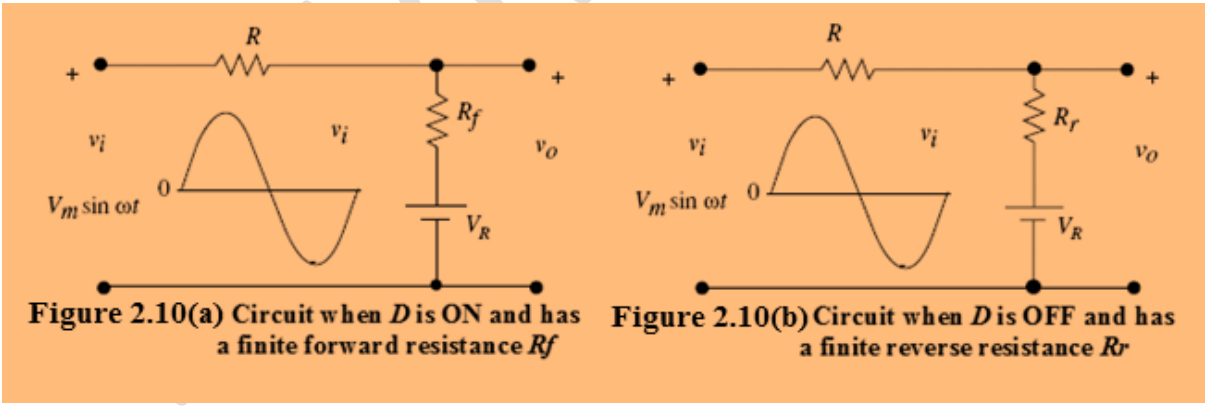


Figure 2.10(a) Circuit when D is ON and has a finite forward resistance Rf

Figure 2.10(b) Circuit when D is OFF and has a finite reverse resistance Rr

- Here, the output is $v_O = (v_i - V_R) \times \dfrac{R_f}{R + R_f} + V_R$ ----------2.1
- Thus, v_O is maximum when v_i is maximum that is when $v_i = V_m$.
- If $V_m \approx 2V_R$, then the maximum output voltage is

- $v_{o(\max)} = (2V_R - V_R) \times \frac{R_f}{R + R_f} + V_R = V_R\left(\frac{R_f}{R + R_f} + 1\right) = V_R\left(\frac{R + 2R_f}{R + R_f}\right)$ ----------2.2
- If the source V_R has an internal resistance R_S, $v_{o(\max)}$ computed using $R_f = (R_f + R_S)$, instead of R_f. R_S will influence the slope of the transfer characteristic. This could be another drawback of a shunt clipper.
- 2. When $v_i < V_R$, the diode is OFF and the reverse resistance of the diode is R_r.
- The resultant circuit that enables us to calculate v_o is given in Figure 2.10(b). v_o is minimum when v_i is at its negative maximum, i.e., $v_i = -V_m \approx -2V_R$.
- Therefore,

$$v_{o(\min)} = (v_i - V_R) \times \frac{R_r}{R + R_r} + V_R = (-2V_R - V_R) \times \frac{R_r}{R + R_r} + V_R$$

$$= (-3V_R) \times \frac{R_r}{R + R_r} + V_R = V_R\left(1 - \frac{3R_r}{R + R_r}\right) = V_R\left(\frac{R + R_r - 3R_r}{R + R_r}\right)$$

- $v_{o(\min)} = V_R\left(\frac{R - 2R_r}{R + R_r}\right)$ ----------2.3
- In this case, R_S of the battery will not influence the output in any way because $R_r >> R_S$. R is chosen based on the following considerations.
- Consider the circuit shown in Figure 2.10(b).
- During the transmission period, the diode is OFF, offering a large reverse resistance R_r.
- For the input to be transmitted to the output terminals with negligible loss of signal, R_r should be much larger than R. This requirement says that
- $R_r = k\,R$ or $R = \frac{R_r}{k}$ ----------2.4
- Where k is a large number.
- Consider the circuit shown in Figure 2.10(a).
- When the diode is ON, the output signal is small and is said to be attenuated. This condition stipulates that R should be significantly larger than R_f, the forward resistance of the diode. This requirement means

- $R = k\,R_f$ ----------2.5
- From Equations (2.4) and (2.5):
- $R^2 = R_r R_f$ or $R = \sqrt{R_f R_r}$ ----------2.6
- R is chosen as the geometric mean of R_f and R_r.
- $k = \sqrt{\frac{R_r}{R_f}}$ ----------2.7
- To illustrate how to plot the output, consider following examples shown in Figure 2.11(a) and Figure 2.11(b).

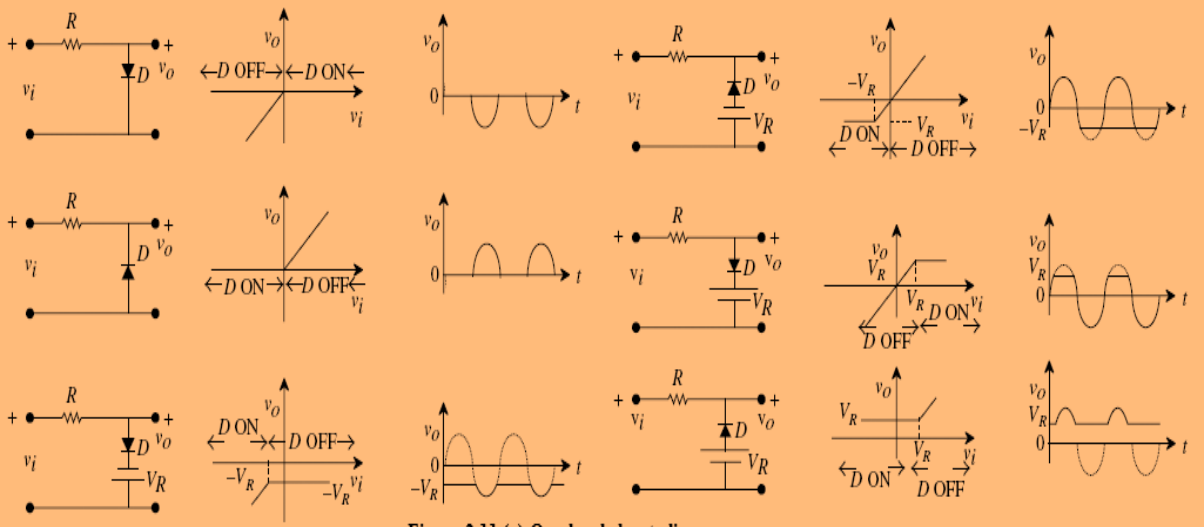


Figure 2.11 (a) One-level shunt clippers

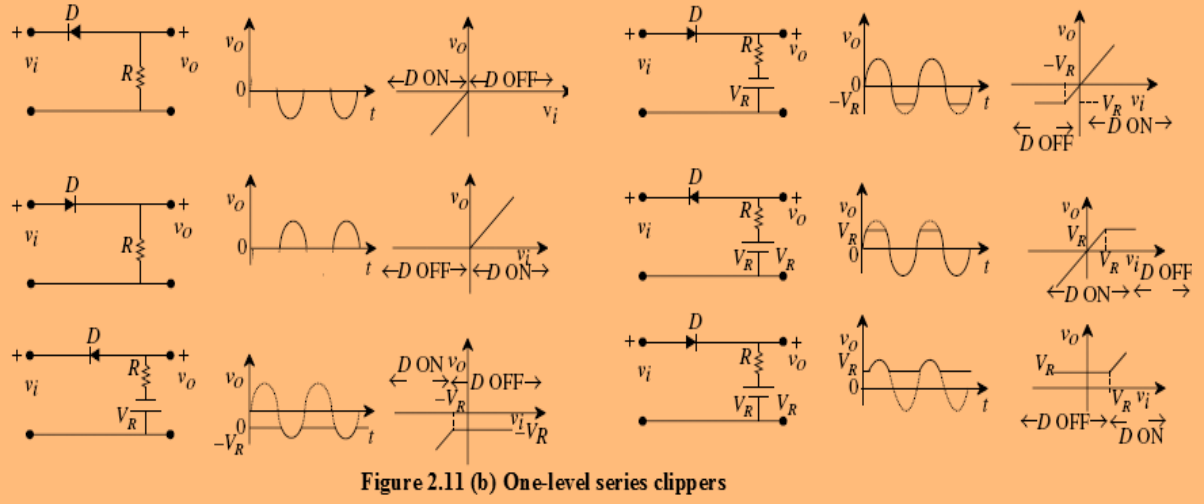
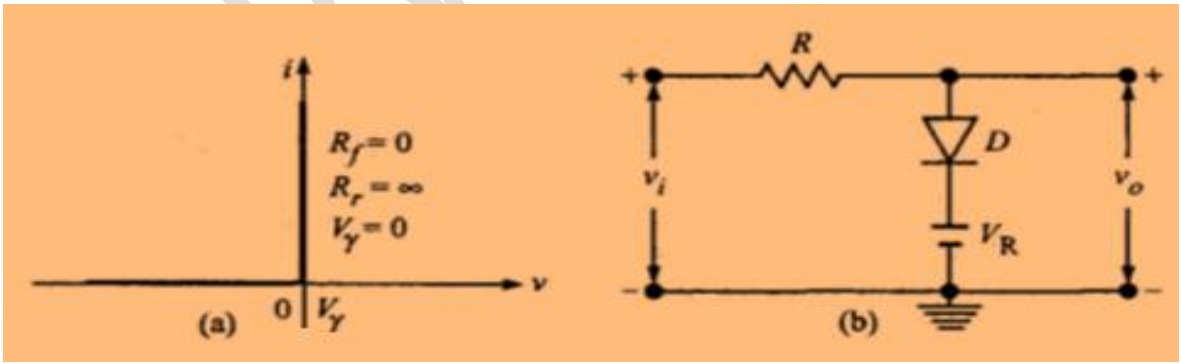


Figure 2.11 (b) One-level series clippers

2.9 Clipping above Reference Level V_R:

- Using the ideal diode characteristic of Figure 2.12(a), the clipping circuit shown in Figure 2.12 (b), has the transmission characteristic shown in Figure 2.12 (c).
- The transmission characteristic which is a plot of the output voltage v_o as a function of the input voltage v_i , also exhibits piece-wise linear discontinuity.
- The break point occurs at the reference voltage V_R .
- For $v_i < V_R$ the diode is reverse biased (OFF) and the equivalent circuit shown in Figure 2.12 (d) results. The signal v_i , may be transmitted directly to the output,
- For $v_i \geq V_R$ the diode is forward biased (ON) and the equivalent circuit shown in Figure 2.12 (e) results and the output is fixed at V_R .
- Figure 2.12 (c) shows a sinusoidal input signal of amplitude large enough so that the signal makes excursions past the break point.
- The corresponding output exhibits a suppression of the positive peak of the signal.
- The output will appear as if the positive peak had been ***Clipped off or sliced off*** .



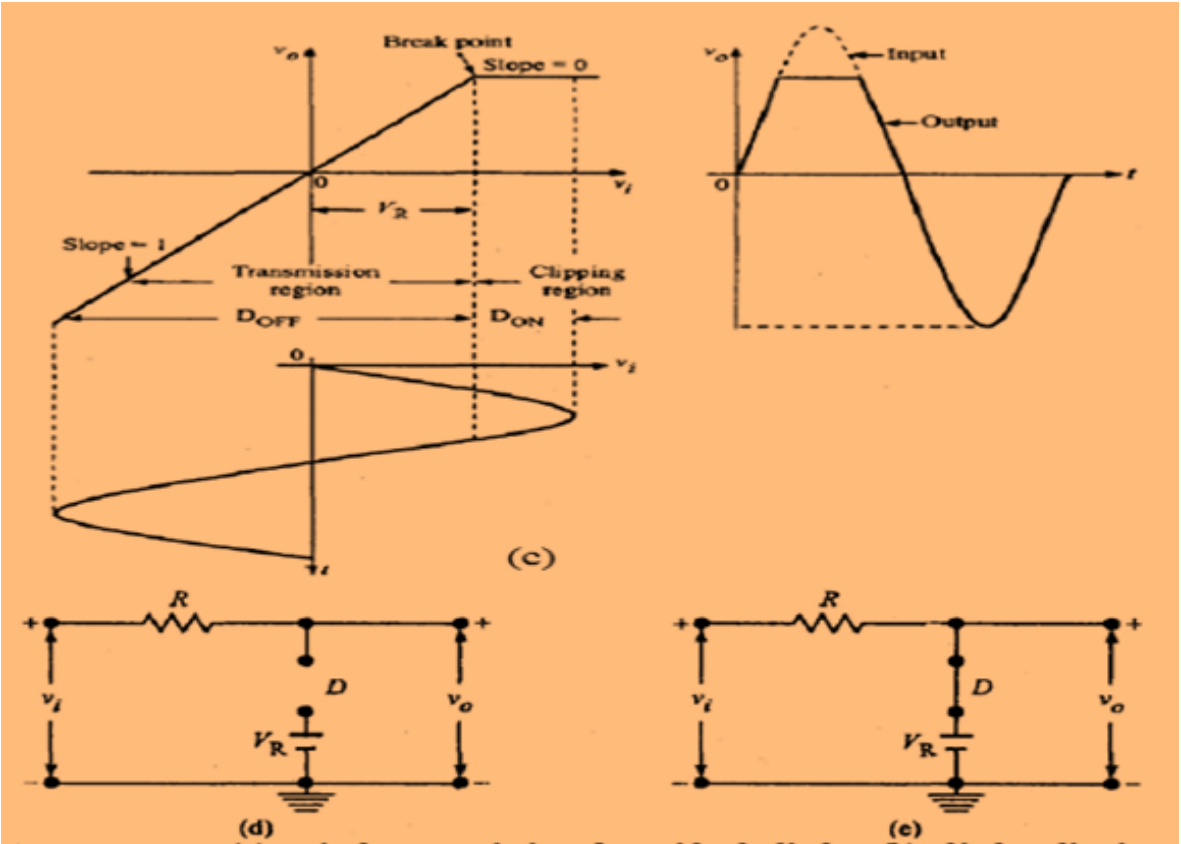


Figure 2.12 (a) *v-i* characteristic of an ideal diode, (b) diode clipping circuit, which removes that part of the waveform that is more positive than V_R, (c) the piece-wise linear transmission characteristic of the circuit, a sinusoidal input and the clipped output, (d) equivalent circuit for $v_i < V_R$, and (e) equivalent circuit for $v_i > V_R$.

2.10 Clipping below Reference Level V_R:

- For the circuit shown in Figure 2.13(a), the corresponding piece-wise linear transfer characteristic and the output for a sinusoidal input will be as shown in Figure 2.13(b).
- For $v_i \le V_R$, the diode conducts and acts as a short circuit and the equivalent circuit shown in Figure 2.13(c) results and the output is fixed at V_R. The portion of the waveform less positive than V_R is totally suppressed.
- For $v_i > V_R$, the diode is reverse biased and acts as an open circuit and the equivalent circuit shown in Figure 2.13(d) results and the output is the same as the input. The portion of the waveform more positive than V_R is transmitted without any attenuation.

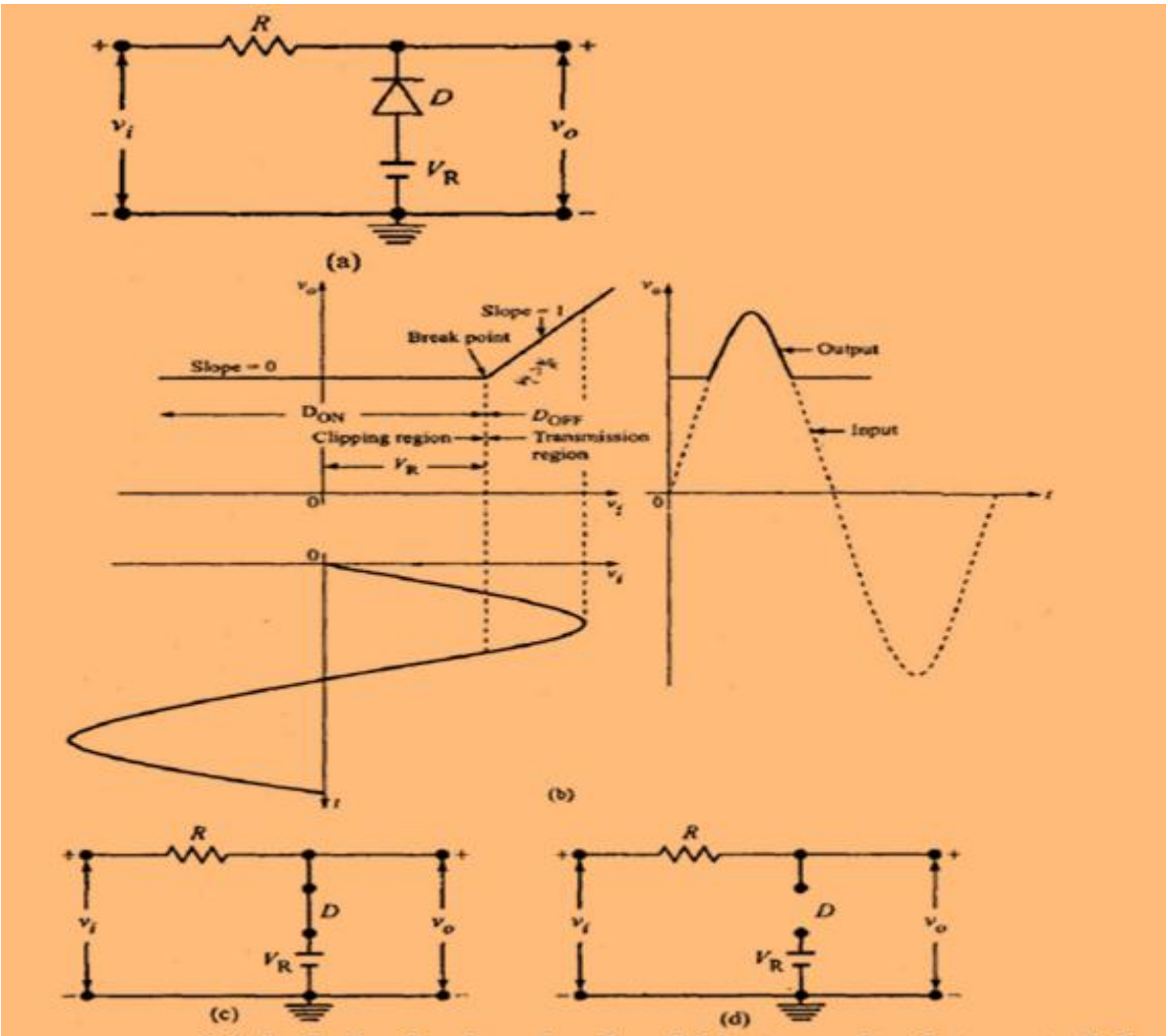


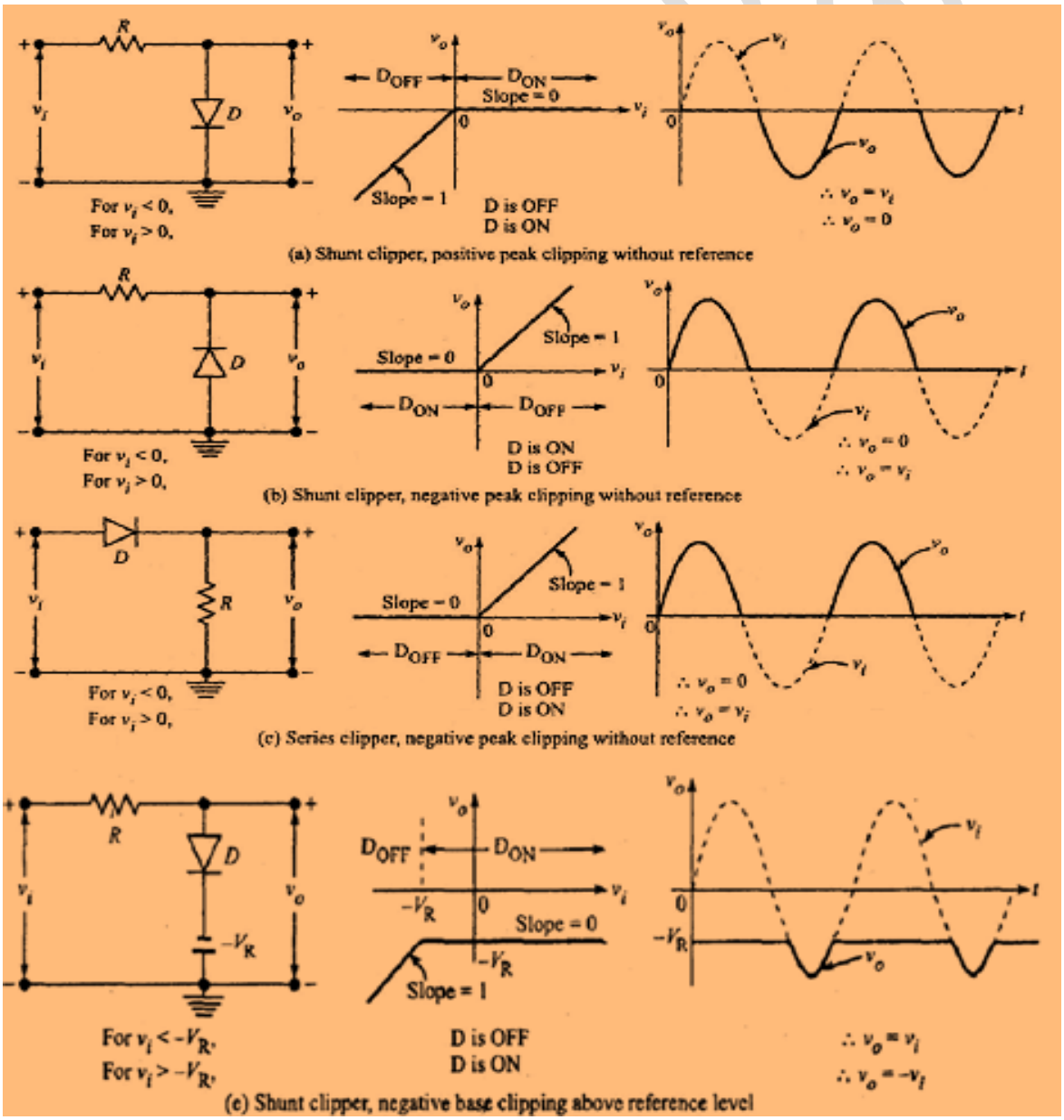
Figure 2.13 (a) A diode clipping circuit, which transmits that part of the sine wave that is more positive than V_R, (b) the piece-wise linear transmission characteristic, a sinusoidal input and the clipped output, (c) Equivalent circuit for $v_i < V_R$, and (d) Equivalent circuit for $v_i > V_R$.

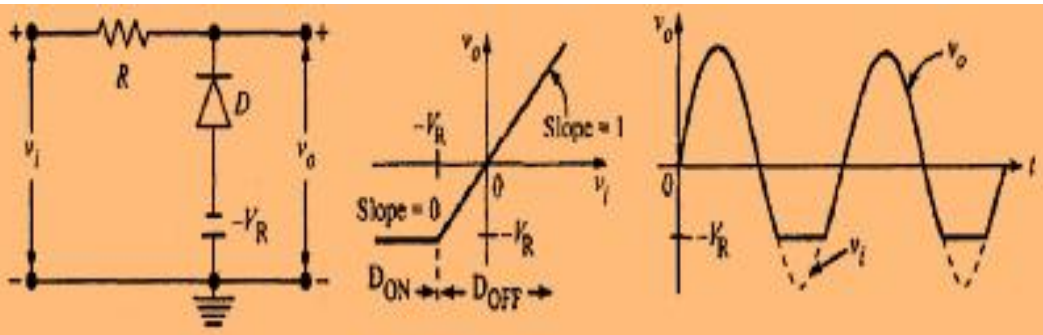
- For a given ideal diodes we assumed that $R_f = 0$ and $R_r = \infty$.
- If this condition does not apply, the portions of those curves which are indicated as having unity slope must be considered as having a slope of $R_r/(R_r + R)$, and those, having zero slope as having a slope of $R_f/(R_f + R)$.
- In the transmission region of a diode clipping circuit, it is required that $R_r >> R$, i.e. $R_r = kR$, where k is a large number.
- And in the attenuation region, it is required that $R >> R_f$ i.e. $R = kR_f$.

- From these equations we can deduce that $R^2 = R_r R_f$ or $R = \sqrt{R_f R_r}$, i.e. the external resistance R is to be selected as the geometric mean of R_f and R_r
- The ratio $k = \sqrt{R_r / R_f}$ serves as a figure of merit for the diodes used in these applications.
- A zener diode may also be used in combination with a *p-n* junction diode to obtain single-ended clipping, i.e. one-level clipping.

2.11 Some Single-Ended Clipping Circuits:

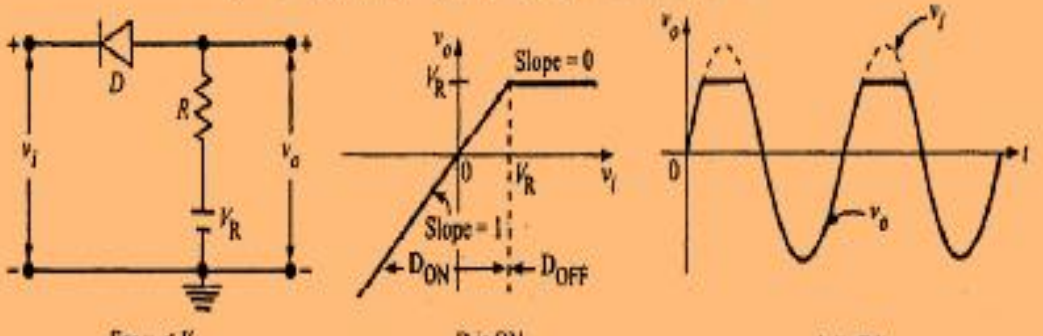
Some single-ended diode clipping circuits, their transfer characteristics and the output waveforms for sinusoidal inputs are shown in below Figure 2.14.





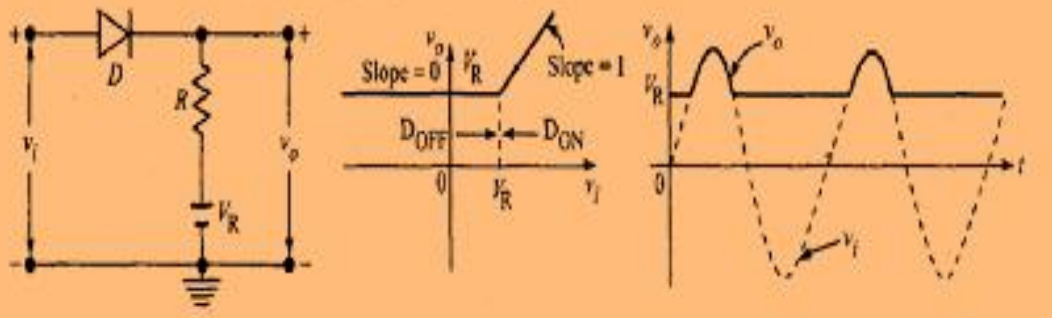
For $v_i < -V_R$, D is ON, $\therefore v_o = -V_R$
For $v_i > -V_R$, D is OFF, $\therefore v_o = v_i$

(f) Shunt clipper, negative base clipping below reference level



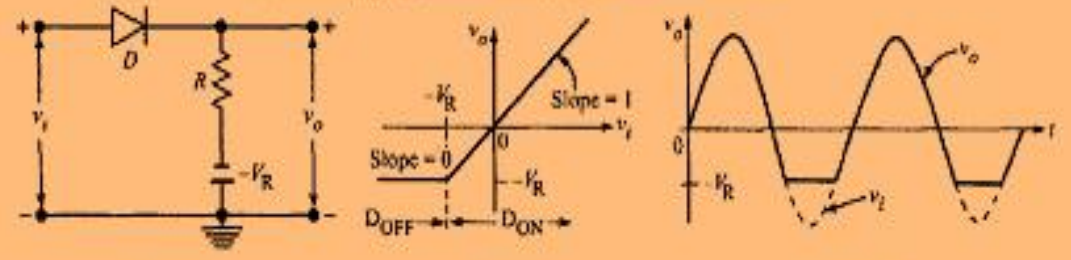
For $v_i < V_R$, D is ON, $\therefore v_o = v_i$
For $v_i > V_R$, D is OFF, $\therefore v_o = V_R$

(g) Series clipper, positive base clipping above reference level



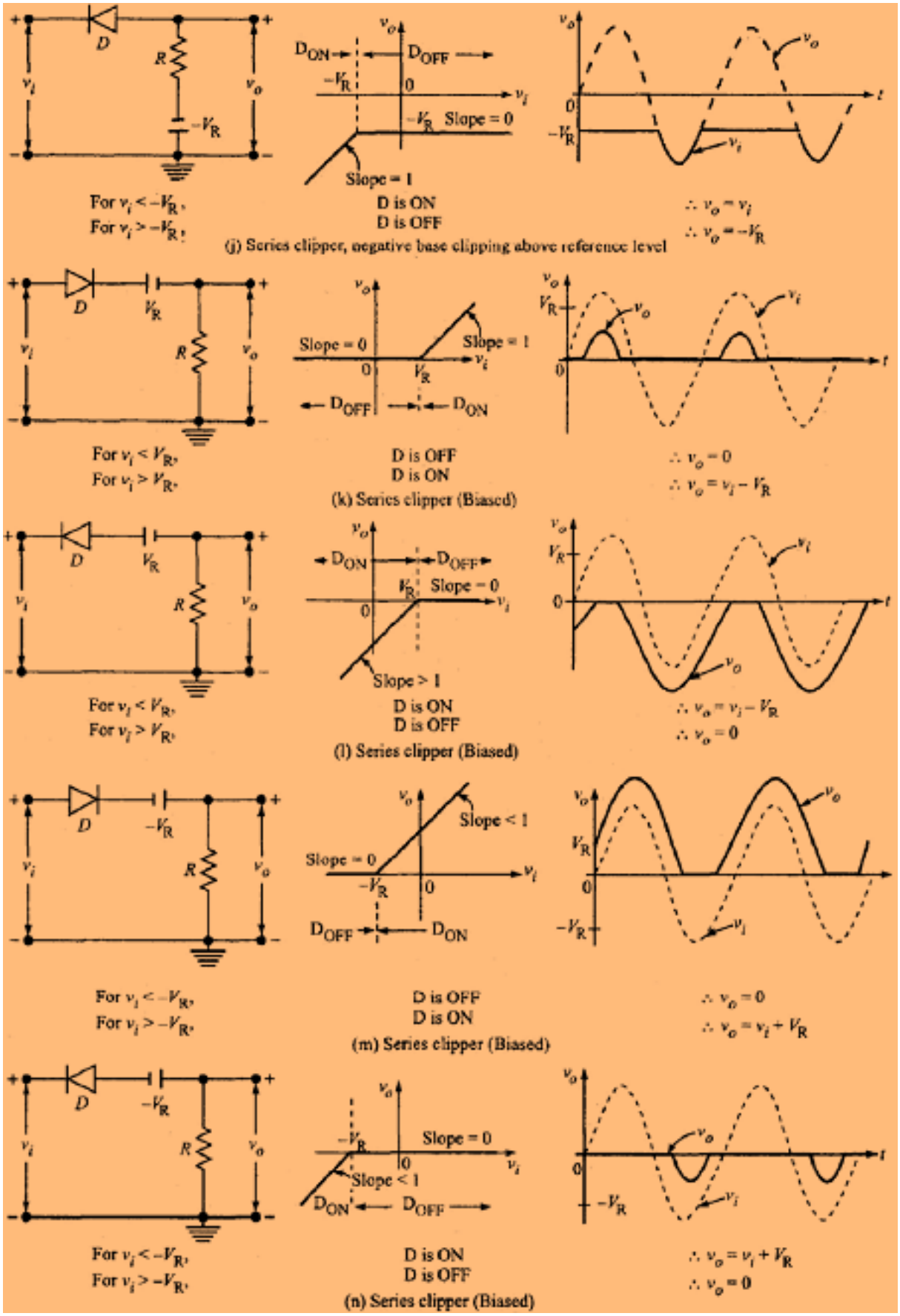
For $v_i < V_R$, D is OFF, $\therefore v_o = V_R$
For $v_i > V_R$, D is ON, $\therefore v_o = v_i$

(h) Series clipper, positive base clipping before reference level



For $v_i < -V_R$, D is OFF, $\therefore v_o = -V_R$
For $v_i > -V_R$, D is ON, $\therefore v_o = v_i$

(i) Series clipper, negative base clipping above reference level


D
R
v_i
v_o
$-V_R$
D_{ON}
D_{OFF}
0
Slope = 0
Slope = 1
t
For $v_i < -V_R$, D is ON
For $v_i > -V_R$, D is OFF
$\therefore v_o = v_i$
$\therefore v_o = -V_R$
(j) Series clipper, negative base clipping above reference level
V_R
For $v_i < V_R$, D is OFF
For $v_i > V_R$, D is ON
$\therefore v_o = 0$
$\therefore v_o = v_i - V_R$
(k) Series clipper (Biased)
Slope > 1
(l) Series clipper (Biased)
Slope < 1
(m) Series clipper (Biased)
(n) Series clipper (Biased)

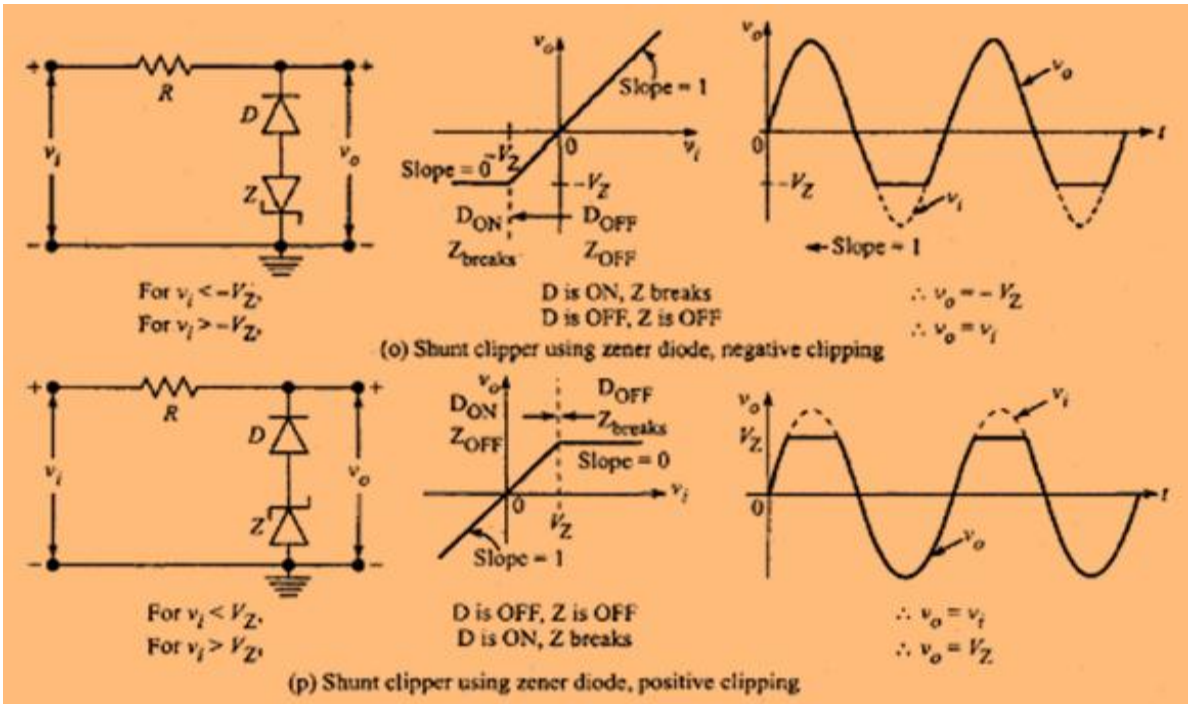


Figure 2.14 (nos. a to p) Examples if Single Ended Clipping Circuits

- In the clipping circuits, the diode may appear as a series element or as a shunt element.
- The use of the diode as a series element has the disadvantage that when the diode is OFF and it is intended that there be no transmission, fast signals or high frequency waveforms may be transmitted to the output through the diode capacitance.
- The use of the diode as a shunt element has the disadvantage that when the diode is open and it is intended that there be transmission, the diode capacitance together with all other capacitances in shunt with the output terminals will round off the sharp edges of the input waveforms and attenuate the high frequency signals.

2.12 Two-Level Clippers:

- Let us now consider clippers which clip the signal at two independent levels.
- Two diode clippers may be used in a cascade to limit the output at two independent levels.

- If a positive-peak clipper and a negative-peak clipper are used in a pair, the resultant circuit is called a two-level clipper.
- If the positive and negative peaks are clipped at the same level, the two-level clipper is called a limiter.
- On the other hand, if a positive-peak clipper and a positive-base clipper are connected in tandem, the circuit is called a positive slicer.

2.13 Slicers:

- The input can be clipped at two independent levels, either during the positive going half-cycle or during the negative going half-period.
- If the input is clipped at two levels during the positive going half-cycle, leaving only a slice of the input at the output, the circuit is called a positive slicer.
- If on the other hand, the signal is sliced during the negative half-cycle, the circuit is called a negative slicer.

2.14 Positive Slicers:

- The circuit shown in Figure 2.15(a) is a positive slicer, as it slices the positive going signal at two independent levels. Consider the following conditions

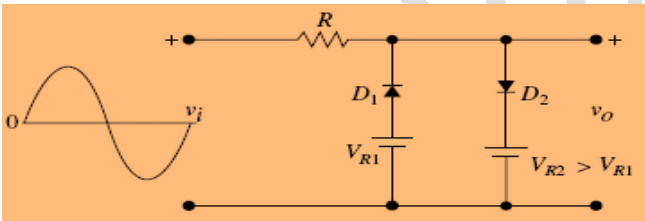


Figure 2.15 (a) A positive slicer

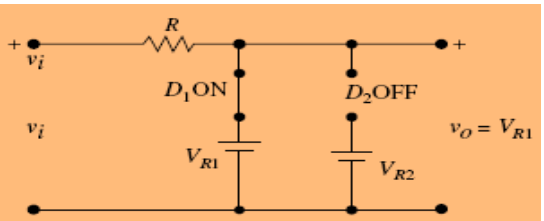


Figure 2.15 (b) The circuit of Fig. 2.15(a) when *D*1 is ON and *D*2 is OFF

- 1. When $v_i \le V_{R1}$, D_1 is ON, D_2 is OFF. The circuit in Figure 2.15(a) reduces to that in Figure 2.15(b). From Figure 2.15(b), $v_o = V_{R1}$.
- 2. When $V_{R1} < v_i < V_{R2}$, D_1 and D_2 are OFF. Hence, the resultant circuit is shown in Figure 2.15(c). From Figure 2.15(c) $v_o = v_i$.
- 3. When $v_i \ge V_{R2}$, D_1 is OFF, D_2 is ON. Hence, the circuit reduces to that in Figure 2.15(d). Hence, $v_o = V_{R2}$.

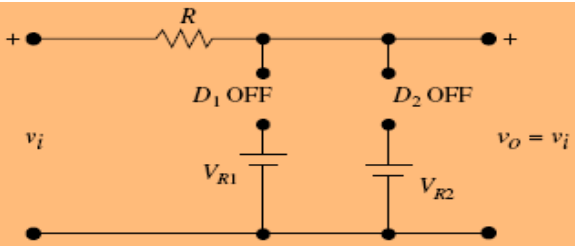


Figure 2.15 (c) The circuit of Fig. 2.15(a) when *D*1 and *D*2 are OFF

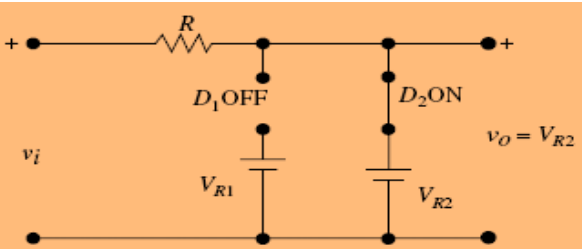


Figure 2.15 (d) The Circuit of Fig. 2.15(a) when *D*1 is OFF and *D*2 is ON

- Figure 2.15(e) represents the transfer characteristic of a positive slicer. We observe that in the output only a portion of the positive going signal is selected.

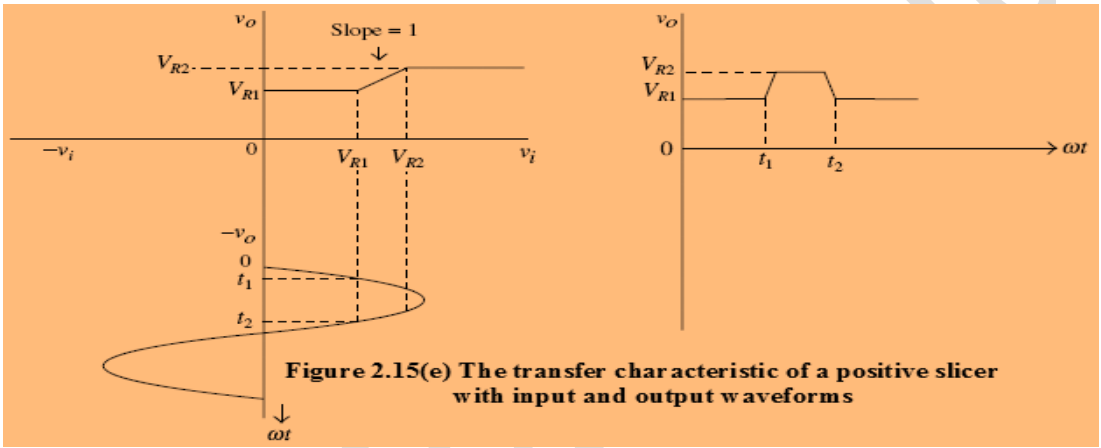


Figure 2.15(e) The transfer characteristic of a positive slicer with input and output waveforms

2.15 Negative Slicers:

- To implement a negative slicer, consider the circuit shown in Figure 2.16(a). Consider the following conditions. Here $-V_{R1}$ *is more positive than* $-V_{R2}$
- Case:1. When $v_i \geq -V_{R1}$, D_1 is ON, D_2 is OFF. The circuit in Figure 2.16(a) reduces to that in Figure 2.16(b). From Figure 2.16(b), $v_o = -V_{R1}$.

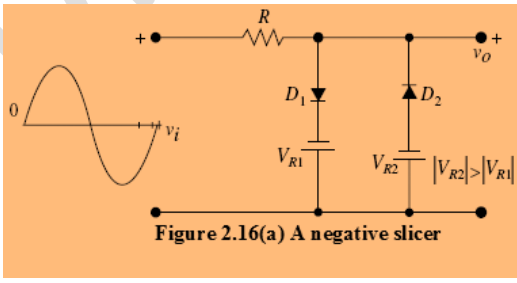


Figure 2.16(a) A negative slicer

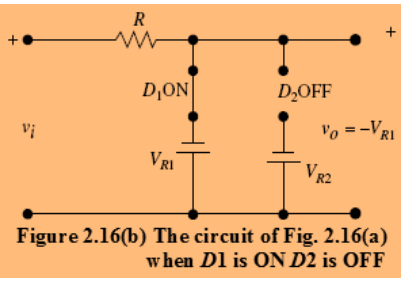


Figure 2.16(b) The circuit of Fig. 2.16(a) when *D*1 is ON *D*2 is OFF

- Case:2. When $-V_{R2} < v_i < -V_{R1}$, D_1 and D_2 are OFF. Hence, the resultant circuit is shown in Figure 2.16(c). From Figure 2.16(c) $v_o = v_i$.

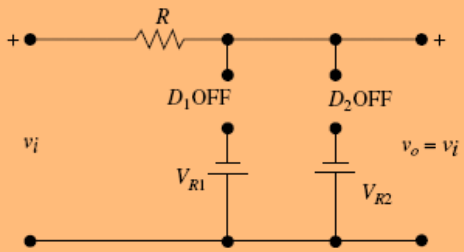


Figure 2.16(c) The circuit of Fig. 2.16(a) when *D*1 and *D*2 are OFF

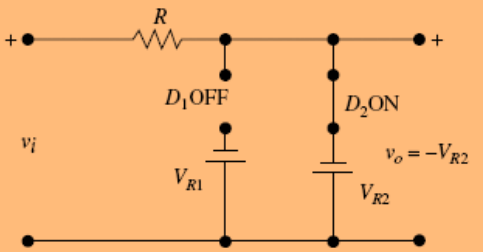


Figure 2.16(d) The circuit of Fig. 2.16(a) when *D*1 is OFF and *D*2 is ON

- Case:3. When $v_i \le -V_{R2}$, D_1 is OFF, D_2 is ON. Hence, the circuit reduces to that in Figure 2.16(d). Hence, $v_o = -V_{R2}$. The transfer characteristic is plotted in Fig. 2.16(e). We see that in the output only a portion of the negative going signal is selected.

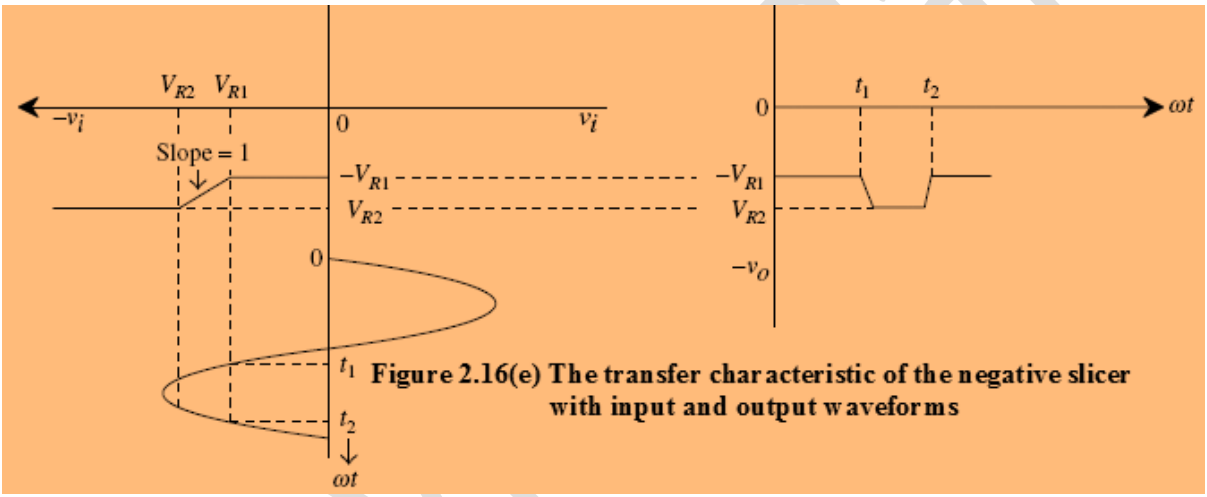


Figure 2.16(e) The transfer characteristic of the negative slicer with input and output waveforms

2.16 Limiters:

- The combination of a positive-peak clipper and a negative-peak clipper, clipping the input symmetrically at the top and the bottom is called a limiter as shown in Figure 2.17(a). Consider the following conditions:
- Case: 1. When $-V_R < v_i < V_R$, D_1 and D_2 are OFF. Hence, the resultant circuit is shown in Figure 2.17(b). From Figure 2.17(b) $v_o = v_i$.

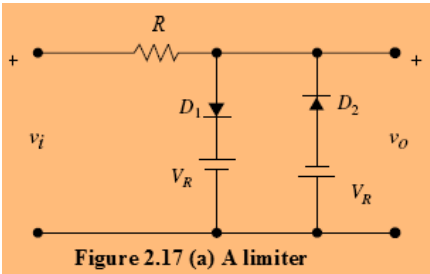


Figure 2.17 (a) A limiter

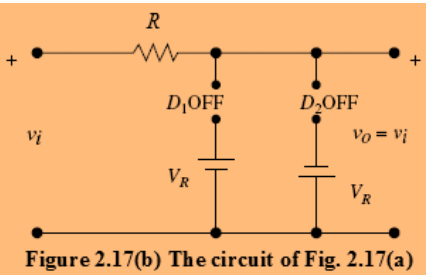


Figure 2.17(b) The circuit of Fig. 2.17(a) when both *D*1 and *D*2 are OFF

- Case: 2. When $v_i \geq V_R$, D_1 is ON, D_2 is OFF. The circuit in Figure 2.17(a) reduces to that in Figure 2.17(c). From Figure 2.17(c), $v_o = V_R$.

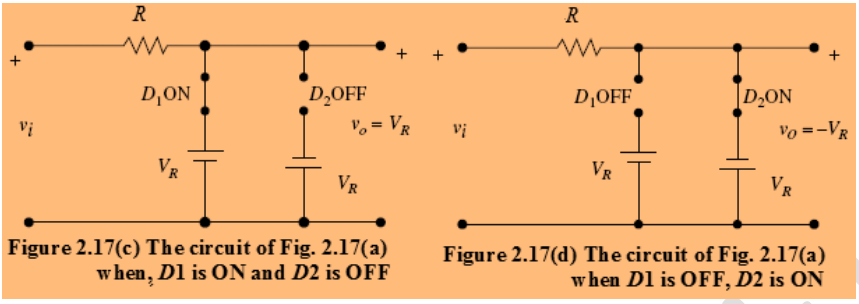


Figure 2.17(c) The circuit of Fig. 2.17(a) when, D1 is ON and D2 is OFF

Figure 2.17(d) The circuit of Fig. 2.17(a) when D1 is OFF, D2 is ON

- Case: 3. When $v_i \leq -V_R$, D_1 is OFF, D_2 is ON. Hence, the circuit reduces to that in Figure 2.17(d). Hence, $v_o = -V_R$. The transfer characteristic is plotted in Figure 2.17(e). We see that in the output both portions of the positive and the negative going signal is selected.

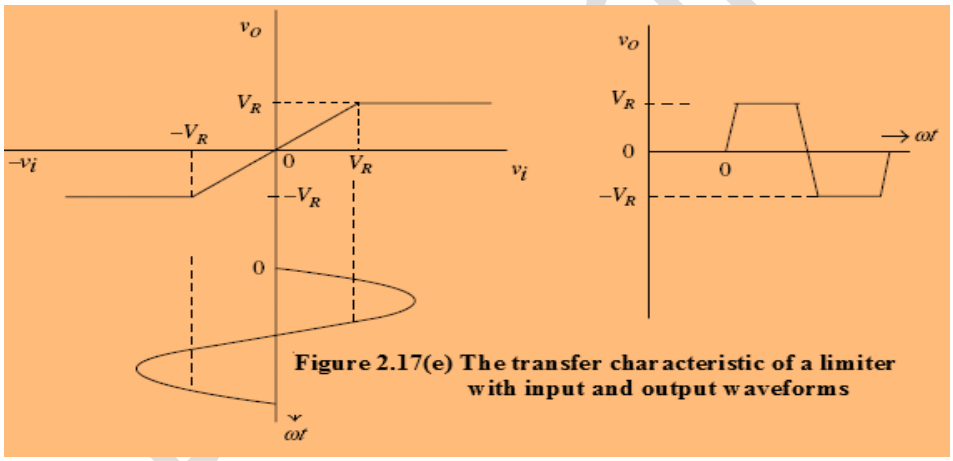


Figure 2.17(e) The transfer characteristic of a limiter with input and output waveforms

- The limiter circuit can also be implemented using Zener diodes as shown in Figure 2.18(a).
- When $-(Vz + V\gamma) < v_i < (Vz + V\gamma)$, $v_O = v_i$ ----------2.8
- The two zeners are OFF , $v_O = v_i$
- When $vi \geq (Vz + V\gamma)$, $v_O = (Vz + V\gamma)$ ----------2.9
- Z_1 Break and Z_2 On , $v_O = (Vz + V\gamma)$
- When $vi \leq -(Vz + V\gamma)$, $v_O = -(Vz + V\gamma)$ ----------2.10
- Z_1 On and Z_2 Break , $v_O = -(Vz + V\gamma)$

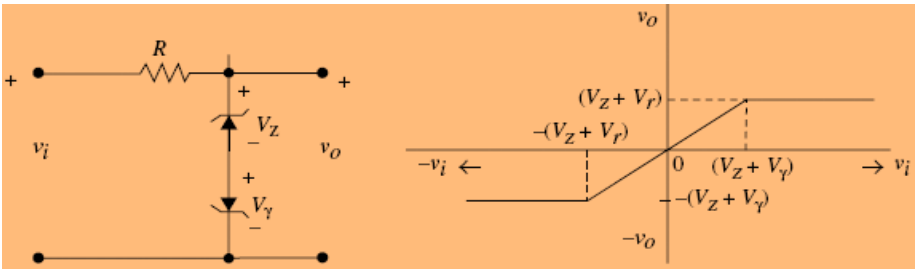


Figure 2.18(a) A limiter using Zener diodes and (b) the transfer characteristic

- The transfer characteristic is drawn in Figure 2.18(b). Limiters are used in frequency-modulated systems where only the frequency of the carrier is varied, but its amplitude remains constant.

2.17 Clipping at Two Independent Levels:

- A parallel- series or a series-parallel arrangement may be used in double-ended limiting at two independent levels.
- A parallel arrangement is shown in Figure 2.19. Figure 2.19(a) shows the transfer characteristic and the output for a sinusoidal input.
- The input-output characteristic has two breakpoints, one at $v_o = v_i = V_{R1}$ and the second at $v_o = v_i = -V_{R2}$, and has the following characteristics.

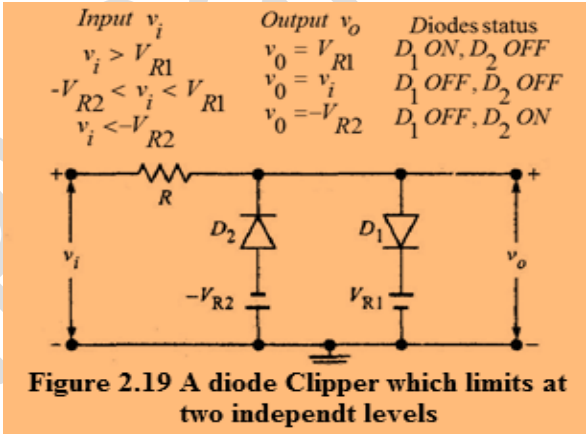


Figure 2.19 A diode Clipper which limits at two independt levels

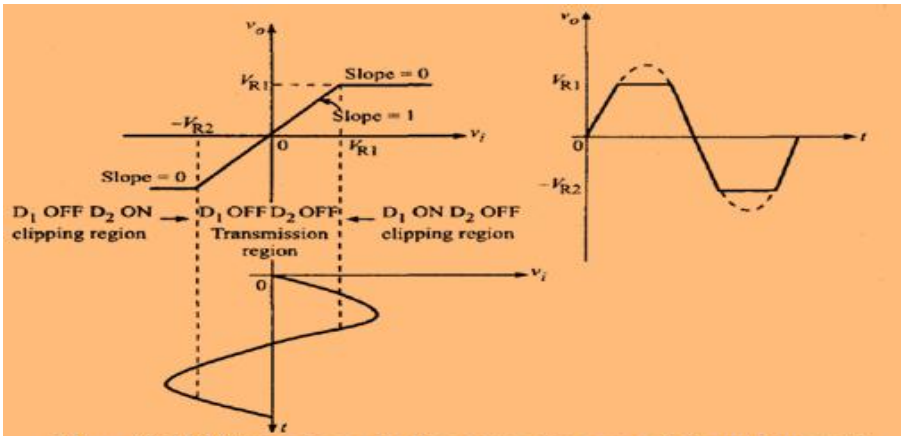


Figure 2. 19 (a) The piece wise linear transfer curve, the input sinusoidal waveform and the corresponding output for the clipper of Figure 2.19

- The two level diode clipper shown in Figure 2.19 works as follows.
- For $v_i \geq V_{R1}$, DI is ON and D2 is OFF and the equivalent circuit shown in Figure 2.19(c) results. So the output $v_O = V_{R1}$ and the slope of the transfer characteristic is zero.

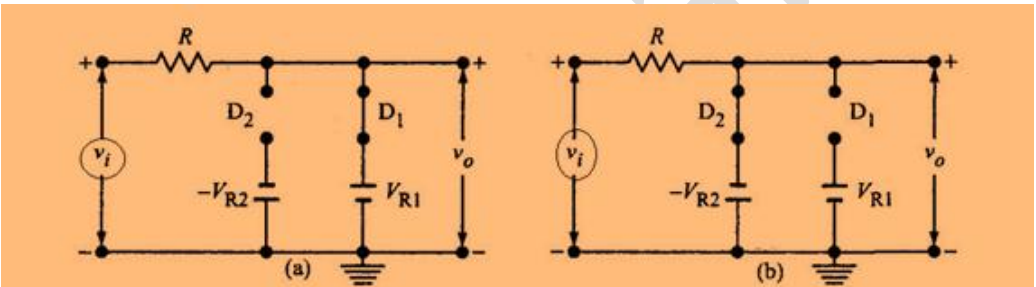


Figure 2.19 (c) equivalent circuit for $v_i > V_{R1}$ and (d) equivalent circuit for $v_i < -V_{R2}$

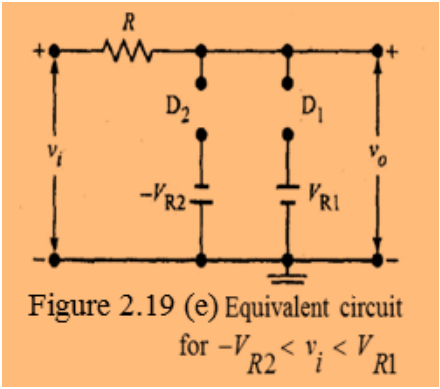
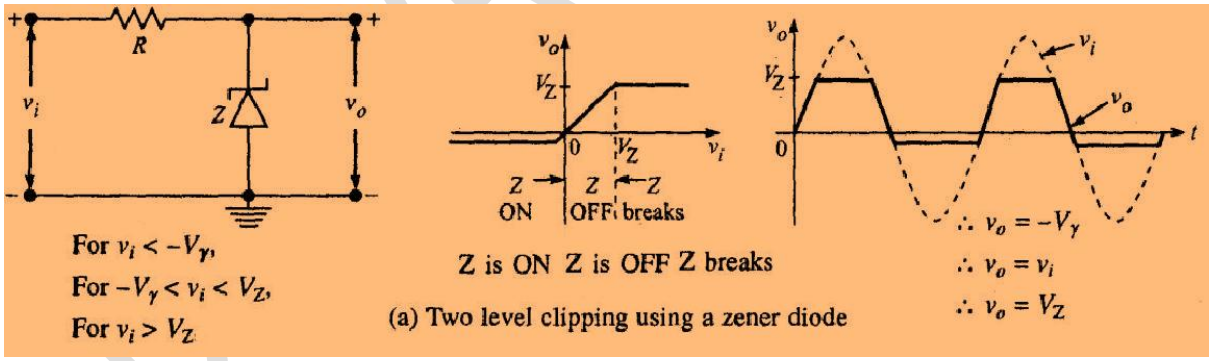


Figure 2.19 (e) Equivalent circuit for $-V_{R2} < v_i < V_{R1}$

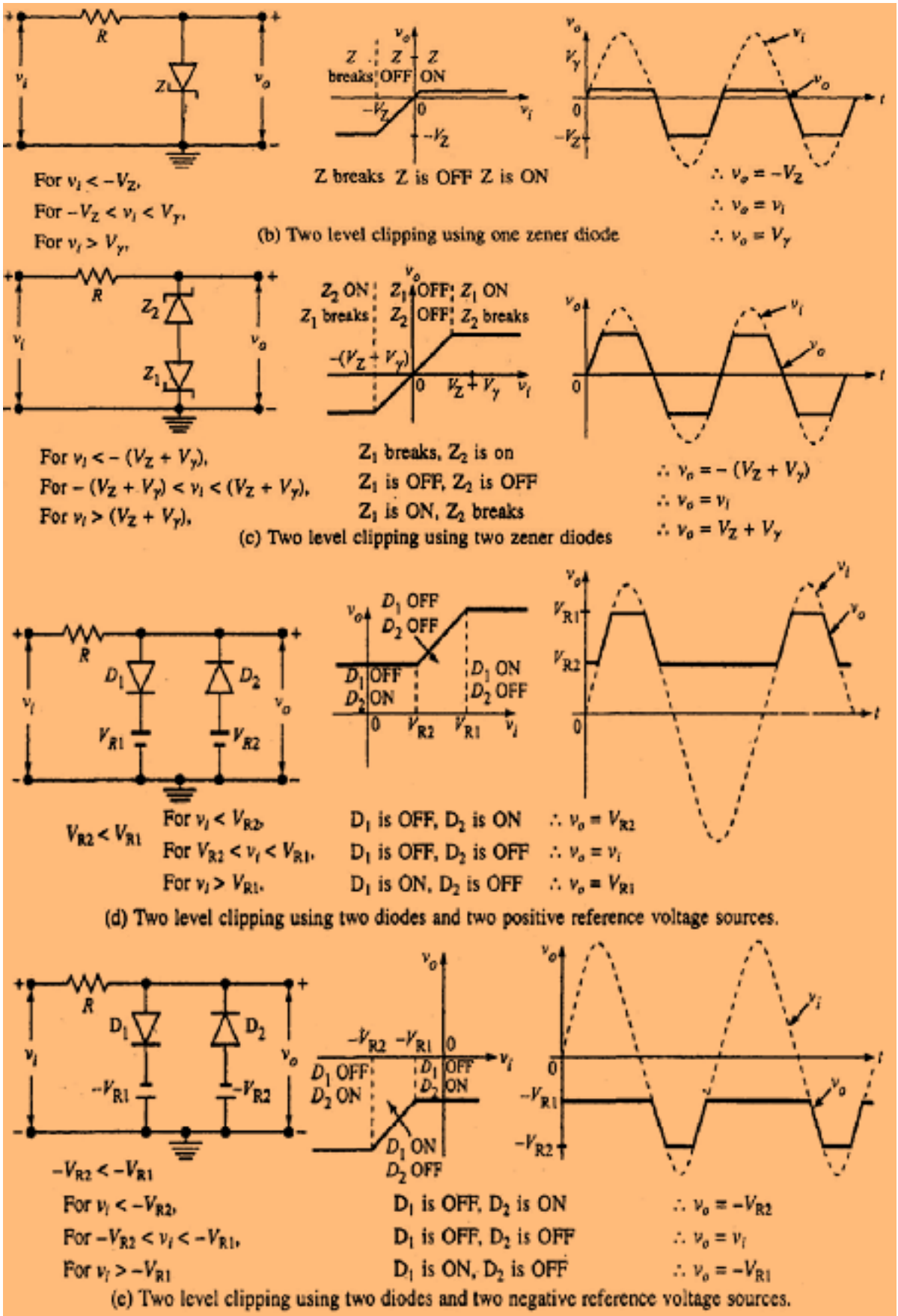
- The two level diode clipper shown in Figure 2.19 works as follows.
- For $v_i \geq V_{R1}$, DI is ON and D2 is OFF and the equivalent circuit shown in Figure 2.19(c) results. So the output $v_O = V_{R1}$ and the slope of the transfer characteristic is zero.

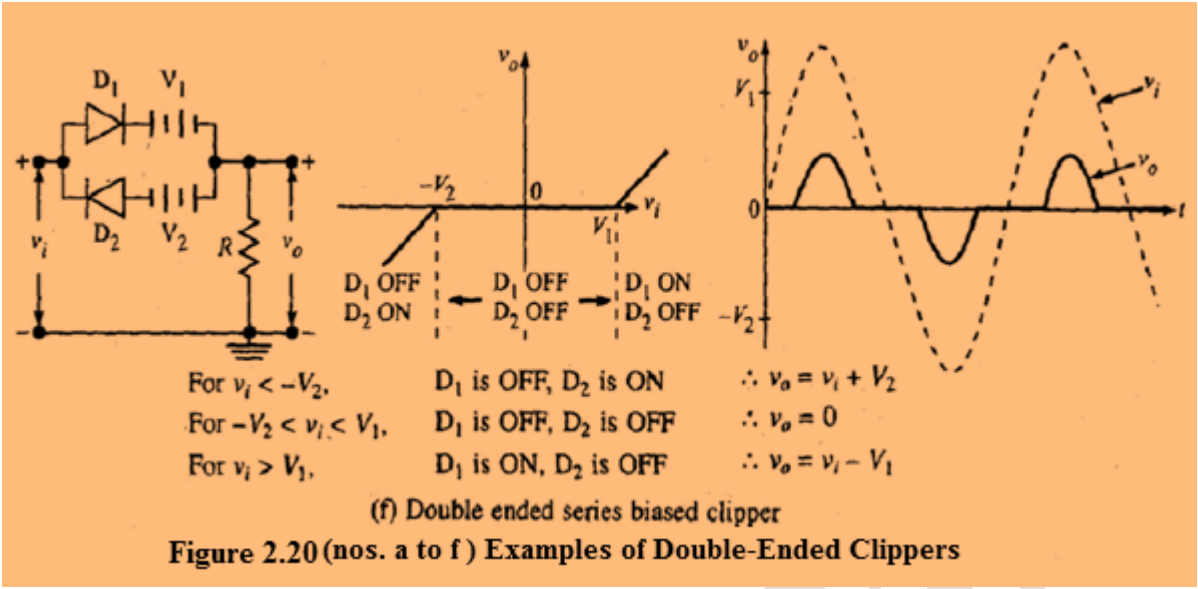
- For $v_i \le -V_{R2}$, DI is OFF and D2 is ON and the equivalent circuit shown in Figure 2.19(d) results. So the output $v_o = -V_{R2}$ and the slope of the transfer characteristic is zero.
- For $-V_{R2} < v_i < V_{R1}$, D1 is OFF and D2 is OFF and the equivalent circuit shown in Figure 2.19(e) results. So the output $v_o = v_i$ the slope of the transfer characteristic is one.
- The circuit of Figure 2.19 is called a slicer because the output contains a slice of the input between two reference levels V_{R1} and $-V_{R2}$.
- Looking at the input and output waveforms, we observe that this circuit may be used to convert a sine wave into a square wave, if $V_{R1} = -V_{R2}$ and if the amplitude of the input signal is very large compared with the difference in the reference levels, the output will be a symmetrical square wave.
- Two zener diodes in series opposing may also be used to form a double-ended clipper.
- If the diodes have identical characteristics, then, a symmetrical limiter is obtained.

2.18 Some Double-Ended Clipping Circuits: Some double-ended clippers, their transfer characteristics and the outputs for sine wave inputs are shown in Figure 2.20.



(a) Two level clipping using a zener diode


R
Z
v_i
v_o
Z breaks Z is OFF Z is ON
$-V_Z$
V_γ
For $v_i < -V_Z$, $\therefore v_o = -V_Z$
For $-V_Z < v_i < V_\gamma$, $\therefore v_o = v_i$
For $v_i > V_\gamma$, $\therefore v_o = V_\gamma$
(b) Two level clipping using one zener diode
Z_1
Z_2
Z_2 ON; Z_1 OFF; Z_1 ON
Z_1 breaks; Z_2 OFF; Z_2 breaks
$-(V_Z + V_\gamma)$
$V_Z + V_\gamma$
For $v_i < -(V_Z + V_\gamma)$, Z_1 breaks, Z_2 is on, $\therefore v_o = -(V_Z + V_\gamma)$
For $-(V_Z + V_\gamma) < v_i < (V_Z + V_\gamma)$, Z_1 is OFF, Z_2 is OFF, $\therefore v_o = v_i$
For $v_i > (V_Z + V_\gamma)$, Z_1 is ON, Z_2 breaks, $\therefore v_o = V_Z + V_\gamma$
(c) Two level clipping using two zener diodes
D_1
D_2
V_{R1}
V_{R2}
D_1 OFF
D_2 OFF
D_1 ON
D_2 OFF
D_1 OFF
D_2 ON
$V_{R2} < V_{R1}$
For $v_i < V_{R2}$, D_1 is OFF, D_2 is ON, $\therefore v_o = V_{R2}$
For $V_{R2} < v_i < V_{R1}$, D_1 is OFF, D_2 is OFF, $\therefore v_o = v_i$
For $v_i > V_{R1}$, D_1 is ON, D_2 is OFF, $\therefore v_o = V_{R1}$
(d) Two level clipping using two diodes and two positive reference voltage sources.
$-V_{R1}$
$-V_{R2}$
$-V_{R2} < -V_{R1}$
For $v_i < -V_{R2}$, D_1 is OFF, D_2 is ON, $\therefore v_o = -V_{R2}$
For $-V_{R2} < v_i < -V_{R1}$, D_1 is OFF, D_2 is OFF, $\therefore v_o = v_i$
For $v_i > -V_{R1}$, D_1 is ON, D_2 is OFF, $\therefore v_o = -V_{R1}$
(e) Two level clipping using two diodes and two negative reference voltage sources.



(f) Double ended series biased clipper

Figure 2.20 (nos. a to f) Examples of Double-Ended Clippers

2.19 Transistor Clippers:

- A nonlinear device is required for clipping purposes.
- A diode exhibits a nonlinearity, which occurs when it goes from OFF to ON.
- On the other hand, the transistor has two pronounced nonlinearities, which may be used for clipping purposes.
- One occurs when the transistor crosses from the cut-in region into the active region and the second occurs when the transistor crosses from the active region into the saturation region.
- A portion of the input waveform will be clipped at different levels, if the peak-to-peak value of the input waveform is such that it can carry the transistor across the boundary between the cut-in and active regions and across the boundary between the active and saturation regions.
- Normally, it is required that the portion of the input waveform, which keeps the transistor in the active region shall appear at the output without distortion.
- Hence, it is required that the input current rather than the input voltage be the waveform of the input signal.
- It is required because of that over a large signal excursion in the active region, the transistor output current responds nominally linearly to the input current but is related in a quite nonlinear manner to the input voltage. So, in transistor clippers a current drive needs to be used.

A transistor clipper is shown in Figure 2.21. The resistor *R* which represents either the signal source impedance or a resistor deliberately introduced must be large compared with the input resistance of the transistor in the active region. Under these circumstances, the input base current will very nearly have the waveform of the input voltage, because the base current is given $i_B = (v_i - V_\gamma)/R$

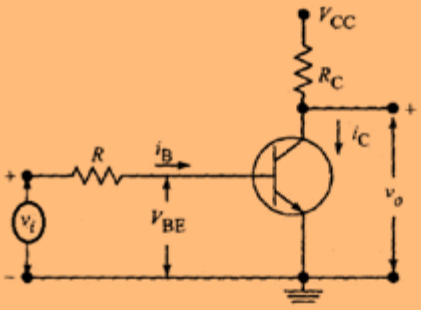


Figure 2.21 A Transistor Two Level Clipper

by where *Vr* is the base-to-emitter cut-in voltage. *Vr* = 0.1 V for Ge and *Vr* = 0.5 V for Si.

If a ramp input signal *vi* which starts at a voltage below cut-off and carries the transistor into saturation is applied, the base voltage, the base current, and the collector current waveforms of the transistor clipper will be as shown in Figure 2.22.

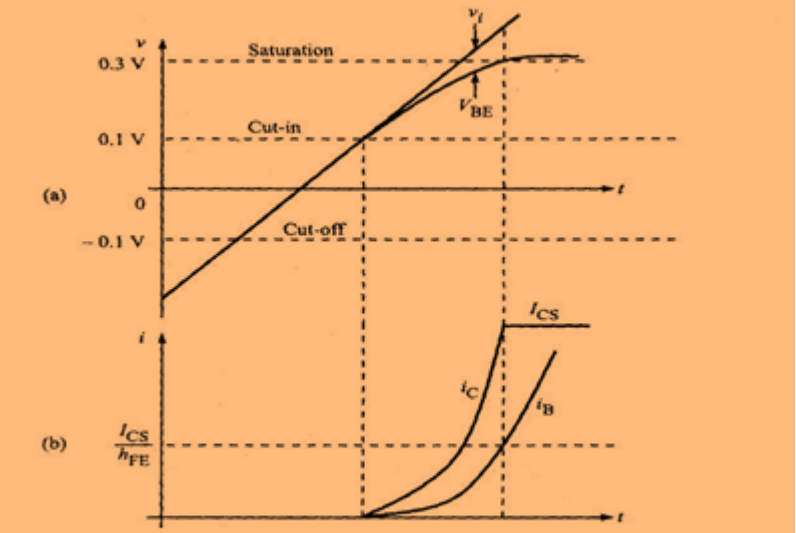


Figure 2.22 (a) wave forms the transistor clipper of Figure 2.21 voltage V_{BE} which results when a ramp input drives the Transistor fro cut-off into saturation and (b) The base and collector currents

- The waveforms which result when a sinusoidal voltage v_i, carries the transistor from cut-off to saturation are shown in Figure 2.23. The base circuit is biased so that cut-in occurs when *VBE* reaches the voltage *V*.

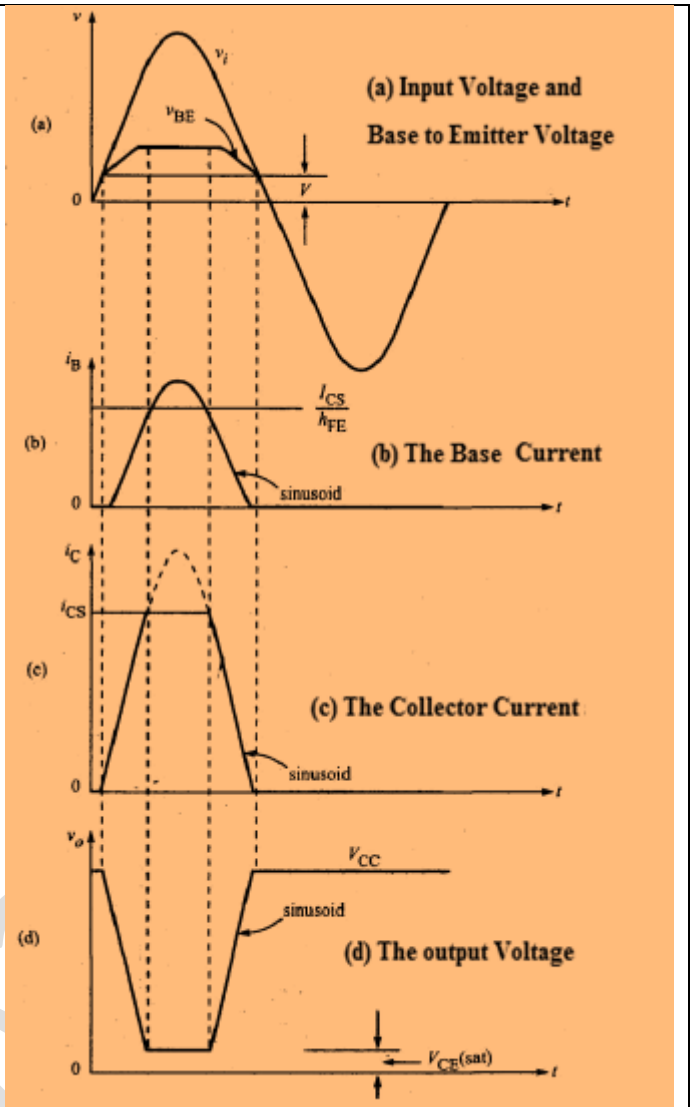


Figure 2.23 Wave forms of Transistor Clipper of Figure2.21

2.20 Two-Level Emitter-Coupled Transistor Clipper:

- The circuit shown in Figure 2.24 (a) is a two-level emitter-coupled transistor clipper. Let the input v_i to Q_1 be small enough ($< v_{i1}$) to keep Q_1 OFF.
- As a result of $I_{C1} \approx I_{E1} = 0$, if V_{BB} is adjusted such that Q_2 is in the active region, then the voltage $v_o = V_{CC} - I_{C2} R_C$.
- When v_i is increased further so that Q_1 conducts, there is I_{E1} through *Re*, the drop across *Re* increases which in turn reduces I_{B2} of Q_2 resulting in reduction of I_{C2}. Consequently v_o increases.
- When v_i is increased further, v_o also rises. Thus, the output is proportional to the input in a limited region.

- A further increase in v_i to v_{i2} enables Q_1 to draw reasonably large I_{E1} and the drop across *Re* can now reverse-bias the base−emitter diode of Q_2, thereby driving Q_2 into the OFF state. As a result, v_o is limited to V_{CC}.
- The transfer characteristic with input and output waveforms is shown in Figure 2.24 (b). Thus, this circuit behaves as a two-level clipper (slicer).
- The region of linearity can be controlled by the choice of V_{BB}.

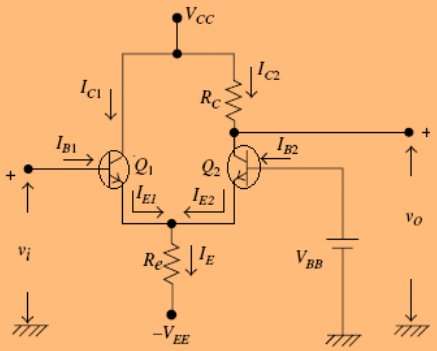


Figure 2.24 (a) A two-level transistor clipper

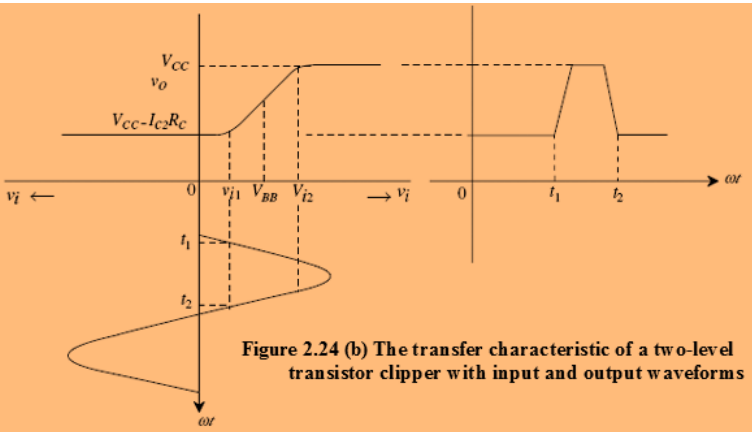
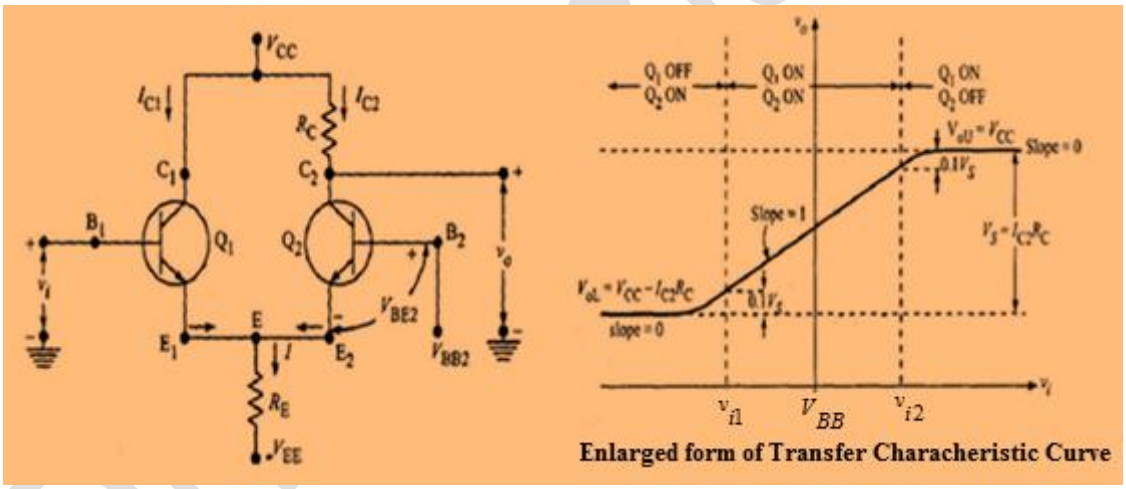


Figure 2.24 (b) The transfer characteristic of a two-level transistor clipper with input and output waveforms



Enlarged form of Transfer Characheristic Curve

2.21 Emitter-Coupled Clipper:

An emitter-coupled clipper is shown in Figure 2.25(a). It is a two-level clipper using transistors. The base of Q2 is fixed at a voltage V_{BB2}, and the input is applied to B1. If initially the input is negative, Q1 is OFF and only Q2 carries the current. Assume that V_{BB2} has been adjusted so that Q2 operates in its active region. Let us assume that the current I_E in the emitter resistance is constant. This is valid if V_{BE2} is small compared to VBB2 + VEE When *vi* is below the cut-off point of Q1, all the current I flows through Q2. As *vi*, increases, Q1 will eventually come out of cut-off, both the transistors will be carrying currents but the current in Q2 decreases while the current in Q1 increases, the sum of the currents in the two transistors remaining constant and equal to I. The input signal appears at the output, amplified but not inverted. As *vi* continues to increase, the common emitter will follow the base of Q1.

Since the base of Q2 is fixed, a point will be reached when the rising emitter voltage cuts off Q2. Thus, the input signal is amplified but twice limited, once by the cutoff of Q1 and once by the onset of cut-off in Q2. The total range *Avo*, over which the output can follow the input is VE and is constant and therefore adjustable through an adjustment of I. The absolute voltage of the portion of the input waveform selected for transmission may be selected through an adjustment of a biasing voltage on which *vi* is superimposed or through an adjustment of V_{BB2}. The total range of input voltage Δv_i, between the clipping limits is Δv_0 /*A*, where *A* is the gain of the amplifier stage. Figure 2.25(b) shows the transfer characteristic of an emitter-coupled clipper.

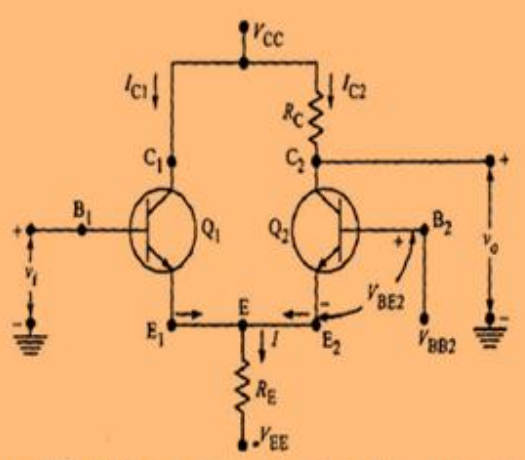


Figure 2.25 (a) An Emitter-Coupled Clipper(Double Clipper)

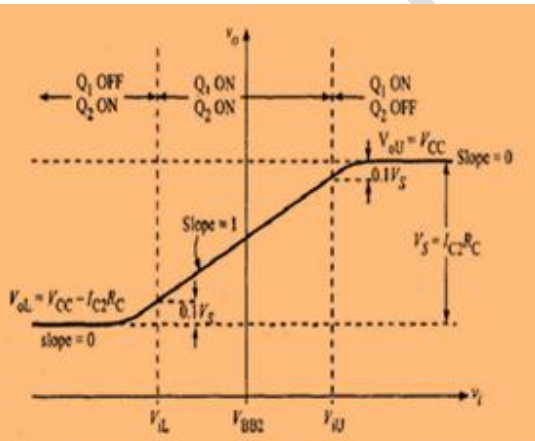


Figure 2.25(b) Transfer Charecteristics of the Emitter-Coupled Clipper

2.22 Comparators:

A comparator circuit is one, which may be used to mark the instant when an arbitrary waveform attains some particular reference level. The nonlinear circuits, which can be used to perform the operation of clipping, may also be used to perform the operation of comparison. In fact, the clipping circuits become elements of a comparator system and are usually simply referred to as comparators. The distinction between comparator circuits and the clipping circuits is that, in a comparator there is 'no interest in reproducing any part of the signal waveform, whereas in a clipping circuit, part of the signal waveform is needed to be reproduced without any distortion.

An amplitude comparator is a circuit that tells the time instant at which the input amplitude has reached a reference level. A comparator is shown in Figure 2.26

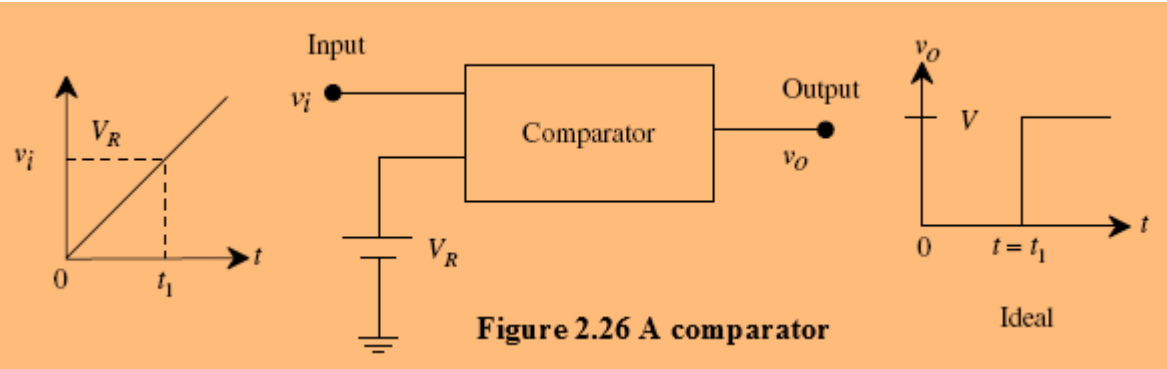


Figure 2.26 A comparator

Ideally, in this comparator:

$V_O = 0$ for $t < t_1$, $v_O = V$ for $t \geq t_1$

The amplitude of the output abruptly rises from 0 to V at $t = t_1$, t_1 is the time instant at which v_i reaches V_R .

2.23 Diode Comparators:

There are two types of diode comparators. 1. Pick-off and 2. Break-away diode comparators.

2.23.1 Pick-off Diode Comparators:

A simple diode comparator circuit is shown in Figure 2.27. A base clipper is used as a comparator. The input now is a ramp and V_R is the reference voltage. The circuit is required to tell the time instant at which the input reaches V_R.

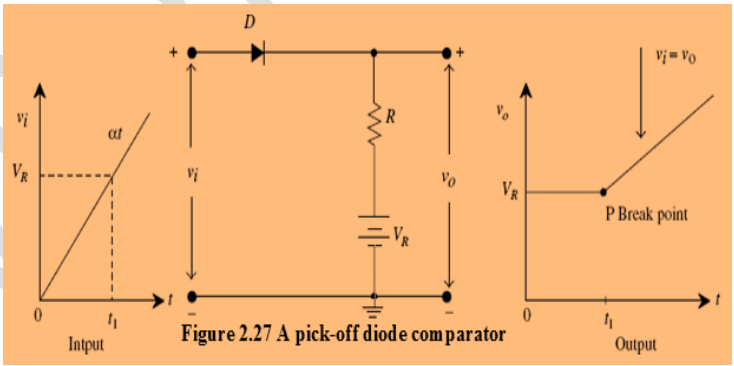


Figure 2.27 A pick-off diode comparator

Using an ideal diode, as long as, $v_i < V_R$, $v_O = V_R$. If $v_i \geq V_R$, $v_O = v_i$. Up to $t = t_1$, $v_O = V_R$ and the slope of the output is 0. At $t = t_1$, output suddenly rises as the input (the slope at the output has changed) and this is the time instant at which the input reaches the reference level V_R. The point P where the slope changes when the diode conducts is called the break point. The diode in this case is called a "pick-off" diode.

As is evident from the Figure 2.27, there is a sudden change in the slope of the output at the instant the input reaches V_R . However, due to ageing and temperature variations, the diode may not switch from OFF to ON at exactly $t = t_1$ (break point, P). It may switch state at any instant after t_1 and before t_2 (see Figure 2.28).

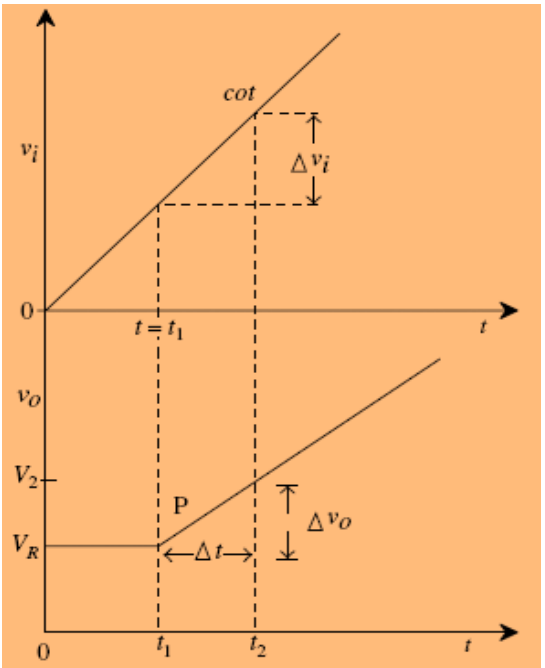


Figure 2.28 The input and output of the diode comparator

Hence, the break point (the point at which the device *D* changes state) may not exactly be at t_1. Instead, there is a break region (t_1 to t_2), within which, at any instant the device may switch state. Therefore, there is a large region of uncertainty. After the break point, the output follows the input—it has the same slope as the input. If this region of uncertainty is to be reduced to know precisely at which time instant the input reaches the reference level, the break region should be sharp. To achieve this, an amplifier may be placed before or after the comparator.

Consider the response of the comparator circuit shown in Figure 2.27. To the left of the break point, the diode is OFF. Hence, the reverse incremental resistance of the diode is significantly larger when compared to *R*. To the right of the break point, the forward incremental resistance of the diode is much smaller than *R*. If the break point is located at a point where the incremental resistance of the diode (Δr) is equal to the resistance (R) then the incremental change in the output voltage (Δv_O) for a corresponding change at the input (Δv_i) is calculated using Figure 2.29.

$$\Delta v_O = \Delta v_i \frac{R}{r+R}. \quad \text{If r = R}$$

$$\frac{\Delta v_o}{\Delta v_i} = \frac{R}{R+R} = \frac{1}{2} \text{----------2.11}$$

This relation tells that $\Delta vi = 2\Delta vo$. That is, for a larger incremental change in the input, there is a smaller incremental change in the output. The region of uncertainty is larger.

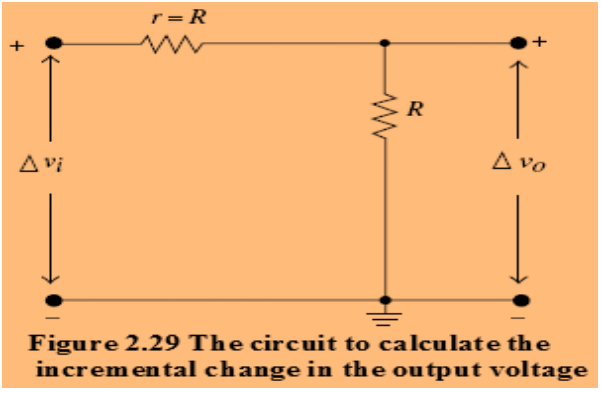


Figure 2.29 The circuit to calculate the incremental change in the output voltage

A device is connected at the output of the comparator, and is required to be activated when the diode current is say, *I* and has a drop across *R* as *I*R*. If, now an amplifier is connected at the output of the comparator to reduce the region of uncertainty, the output of this amplifier activates the device (see Figure 2.30(a)). Let the amplifier have a gain *A*. During $\Delta t = t_2 - t_1$, the output changes by $\Delta vo = V_2 - V_R$, see Figure 2.28, the delay in the response is reduced to $\Delta t/A$ or $(t_2 - t_1) / A$.

Let the amplifier only amplify the change in the comparator input but not the reference voltage. The device to be activated is activated only when the drop across R is $I*R$. However, now $I = I/A$. Hence, the device is activated when the drop across R is $R*I/A$ since the diode current is amplified by A and the dynamic diode resistance, $r = (\eta\ V_T / I)$, varies inversely with current. Therefore, it is evident that, the device to be activated by the comparator will respond at a current corresponding to $r = R*A$.

$$\frac{\Delta v_o}{\Delta v_i} = A\frac{R}{r+R} = \frac{AR}{R+RA} = \frac{A}{1+A}$$

$$As\ \ A \to \infty,\ \frac{\Delta v_o}{\Delta v_i} \to 1 \text{----------2.12}$$

Without an amplifier, $\Delta v_O/\Delta v_i$ (the transmission gain) was half and with an amplifier connected as in Figure 2.30(a), $\Delta v_O/\Delta v_i$ is one; i.e., there is no marked improvement in the response of the comparator arrangement of Figure 2.30(b).

Now, consider a comparator circuit where the amplifier precedes a comparator and the output of the comparator is directly connected to the device to be actuated. Let the amplifier have a gain A and Δv_i be the incremental change in the input needed to actuate the device when the output is directly connected to the device. With a pre-amplifier with gain A connected to the comparator, $\Delta v_i /A$ is now the incremental change in the input needed to make the output change as in the previous case. As $\Delta v_i /A$ is small, the break region is reduced. Thus, this is a better comparator.

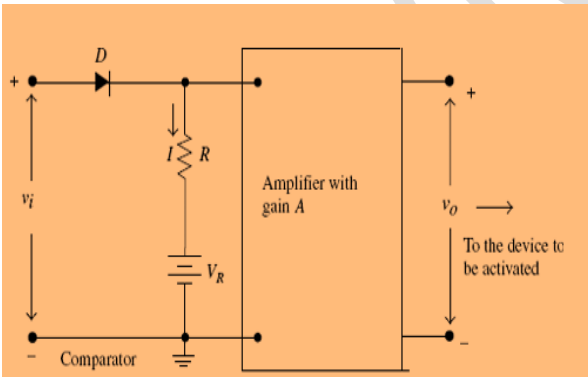


Figure 2.30 (a) The output of the comparator connected to an amplifier

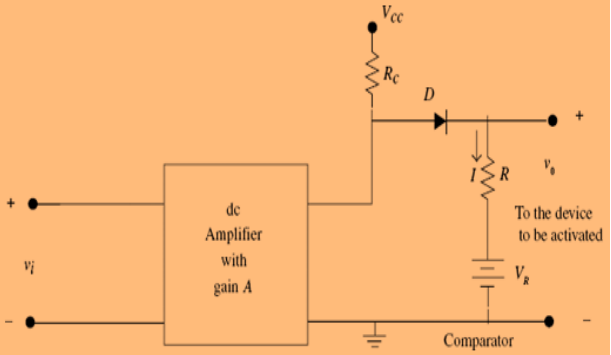


Figure 2.30 (b) The output of the amplifier drives a comparator

2.23.2 Diode Comparator:

Figure 2.31 shows the circuit diagram of a diode comparator. As long as the input voltage v_i is less than the reference voltage V_R, the diode D is ON and the output is fixed at VR. When $v_i > V_R$, the diode is OFF and hence $v0 = vi$. The break occurs at $v_i = V_R$ at time $t = t_1$. So, this circuit can be used to mark the instant at which the input voltage reaches a particular reference level V_R.

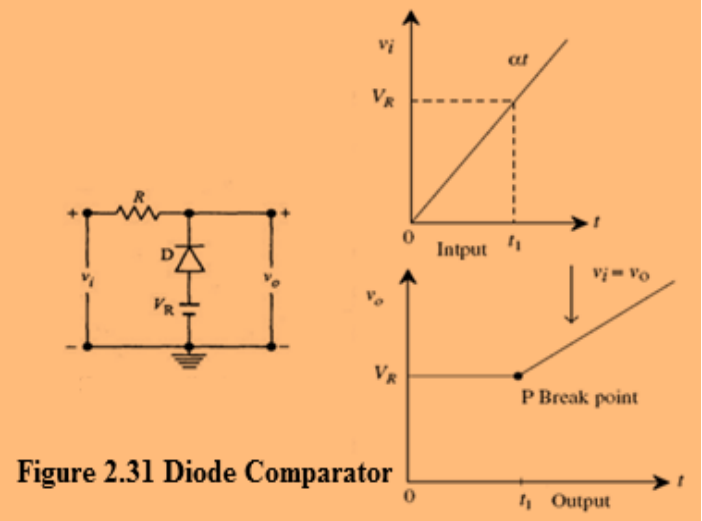


Figure 2.31 Diode Comparator

Comparators may be non-regenerative or regenerative. Clipping circuits fall into the category of non-regenerative comparators. In regenerative comparators, positive feedback is employed to obtain an infinite forward gain (unity loop gain). The Schmitt trigger and the blocking oscillator are examples of regenerative comparators. The Schmitt trigger comparator generates approximately a step input. The blocking oscillator comparator generates a pulse rather than a step output waveform. Most applications of comparators make use of the step or pulse natures of the input. Operational amplifiers and tunnel diodes may also be used as comparators.

2.24 Applications of Voltage Comparators:

Apart from being used as amplitude comparators, comparator circuits can be used for many applications. A few applications are presented in this section.

Voltage comparators may be used:

1) In accurate time measurements, 2) In pulse time modulation, 3) As timing markers generated from a sine wave, 4) In phase meters, 5) In amplitude distribution analyzers 6) To obtain square wave from a sine wave, and 7) In analog-to-digital converters.

2.24.1. Measurement of time delays: In the comparator shown before, if V_{R1} is the reference level in the first comparator (double differentiator), then a pulse is generated with a peak at $t = t1$. If V_{R2} is the reference level set in a second comparator then the pulse is generated with peak at $t = t2$. Then the time difference between the two pulses is $(t2 - t1) = (V_{R2} - V_{R1}) / \alpha$ where, α is the slope of the input ramp.

2.24.2. Timing markers generated from a sine wave:

If a sine wave is applied as input, when the input reaches V_R , the output of the comparator is high till the input reaches V_R again. After differentiating and clipping negative spikes, we get positive spikes which can be implemented as timing markers, as shown in Figure 2.32.

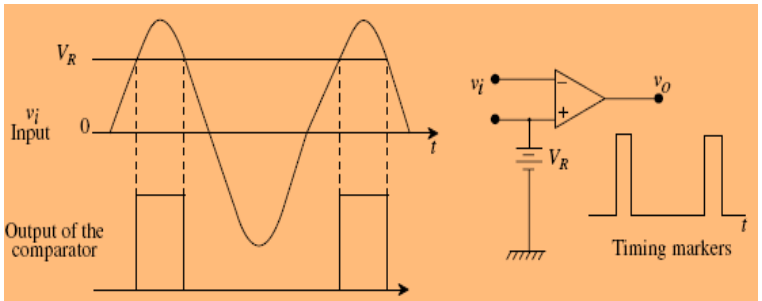


Figure 2.32 Comparator used to generate timing markers

2.24.3. Phase meter:

Let two sinusoidal inputs having a phase difference be applied to a comparator whose reference voltage is zero, as shown in Figure 2.33. Here, the output pulses are differentiated and the time difference between the output spikes is proportional to the phase difference.

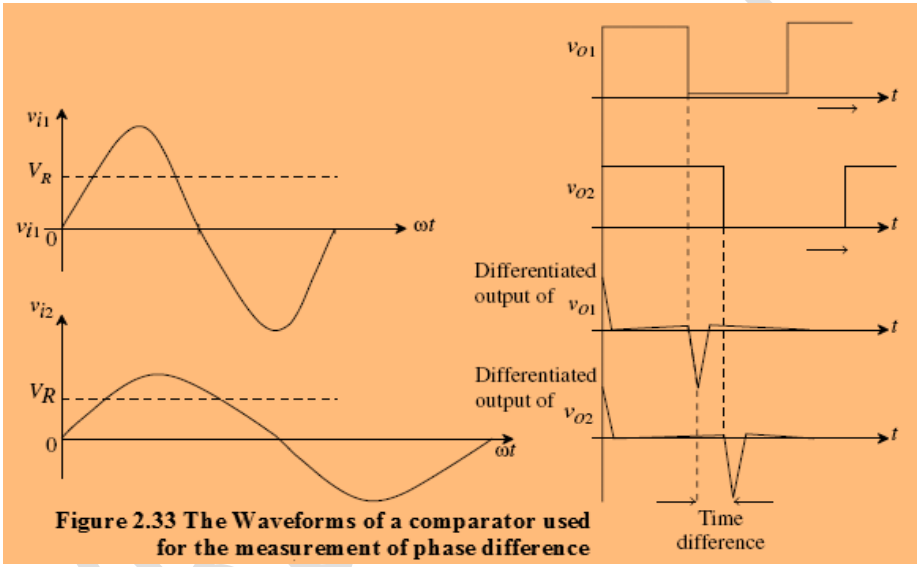


Figure 2.33 The Waveforms of a comparator used for the measurement of phase difference

2.24.4. Square waves from sine waves:

In a regenerative comparator (Schmitt trigger), as long as *vi* is less than *Vref*, *vo* is the same as *vi*, as shown in Figure 2.34. If the input goes beyond ± *Vref*, the output of the comparator remains at either $+V$ or $-V$, thereby converting a sinusoidal input into a square-wave output, when the frequency is sufficiently large.

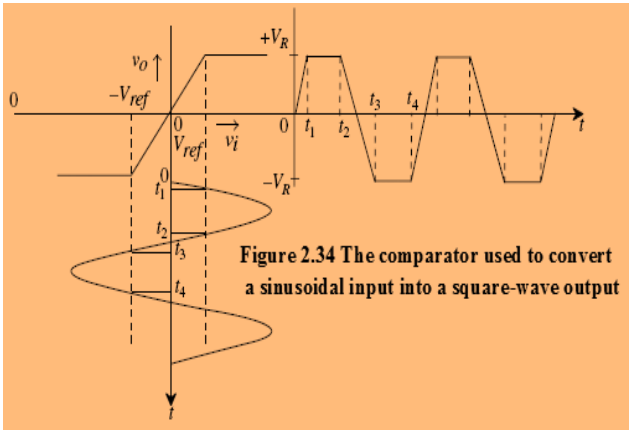


Figure 2.34 The comparator used to convert a sinusoidal input into a square-wave output

2.25 Clamping Circuits:

Clamping circuits which are used to clamp or fix the extremity of a periodic waveform to some constant reference Voltage level V_R. Under steady-state conditions, these circuits restrain the extremity of the waveform from going beyond V_R. Clamping circuits may be one-way clamps or two-way clamps. When only one diode is used and a voltage change in only one direction is restrained, the circuits are called one-way clamps. When two diodes are used

and the voltage change in both the directions is restrained, the circuits are called two-way clamps.

2.26 The Clamping Operation:

When a signal is transmitted through a capacitive coupling network *(RC* high-pass circuit), it looses its dc component, and a clamping circuit may be used to introduce a dc component by fixing the positive or negative extremity of that waveform to some reference level. For this reason, the clamping circuit is often referred to as *dc restorer* or *dc reinserter.* In fact, it should be called a *dc inserter,* because the dc component introduced may be different from the dc component lost during transmission. The clamping circuit only changes the dc level of the input signal. It does not affect its shape

2.27 Classification of Clamping Circuits:

Basically clamping circuits are of two types: (1) positive-voltage clamping circuits and (2) negative-voltage clamping circuits.

In positive clamping, the negative extremity of the waveform is fixed at the reference level and the entire waveform appears above the reference level, i.e. the output waveform is positively clamped with reference to the reference level. In negative clamping, the positive extremity of the waveform is fixed at the reference level and the entire waveform appears below the reference, i.e. the output waveform is negatively clamped with respect to the reference level. The capacitors are essential in clamping circuits. The difference between the clipping and clamping circuits is that while the clipper clipps off an unwanted portion of the input waveform, the clamper simply clamps the maximum positive or negative peak of the waveform to a desired level. There will be no distortion of waveform.

2.28 The Negative Clamping Circuit:

The clamping circuit essentially consists of an input source, a capacitor of a suitable value and a diode connected in shunt with the output terminals. This clamps the positive peak of the input signal (sinusoidal, in this case) to the zero level. The diode is assumed to be ideal and initially there is no charge on the condenser. *vA* is the charge built up on the condenser, *C*. Figure 2.35 shows a basic clamping circuit.

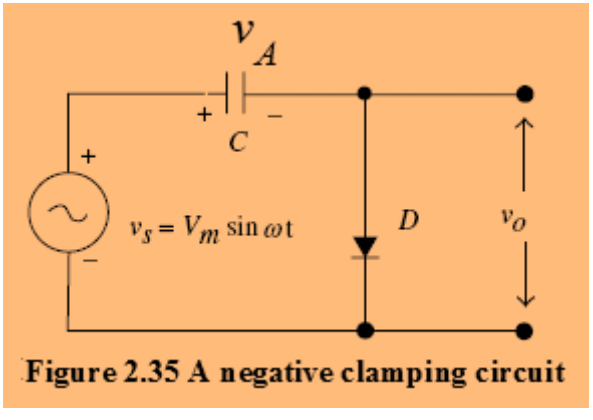


Figure 2.35 A negative clamping circuit

As the input rises from 0 to V_m in the first quarter cycle, D conducts [see Figures 2.35 (a) and 2.36 (a)], C charges to V_m. During this period, $v_O = 0$ if the diode is ideal. The input falls

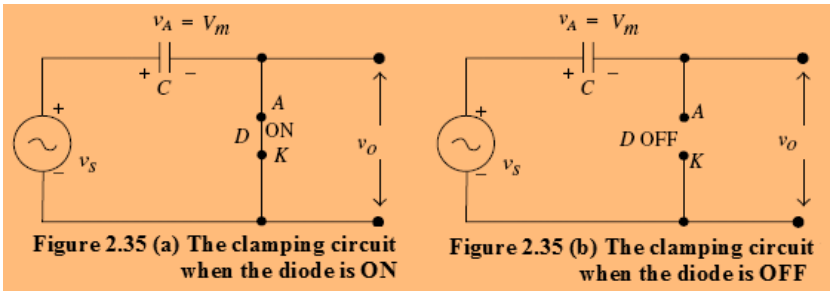


Figure 2.35 (a) The clamping circuit when the diode is ON

Figure 2.35 (b) The clamping circuit when the diode is OFF

after the first quarter cycle. $v_S < V_m$, where V_m is the charge on the condenser. As a result, the diode is reverse-biased by a voltage ($v_S - V_m$). Hence, D is OFF, as shown in Figure 2.35(b).

Thus, the voltage across C remains unchanged. The output voltage is given by

$$V_O = V_S - V_A = V_S - V_m \text{----------2.13}$$

From Eq. (2.13) at $v_S = 0$, $v_O = -V_m$. And if, $v_S = -V_m$, $v_O = -V_m - V_m = -2\ V_m$ and at $v_S = V_m$, $v_O = v_m - V_m = 0$

During the next cycle, the positive peak of the output just reaches the zero level. Hence, in the output, the positive peak is clamped to the zero level. To clamp the positive peak to zero, a negative dc voltage is introduced in this circuit. Therefore, this circuit is called a negative clamp.

Negative Clamper Operation:

- Figure 2.36 (a) shows the circuit diagram of a basic negative clamper. It is also termed a positive peak clamper since the circuit clamps the positive peak of a signal to zero level.
- Assume that the signal source has negligible output impedance and that the diode is ideal, $R_f = 0$ and $V_r = 0$ V in that, it exhibits an arbitrarily sharp break at 0 V, and that its input signal shown in Figure 2.36 (b) is a sinusoid which begins at $t = 0$. Let the capacitor C be uncharged at $t = 0$.

During the first quarter cycle, the input signal rises from zero to the maximum value. The diode conducts during this time and since we have assumed an ideal diode, the voltage across it is zero. The capacitor C is charged through the series combination of the signal source and the diode and the voltage across C rises sinusoidally.At -the end of the first quarter cycle, the voltage across the capacitor, $v_C = V_m$ .When, after the first quarter cycle, the peak has been passed and the input signal begins to fall, the voltage v_C across the capacitor is no longer able to follow the input, because there is no path for the capacitor to discharge as now diode is OFF.

- Hence, the voltage across the capacitor remains constant at $v_C = V_m$, and the charged capacitor acts as a voltage source of V volts and after the first quarter cycle and the output is given by $v_O = v_i - V_m$.
- During the succeeding cycles, the positive extremity of the signal will be *clamped* or *restored* to zero .

- The output for $v_i = 0$, $v_o = -V_m$, for $v_i = V_m$, $v_0 = 0$, and for $v_i = -V_m, v_0 = -2\ V_m$.
- The waveform is shown in Figure 2.36 (c) results.

At -the end of the first quarter cycle, the voltage across the capacitor, $v_C = V_m$ .When, after the first quarter cycle, the peak has been passed and the input signal begins to fall, the voltage v_C across the capacitor is no longer able to follow the input, because there is no path for the capacitor to discharge. Hence, the voltage across the capacitor remains constant at $v_C = V_m$, and the charged capacitor acts as a voltage source of V volts and after the first quarter cycle, the output is given by $v_O = v_i - V_m$.

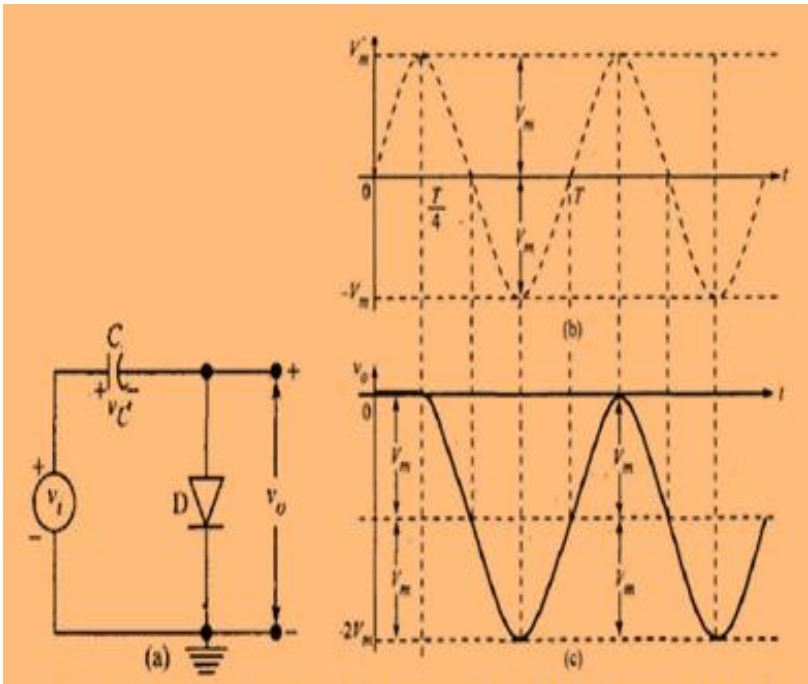


Figure 2.36 (a) A Negative Clamping Circuit (b) A Sinusoidal Input and (c) A Steady-State Clamped Output

During the succeeding cycles, the positive extremity of the signal will be *clamped* or *restored* to zero and the output for $v_i = 0$,

$v_o = -V_m$, for $v_i = V_m$, $v_0 = 0$, and for $v_i = -V_m, v_0 = -2\ V_m$. Waveform is shown in Figure 2.36 (c) results.

Suppose that after the steady-state condition has been reached, the amplitude of the input signal is increased, then the diode will again conduct for at most one quarter cycle and the dc voltage across the capacitor would rise to the new peak value, and the positive excursions of the signal would be again restored to zero.

Suppose the amplitude of the input signal is decreased after the steady-state condition has been reached. There is no path for the capacitor to discharge.

To permit the voltage across the capacitor to decrease, it is necessary to shunt a resistor across *C*, or equivalently to shunt a resistor across D.

In the latter case, the capacitor will discharge through the series combination of the resistor *R* across the diode and the resistance of the source, and in a few cycles the positive extremity would be again clamped at zero as shown in Figure 2.37(b). A circuit with such a resistor *R* is shown in Figure 2.37(a).

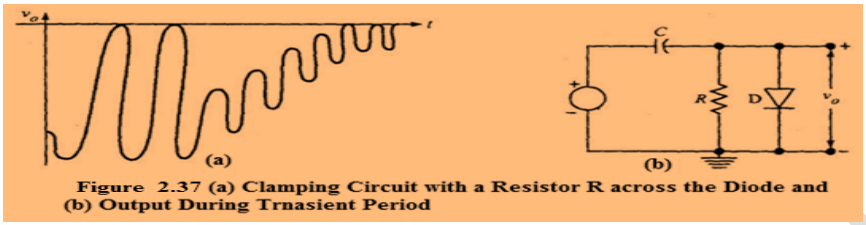


Figure 2.37 (a) Clamping Circuit with a Resistor R across the Diode and (b) Output During Trnasient Period

Alternatively, if a positive dc voltage is inserted by the clamping circuit so that the negative peak of the input signal is clamped to the zero level then the circuit is called a positive clamp [see Figure 2.38(b)].

The input to this circuit in Figure 2.38(b) is a sinusoidal waveform with zero reference level.

The output is referenced to *+Vm* and the negative peak is clamped to zero. The input and output waveforms of negative and positive clamp circuits are represented in Figures 2.38(a) and 2.38(b), respectively.

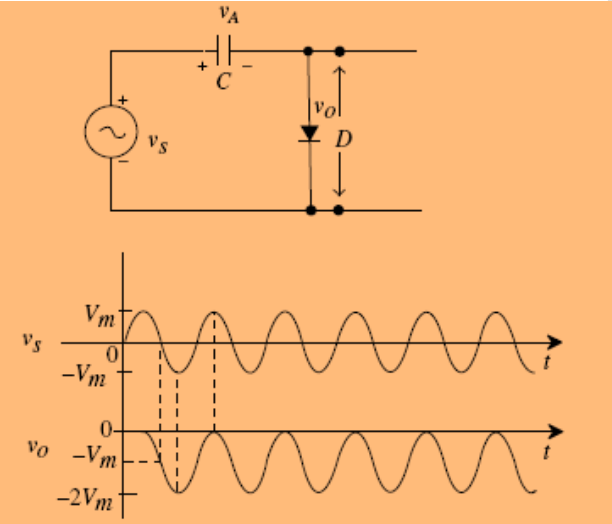


Figure 2.38 (a) The circuit, input and output waveforms of a negative clamp

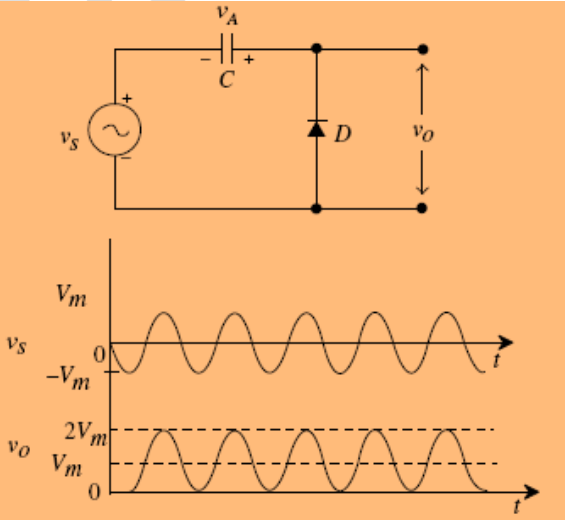


Figure 2.38 (b) The circuit, input and output waveforms of a positive clamp

2.29 The Clamping Circuit for Varying Input Amplitude:

The amplitude of the input signal may either increase or decrease for various reasons.

Suppose that after the steady-state condition has been reached, if the amplitude of the input increases at $t = t_1$ [see Figure 2.39(a)], then the diode will again conduct for at most one quarter cycle and the dc voltage across the capacitor would rise to the new peak value, and the positive excursions of the signal would be again restored to zero. The output is zero for this period. Subsequently, the positive peak of the output remains clamped to zero, as shown

in Figure 2.39 (b). Obviously, this simple clamping circuit can clamp the output to zero, even if the input increases. However, the output is distorted for a quarter of a cycle.

In our description of the clamping circuit in the previous section, a steady input signal was assumed; which is always not the case. The amplitude of the input signal may either increase or decrease for various reasons. So, what is the effect of this variation on the output? To answer this question, let us analyses the behavior of the circuit under the two possible conditions: increase in amplitude and decrease in amplitude.

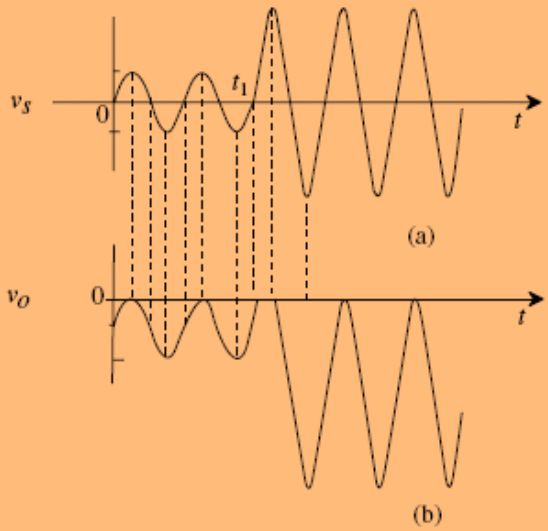


Figure 2.39 (a) The amplitude of the input increases at *t*1; (b) the output is once again clamped to zero in a quarter cycle

If the amplitude of the input increases at $t = t1$ [see Figure 2.39(a)], once again the diode *D* conducts for a quarter cycle. The output is zero for this period. Subsequently, the positive peak of the output remains clamped to zero, as shown in Figure 2.39 (b). Obviously, this simple clamping circuit can clamp the output to zero, even if the input increases. However, the output is distorted for a quarter of a cycle.

However, this clamping circuit cannot handle an input signal with decreasing amplitude. When the amplitude of the input signal decreases, the voltage across the capacitor should change to the peak amplitude of the new input so as to clamp the positive peak to the zero level. In this circuit, there is no path for the charge on the capacitor to discharge.

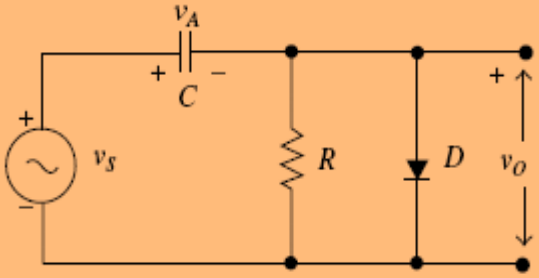


Figure 2.40 (a) The clamping circuit with a resistance shunted across the diode

- Suppose the amplitude of the input signal is decreased after the steady-state condition has been reached. There is no path for the capacitor to discharge.
- To permit the voltage across the capacitor to decrease, it is necessary to shunt a resistor across *C*, or equivalently to shunt a resistor across D.
- In the latter case, the capacitor will discharge through the series combination of the resistor *R* across the diode and the resistance of the source, and in a few cycles the positive extremity would be again clamped at zero as shown in Figure 2.37(b). A circuit with such a resistor *R* is shown in Figure 2.37(a).

- Suppose the amplitude of the input signal is decreased after the steady-state condition has been reached. There is no path for the capacitor to discharge.

Suppose the amplitude of the input signal is decreased after the steady-state condition has been reached. The voltage across the capacitor should change to the peak amplitude of the new input so as to clamp the positive peak to the zero level.

In this circuit, there is no path for the charge on the capacitor to discharge. To facilitate the discharge of the condenser, a resistance R is introduced in shunt with the diode D, as shown in Figure 2.38(a).

It is seen from Figures 2.38 (b) (i) and (ii), at $t = t_1$, if the input amplitude is abruptly reduced, as the voltage across the capacitor cannot change instantaneously, the positive peaks will not reach the zero level.

However, as the capacitor discharges, the voltage across the capacitor varies exponentially with a time constant, $\tau = RC$.

The output reaches the zero level at $t = t_2$, and the positive peak is again clamped to zero after a few cycles [see Figure 2.38 (b) (iii)].

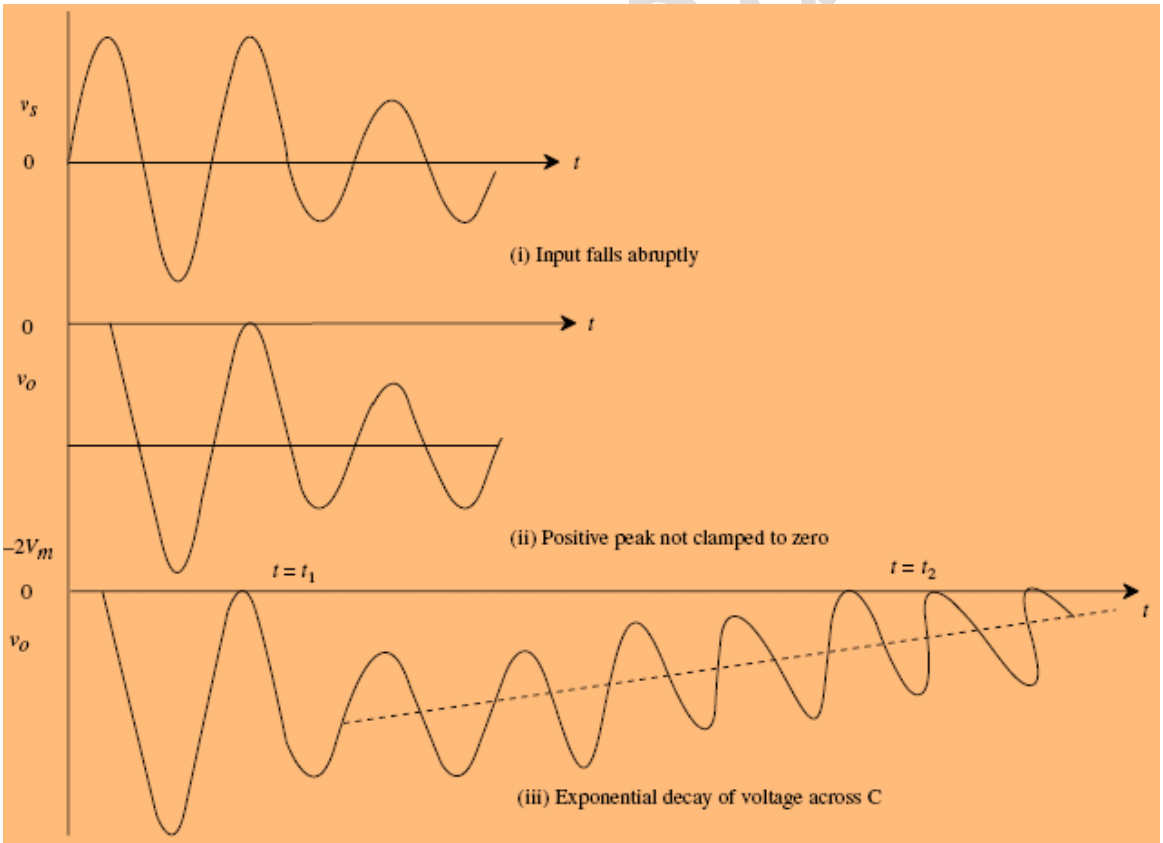


Figure 2.40 (b) (i) The input when the amplitude decreases at $t = t1$; (ii) the output when $R = 8$; and (iii) the output with finite R

Let us examine the situation in detail, when the positive peak is clamped to zero as shown in Figure 2.41.

In the proximity of a positive peak, *D* conducts and at *t* = , *vo* = 0. In the absence of the diode, the output should have followed the dashed line with the peak at *t* = *t*2. However, because of the diode, the output is zero from to *t*2; and in the subsequent cycles the positive peaks of the sinusoidal waveform are clamped to zero. Although, for a small duration between and *t*2, the output is different from the variation of a sinusoidal signal, i.e., there is a distortion. If the distortion is to be minimized, the capacitor must not lose an appreciable charge in one cycle. For this, the time constant has to be very large as compared to the time period of the input signal.

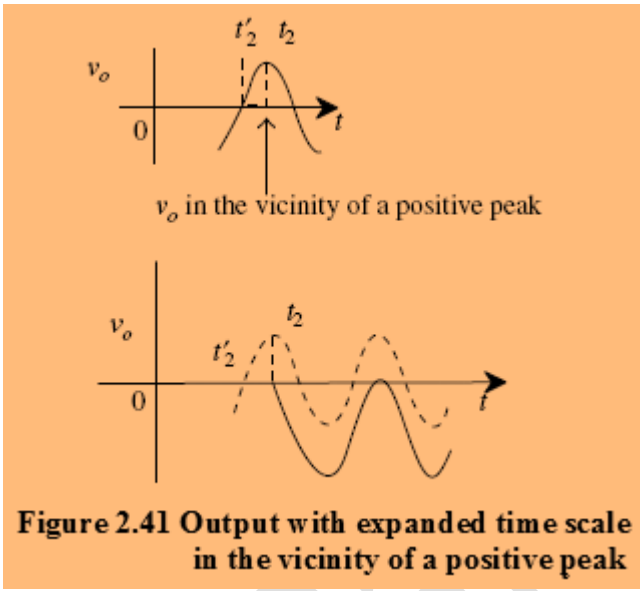


Figure 2.41 Output with expanded time scale in the vicinity of a positive peak

2.30 Positive Clamper:

- Figure 2.42(a) shows a positive clamper also termed as negative peak clamper since this circuit clamps the negative peaks of a signal to zero level.
- The negative peak clamper, i.e. the positive clamper introduces a positive dc. Let the input voltage be $v_i = V_m \sin\omega t$ as shown in Figure 2.42(b).
- When v_i goes negative, the diode gets forward biased and conducts and in a few cycles the capacitor gets charged to V_m with the polarity shown in Figure 2.42(a). Under steady-state conditions, the capacitor acts as a constant voltage source and the output is
- $v_O = v_i - (-V_m) = v_i + V_m$.----------2.14

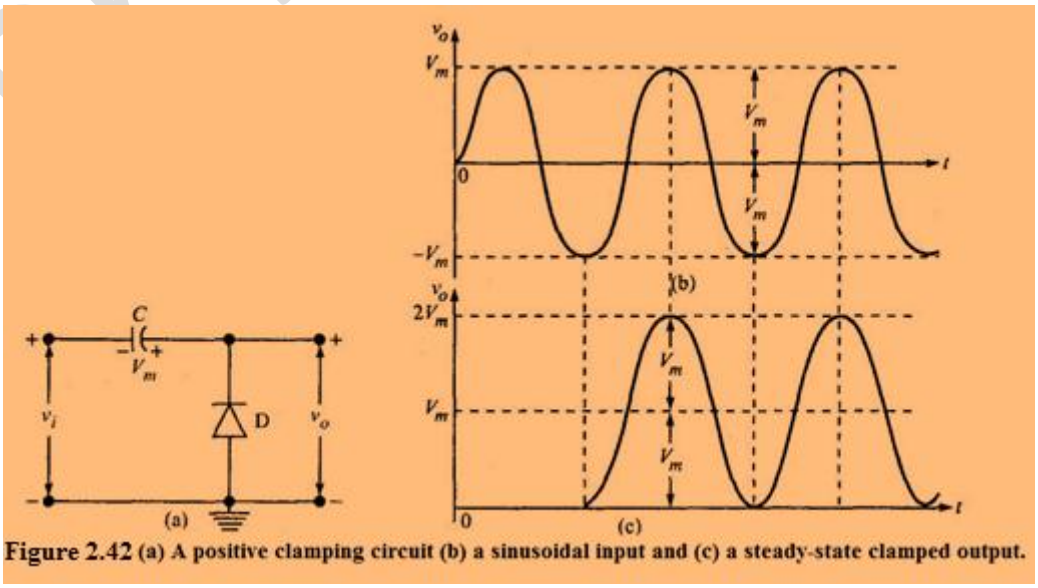


Figure 2.42 (a) A positive clamping circuit (b) a sinusoidal input and (c) a steady-state clamped output.

Based on the above relation between *vo* and v_i, the output voltage waveform is plotted.

- As seen in Figure 2.42(c) the negative peaks of the input signal are clamped to zero level.
- The peak-to-peak value of output voltage is equal to the peak-to-peak value of input voltage $v_i = 2V_m$.
- There is no distortion of waveform. To accommodate for variations in amplitude of input, the diode D is shunted with a resistor as shown in Figure 2.43(a).
- When the amplitude of the input waveform is reduced, the output will adjust to its new value as shown in Figure 2.43(b).

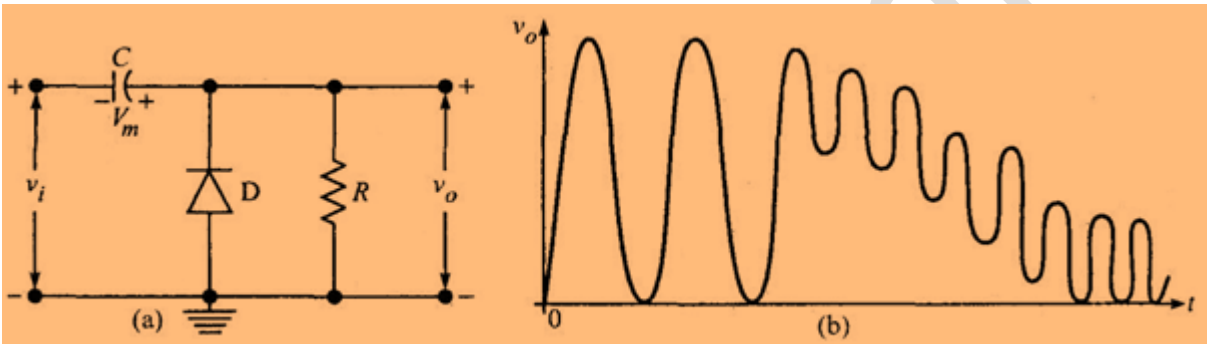


Figure 2.43 (a) Clamping circuit with a resistor R across D and (b) output during transient period.

2.31 Clamping Circuit taking Source and Diode Resistances into Account:

In the discussion of the clamping circuit of Figure 2.44, we neglected the output resistance of the source as well as the diode forward resistance. Many times these resistances cannot be neglected. Figure 2.44 shows a more realistic clamping circuit taking into consideration the output resistance of the source R_S, which may be negligible or may range up to many hundreds of ohms depending on the source, and the diode forward resistance R_f which may range from tens to hundreds of ohms. Assume that the diode break point V_r occurs at zero voltage.

The precision of operation of the circuit depends on the condition that $R >> R_f$, and $R_r >> R$. When the input is positive, the diode is ON and the equivalent circuit shown in Figure 2.44(a) results. When the input is negative, the diode is *OFF* and the equivalent circuit shown in Figure 2.44(b) results.

range from tens to hundreds of ohms. Assume that the diode break point V_r occurs at zero voltage.

The precision of operation of the circuit depends on the condition that $R >> R_f$, and $R_r >> R$. When the input is positive, the diode is ON and the equivalent circuit shown in Figure 2.44(a) results.

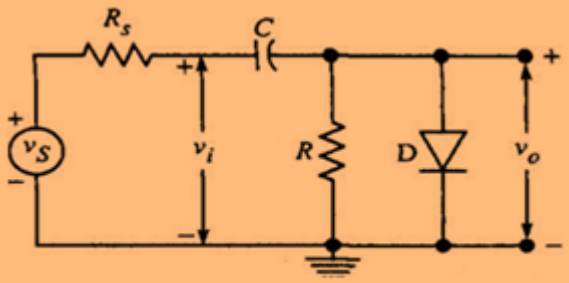


Figure 2.44 Clamping Circuit Considering the Source and Diode Forward Resistance

When the input is negative, the diode is *OFF* and the equivalent circuit shown in Figure 2.44(b) results.

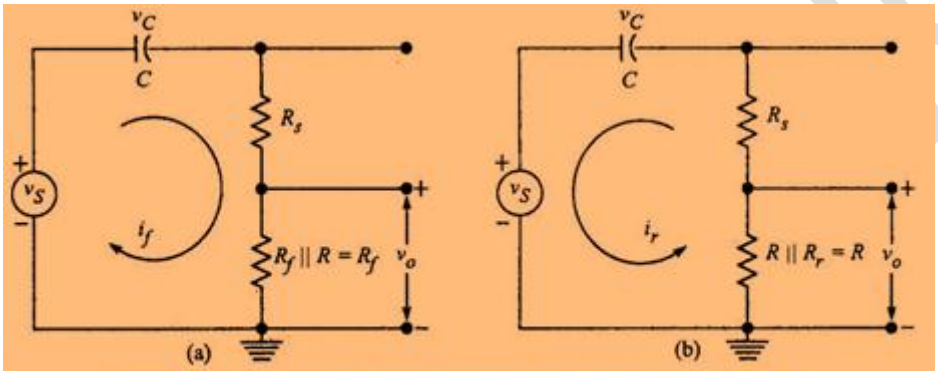


Figure 2.44 (a) Equivalent circuit when the diode is conducting and (b) the equivalent circuit when the diode is not conducting.

2.31.1 The Transient Waveform: When a signal is suddenly applied to the circuit shown in Figure 2.44 the capacitor charges (transient period) and gradually the steady-state condition is reached in which the positive peaks will be clamped to zero. The equivalent circuits shown in Figures 2.44(a) and 2.44(b) may be used to calculate the transient response.

2.31.2 Relation between Tilts in Forward and Reverse Directions:

The steady-state output waveform for a square wave input. Consider that the square wave input shown in Figure 2.45(a) is applied to the clamping circuit shown in Figure 2.44. The general form of the output waveform would be as shown in Figure 2.45(b), extending in both positive and negative directions and is determined by the voltages V_1, V_2, $V_1^{|}$, and $V_2^{|}$. These voltages may be calculated as discussed below.

- In the interval $0 < t < T$, the input is at its higher level; so the diode is ON and the capacitor charges with a time constant $(Rs + Rf)C$, and the output decays towards zero with the same time constant.
- Hence, $V_1^{|} = V_1 e^{-T_1 / \left(R_f + R_S \right) C}$ ----------2.15

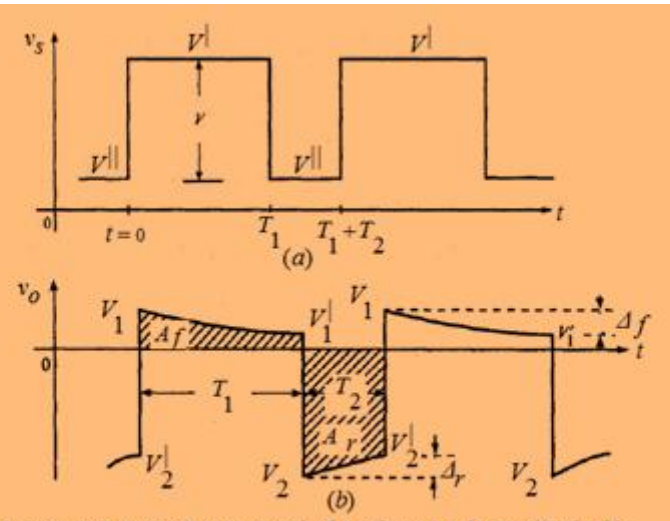


Figure 2.45 (a) A square wave input signal of peak-to-peak amplitude V (b) the general form of the steady-state output of a clamping circuit with the input as in (a)

- In the interval $0 < t < T$, the input is at its higher level; so the diode is ON and the capacitor charges with a time constant $(Rs + Rf)C$, and the output decays towards zero with the same time constant.
- Hence, $V_1^| = V_1 e^{-T_1/\left(R_f + R_S\right)C}$ ----------2.15
- In the interval $T_1 < t < T_1 + T_2$, the input is at its lower level; so the diode is OFF and the capacitor discharges with a time constant $(R + R_S)\,C$, and the output rises towards zero with the same time constant.
- Hence $V_2^| = V_2\, e^{-T_2/(R+R_S)C}$ ----------2.16
- ***Considering the conditions at t= 0.*** At $t = 0^-$, $v_S = V^{||}$, $v_0 = V_2^|$, the diode D is OFF and the equivalent circuit of Figure 2.44 (b) results. The voltage across the capacitor is given by
- $v_c = V^{||} - \frac{V_2^|}{R}(R+R_S)$ ----------2.17
- At $t = 0^+$, the input signal jumps to $V^|$, the output jumps to V_1, the diode conducts and the equivalent circuit of Figure 2.44(a) results. The voltage across the capacitor is given by
- $v_c = V^| - \frac{V_1}{R_f}(R_f + R_S)$ ---------- 2.18
- Since the voltage across the capacitor cannot change instantaneously, equating equations (2.17) and (2.18), we have

$$V^{|} - \frac{V_1}{R_f}(R_f + R_S) = V^{||} - \frac{V_2^{|}}{R}(R + R_S)$$

- $V^{|} - V^{||} = V = \frac{V_1(R_f + R_S)}{R_f} - \frac{V_2^{|}(R + R_S)}{R}$ ----------2.19

- ***Considering the conditions at t= T_1.*** At $t = T_1(-)$, $vs = V^{|}$, $vo = V_1^{|}$, the diode D is ON, and the equivalent circuit of Figure 2.44(a) results. The voltage across the capacitor is given by

- $v_c = V^{|} - \frac{V_1^{|}}{R_f}(R_f + R_S)$ ----------2.20

- At $t = T_1(+)$, $v_S = V^{||}$, $v_0 = V_2$, the diode D is OFF, and the equivalent circuit of Figure 2.44(b) results. The voltage across the capacitor is given by

- $v_c = V^{||} - \frac{V_2}{R}(R + R_S)$ ----------2.21

- Since the voltage across the capacitor cannot change instantaneously, equating equations (2.20) and (2.21), we get

$$V^{|} - \frac{V_1^{|}}{R_f}(R_f + R_S) = V^{||} - \frac{V_2}{R}(R + R_S)$$

- $V^{|} - V^{||} = V = \frac{V_1^{|}(R_f + R_S)}{R_f} - \frac{V_2(R + R_S)}{R}$ ----------2.22

- From equations (2.15), (2.16), (2.19) and (2.22), the values $V_1, V_1^{|}, V_2$ *and* $V_2^{|}$ can be computed and the output waveform determined.
- If the source impedance is taken into account, the output voltage jumps are smaller than the abrupt discontinuity *V* in the input.
- If *Rs* = 0, the jumps in input and output voltages are equal. Thus, when *Rs* = 0, observe that the response is independent of the absolute levels $V^{|}$ and $V^{||}$ of the input signal and is determined only by the amplitude *V*.
- It is possible, for example, for $V^{||}$ to be negative or even for both *V* and $V^{||}$ to be negative.
- The average level of the input plays no role in determining the steady-state output waveform.

- Under steady-state conditions, there is a tilt in the output waveform in both positive and negative directions. The relation between the tilts can be obtained by subtracting Eq. (2.19) from Eq. (2.22), i.e.
- $\frac{(R_f + R_S)}{R_f}(V_1 - V_1^{|}) - \frac{(R + R_S)}{R}(V_2^{|} - V_2) = 0$
- Let $V_1 - V_1^{|} = \Delta_f$ = tilt in the forward direction and
- $V_2^{|} - V_2 = \Delta_r$ = tilt in the reverse direction
- $\therefore \Delta_f = \frac{R_f}{R_f + R_S} \times \frac{R + R_S}{R} \Delta_r$ ----------2.23
- Since *Rs* is usually much smaller than *R*, then, the tilt in the forward direction Δ_f is almost always less than the tilt Δ_r in the reverse direction. Only when *Rs*<< *Rf*, are the two tilts almost equal.

2.32 Clamping Circuit Theorem:

- Under steady-state conditions, for any input waveform, the shape of the output waveform of a clamping circuit is fixed in such a way that the area in the forward direction (when the diode conducts) and the area in the reverse direction (when the diode does not conduct) are related by a relation $\frac{A_f}{A_r} = \frac{R_f}{R}$.
- ***The clamping circuit theorem states that, for any input waveform under steady-state conditions, the ratio of the area A_f under the output voltage curve in the forward direction(when the diode conducts) to that the area A_r in the reverse direction(when the diode does not conduct) is equal to the ratio*** R_f / R
- This theorem applies quite generally independent of the input waveform and the magnitude of the source resistance. The proof is as follows:
- Consider the clamping circuit of Figure 2.44, the equivalent circuits in Figures 2.44(a) and 2.44(b), and the input and output waveforms of Figures 2.45(a) and 2.45(b) respectively.

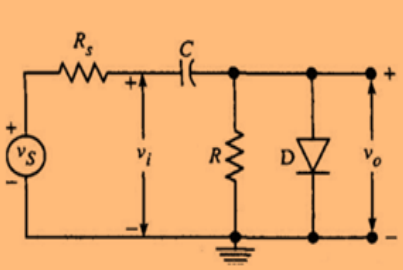


Figure 2.44 Clamping Circuit Considering the Source and Diode Forward Resistance

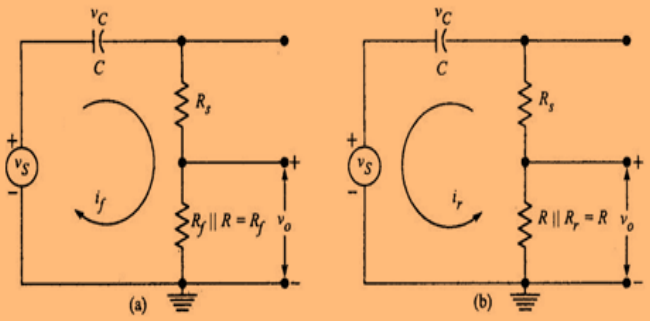


Figure 2.44 (a) Equivalent circuit when the diode is conducting and (b) the equivalent circuit when the diode is not conducting.

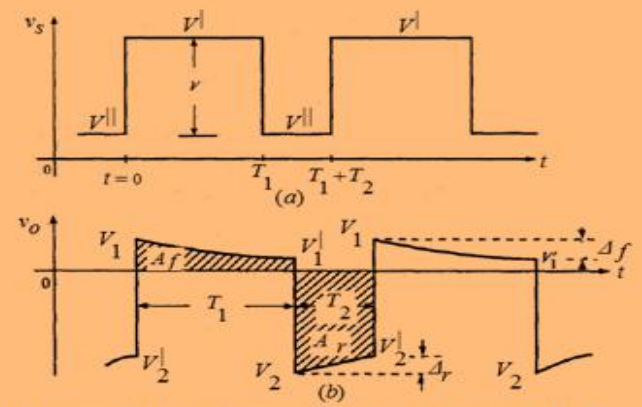


Figure 2.45 (a) A square wave input signal of peak-to-peak amplitude V (b) the general form of the steady-state output of a clamping circuit with the input as in (a)

- In the interval $0 < t < T$, the input is at its upper level, the diode is ON, and the equivalent circuit of Figure 2.44(a) results.
- If $v_f(t)$ is the output waveform in the forward direction, then the capacitor charging current is $i_f(t) = \dfrac{v_f(t)}{R_f}$.
- Therefore, the charge gained by the capacitor during the forward interval is

$$Q_f = \int_0^{T_1} i_f(t)dt = \frac{1}{R_f}\int_0^{T_1} v_f(t)dt = \frac{A_f}{R_f}.$$

- In the interval $T_1 < t < T_1 + T_2$, the input is at its lower level, the diode is OFF, and the equivalent circuit of Figure 2.44(b) results.
- If $v_r(t)$ is the output voltage in the reverse direction, then the current which discharges the capacitor is $i_r(t) = \dfrac{v_r(t)}{R}$.

- Therefore, the charge lost by the capacitor during the reverse interval is

$$Q_r = \int_{T_1}^{T_1+T_2} i_r(t)\,dt = \frac{1}{R}\int_{T_1}^{T_1+T_2} v_r(t)\,dt = \frac{A_r}{R} \quad .$$

- Under steady-state conditions, the net charge acquired by the capacitor over one cycle must be equal to zero.
- Therefore, the charge gained in the interval $0 < t < T_1$ will be equal to the charge lost in the interval $T_1 < t < T_1 + T_2$, i.e. $Q_f = Q_r$.

- $\frac{A_f}{R_f} = \frac{A_r}{R}$ *i.e.* $\frac{A_f}{A_r} = \frac{R_f}{R}$.----------2.24

2.33 The Practical Clamping Circuit:

In our discussion so far, we have assumed an ideal voltage source with $R_S = 0$. However, a practical voltage source has a finite R_S and the influence of R_S on the output will have to be taken into account. In this section, we examine the influence of the internal resistance of the voltage source on the output of the clamping circuit. If the internal resistance of the source R_S is introduced into the clamping circuit, the modified circuit is as depicted in Figure 2.46. When the input is applied to this modified circuit, the output reaches the steady-state value after a few cycles and the positive peaks are clamped to zero.

To understand how the output reaches the steady-state, let us examine the equivalent circuits for both the ON and the OFF states of the diode. When the diode is ON, the circuit is as represented in Figure 2.46(a). As $R_f << R$, this circuit reduces to that shown Figure 2.46(b). For the purpose of computing the output, the circuit in Figure 2.46(b) may be redrawn as shown in Figure 2.46(c).

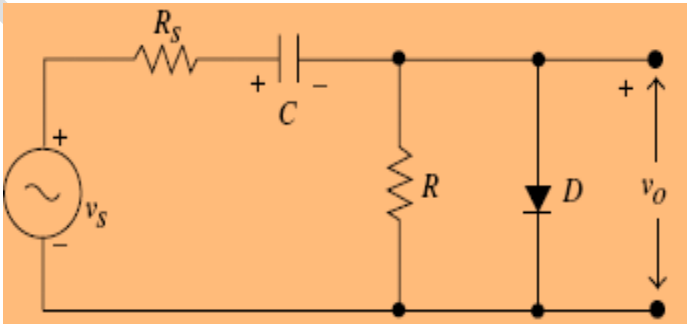


Figure 2.46 A clamping circuit where *RS* has been taken into account

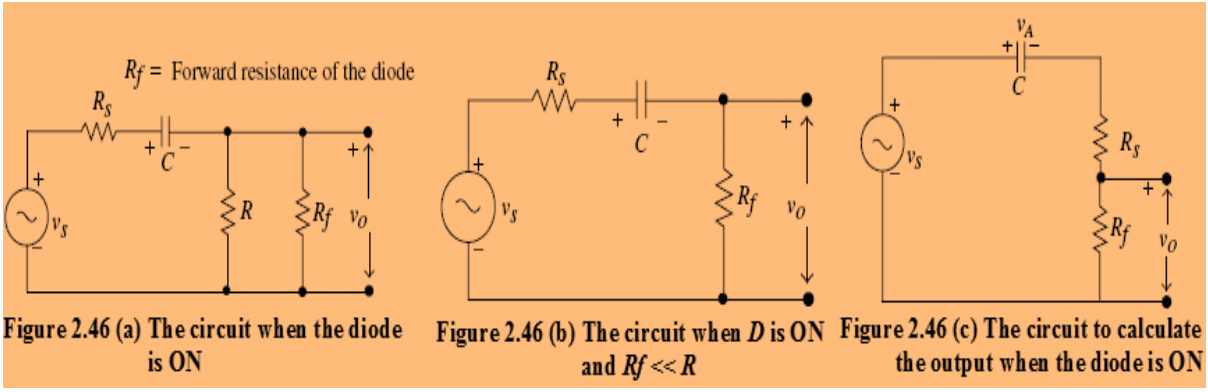


Figure 2.46 (a) The circuit when the diode is ON

Figure 2.46 (b) The circuit when *D* is ON and *Rf* << *R*

Figure 2.46 (c) The circuit to calculate the output when the diode is ON

Figure 2.47 (a) depicts the circuit when the diode is OFF. As the reverse resistance $R_r >> R$, the effective resistance is R and this circuit reduces as shown in Figure 2.47(b). Again, for computing the output, the circuit in Figure 2.47(b) is redrawn as in Figure 2.47(c).

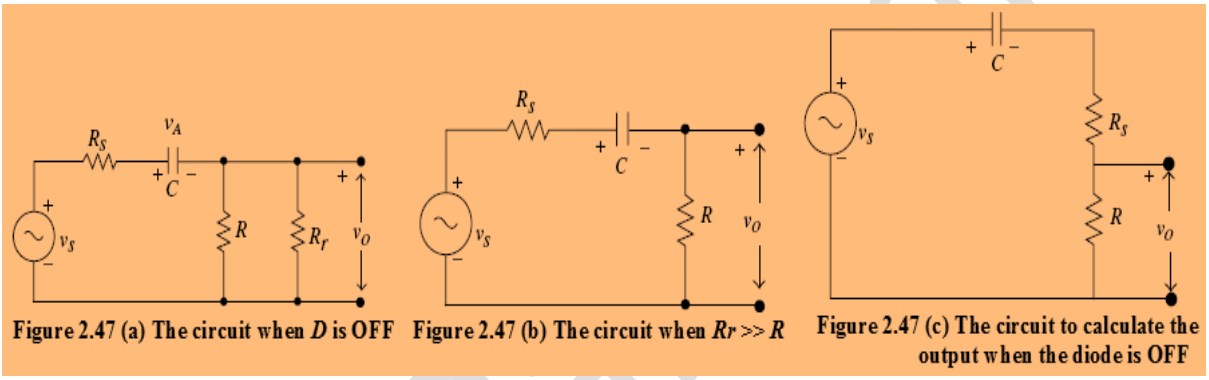


Figure 2.47 (a) The circuit when *D* is OFF

Figure 2.47 (b) The circuit when *Rr* >> *R*

Figure 2.47 (c) The circuit to calculate the output when the diode is OFF

2.33.1 Transient Response: Let us now consider the square wave v_S, shown in Figure 2.48 (a), applied as input to the clamping circuit in Figure 2.46. It is expected that the positive peak of the signal will be clamped to the zero level at the output almost instantaneously, but this does not happen. It takes a few cycles for the positive peak to be clamped to the zero level at the output. When the input is applied, the amplitude of the signal above the zero level goes on decreasing with each successive cycle. The output reaches the steady-state only after a few cycles from the instant the input is applied. The variation of the output with time during this period is called the transient response. At the end of this period when the positive peak is clamped to the zero level, the output is said to have reached the steady state.

We now examine how the output reaches the steady-state value after a few cycles (transient response). The variation of the output for the first few cycles, during the periods when the diode is ON and OFF, is then calculated. The input to the clamping circuit is a square wave with a peak-to-peak amplitude V and a finite frequency f ($1/T$) as shown in Figure 2.48(a).

- At t = 0+, the diode is ON. Using the equivalent circuit shown in Figure 2.46(c)
- $v_O(0+) = V \times \frac{R_f}{R_S + R_f}$. *If* $R_s = R_f$, $v_o(0+) = \frac{V}{2}$ ----------2.25

- During the period 0 to $T/2$, as the input remains constant, the output decays exponentially with the time constant $\tau = C\,(R_S + R_f)$ and is given by
- $v_O = V_f - (V_f - V_i)e^{-t/\tau}$, here $V_i = \frac{V}{2}$ *and* $V_f = 0$, $\tau = C(R_f + R_S)$
- $v_O = 0 - (0 - \frac{V}{2})e^{-t/\tau}$. At $t = T/2$, the voltage across R_f is
- $v_O\left(\frac{T}{2}\right) = v_O(0+)e^{-T/2\tau} = \frac{V}{2}e^{-T/2\tau}$ ----------2.26

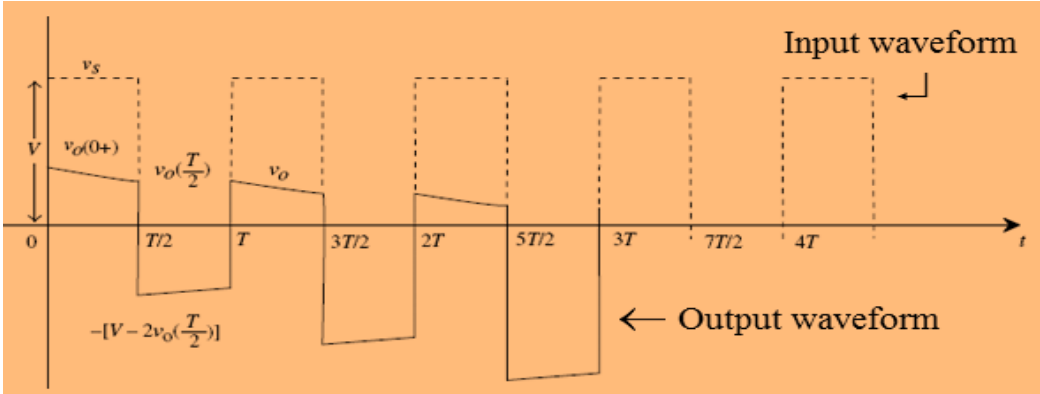


Figure 2.48 (a) The input and output waveforms of the clamping circuit

Hence, the total voltage across ($R_S + R_f$) = 2*vo* (*T*/2). As $R_s = R_f$.

The voltage across *C* is [*V* − 2*vo* (*T*/2)].

Now at *t* = *T*/2, the input falls to 0 V, and the diode is OFF.

The equivalent circuit shown in Figure 2.48(b) is the same as the equivalent circuit shown in Figure 2.48(c), except that the capacitor voltage is indicated here.

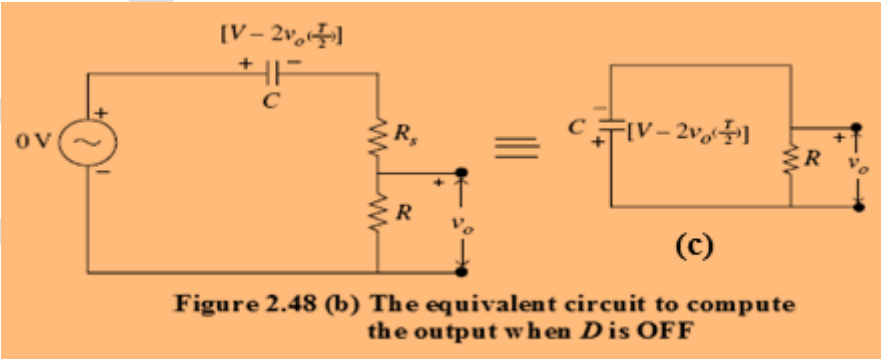


Figure 2.48 (b) The equivalent circuit to compute the output when *D* is OFF

- Since $R_S << R$, the output voltage *vo* is almost the same as [*V* − 2*vo* (*T*/2)] but with a negative sign.
- Hence the output at (*T*/2)+ abruptly falls to $-\left[V - 2v_o\left(\frac{T}{2}\right)\right]$.

- During the period T/2 to T, the input remains constant, the output decays exponentially with the time constant $\tau = C(R + Rs)$.
- $v_O(T) = -\left[V - 2v_o\left(\frac{T}{2}\right)\right]e^{-T/2\tau}$ ----------2.27
- The input once again changes by V. The process is repeated over a few cycles till a steady-state value is reached.

2.34 Biased Clamping:

If a voltage source of V_R volts is connected in series with the diode of a clamping circuit, the input waveform will be clamped with reference to V_R. Depending on the position of the diode, the input waveform may be positively clamped with reference to V_R, or negatively clamped with reference to V_R.

2.34.1 Clamping the Output to a Reference Voltage (V_R):

In the clamping circuit seen in Figure 2.46, the positive peak of the input signal is clamped to the zero level at the output. However, if the positive peak is to be clamped to a chosen reference voltage V_R for the circuit in Figure 2.46 a dc voltage V_R is to be included in the output.

The circuit in Figure 2.49 shows a clamping circuit similar to that seen in Figure 2.46 except for the fact that a reference voltage V_R is included and Rs is zero. To obtain the steady-state response of the circuit, we assume that V_R is zero. This circuit, then, is the clamping circuit that clamps the positive peak of the input signal to $V\gamma$ as shown in Figure 2.46.

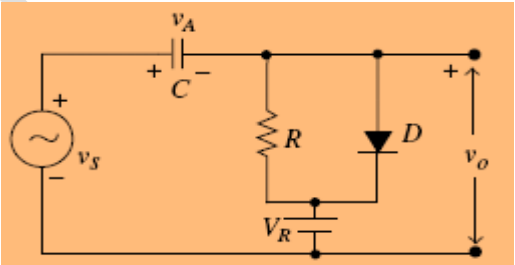


Figure 2.49 The circuit that clamps the positive peak of the input to VR

The steady-state responses for symmetric and un-symmetric square-wave inputs are plotted in Figure 2.50(a) and Figure 2.50(b), respectively.

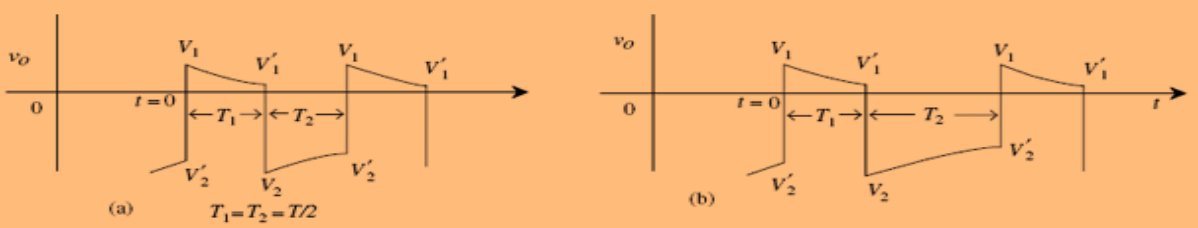


Figure 2.50 The steady-state response for (a) symmetric square-wave input and (b) unsymmetric square-wave input

Solving the four equations [Eqs. (5.6), (5.9), (5.10) and (5.11)], the values of V_1, V_2 and can be evaluated. To find these steady state output voltages with V_R included, add the value of V_R to each of these values. If, on the other hand, the polarity of V_R is reversed, add $-V_R$ to each of the values computed. The result is that the positive peak in the output is clamped to $-V_R$ as shown in Figure 2.51.

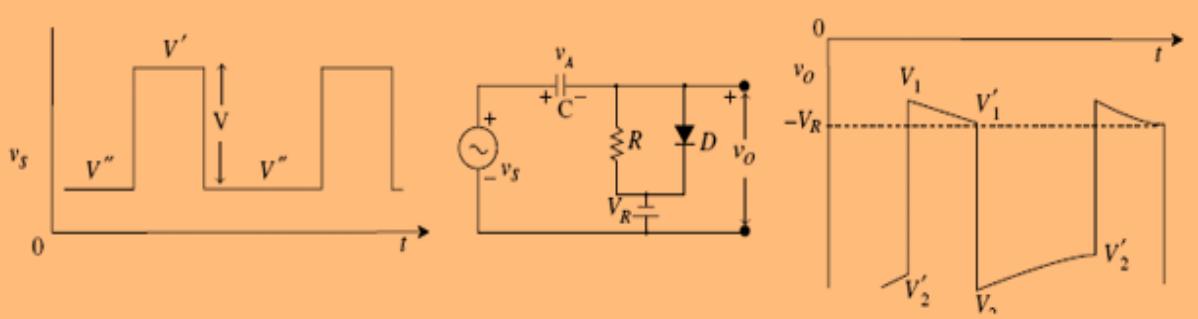


Figure 2.51 The positive peak of the input clamped to –VR

Similarly, look at the circuits in Figure 2.52 (a) and (b). The circuits here clamp the negative peak of the input to + V_R and − V_R respectively.

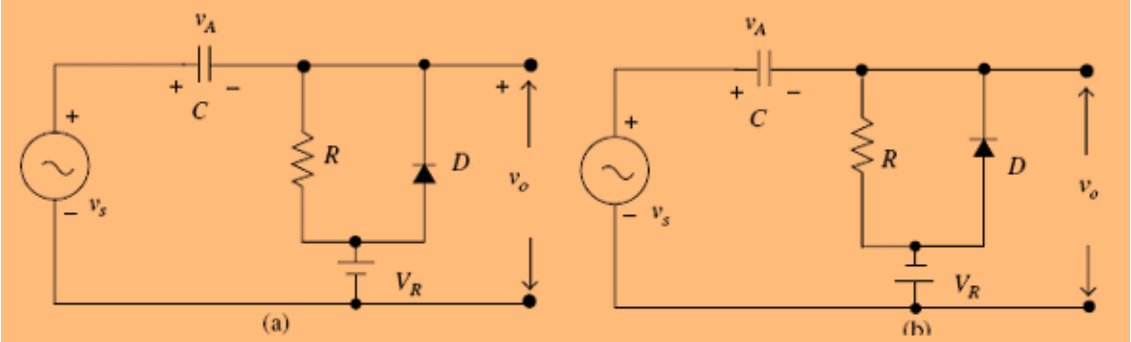


Figure 2.52 (a) The negative peak of the input clamped to +VR; and (b) the negative peak of the input clamped to –VR

To simplify the analysis of the clamping circuits let us assume:

1. The forward resistance of the diode *D* when ON is negligible. We assume that there is no distortion in the output when *D* is ON.

2. The time constant τ (= *RC*) is so large when compared to the time period of the signal under consideration that practically there is no change in the voltage on the condenser *C*, when *D* is OFF.

3. The internal resistance of the source *vs*, *RS* = 0.

Based on these assumptions, a simple and straight forward method to analyze clamping circuits is as follows:

Step 1: Start the analysis from the time duration during which *D* is ON. If the starting time duration keeps *D* OFF, skip that time interval.

Step 2: Consider the relevant circuit, taking care of the polarities of the voltages. Calculate v_O.

Step 3: Find v_C, the voltage on *C*.

Step 4: Consider the next time interval. Draw the circuit, taking care of the polarities of the input and *vA*. Calculate *vo*. If the input is periodic you can plot the steady-state output. To understand the procedure let us consider an example.

2.35 The Effect of Diode Characteristics on the Clamping Voltage:

For the clamping circuit shown in Figure 2.46, to obtain the steady-state response, the diode is replaced by *Rf* when ON and *Rr* = ∞ when OFF. Though the positive peak of the signal in the output is ideally required to be clamped to the zero level, in practice it is clamped to a voltage *Vcl* = *Vγ*, where *Vγ* is the cut-in voltage of the diode. In a practical diode, the current variation is non-linear in nature. Hence, we consider the influence of the diode characteristics on the clamping voltage, *Vcl* and show that the clamping voltage (*Vcl*) changes with a change in the amplitude of the input signal. Let us consider the clamping circuit described in Figure 2.46 and let its input be a symmetric square wave as shown in

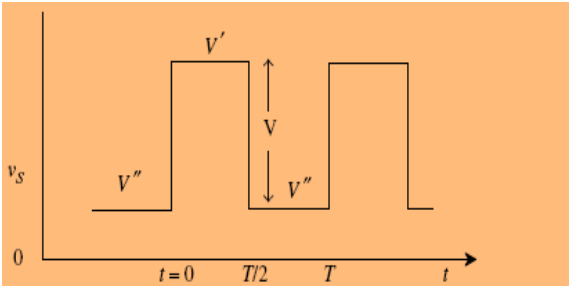


Figure 2.53 (a) A symmetric square-wave input with peak-to-peak amplitude *V*

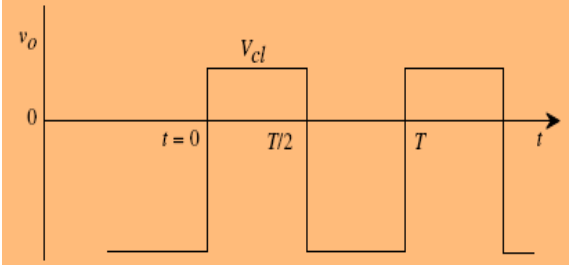


Figure 2.53 (b) The steady-state output with a large C

Figure 2.53 (a).

If *C* is large, irrespective of whether the diode is ON or OFF, the time constants are large so that the output is also a square wave. The steady-state output has a general form as shown in Figure 2.53(b).

In obtaining the steady-state response, we assumed that the diode is ideal with a small *Rf*. In practice, however, an idealized diode, when ON, is represented as a switch in series with a battery voltage of *Vγ*, a resistance *Rf* [see Figure 2.53 (c)]; and biased by *V′* as shown in Figure 2.53(a).

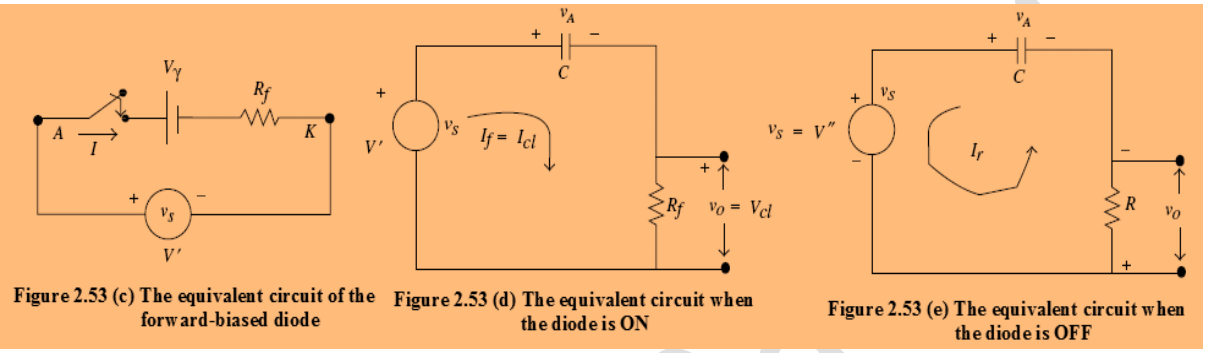


Figure 2.53 (c) The equivalent circuit of the forward-biased diode

Figure 2.53 (d) The equivalent circuit when the diode is ON

Figure 2.53 (e) The equivalent circuit when the diode is OFF

We now consider the V–I characteristic of the practical diode to understand the influence of the diode characteristics on the clamping voltage. The diode current is given by the relation:

$$I = I_o e^{V/\eta V_T} \quad \text{----------2.28}$$

When the diode is ON, the positive peak of the signal is clamped to *Vcl* and the current in the diode is *Icl*. *Vcl* is the voltage to which the positive peak is clamped.

$$I_{cl} = I_o e^{V_{cl}/\eta V_T} \quad \text{----------2.29}$$

The equivalent circuit when the diode is ON, when *vs* = *V′* with *RS* = 0 is shown in Figure 2.53(d). From Figure 2.53 (d)

$$v_A = V^{|} - V_{cl} \quad \text{----------2.30}$$

During the negative half-cycle of the square-wave input, *vs* = *V″* and the diode is OFF. The equivalent circuit is given in Figure 2.53 (e). From Figure 2.53 (e)

$$v_A = V^{||} + v_o \quad \text{----------2.31}$$

And $v_o \approx V - V_{cl}$ ----------2.32

Using Eqs. (2.31) and (2.32), we get

$$v_A - V^{\|} = V - V_{cl} \text{ ----------2.33}$$

In practice, $Vcl \approx V\gamma$ and V can be typically of the order of a few tens of volts. Thus $V >> Vcl$. From Eq. (2.21)

$$v_A - V^{\|} = V \text{ ----------2.34}$$

As the net voltage across R is V, Ir the discharging current of C is given by the relation

$$I_r = \frac{V}{R} \text{ ----------2.35}$$

As the input is a symmetric square wave, under steady-state, the charge gained by C when the diode is ON should be equal to the charge lost by C when the diode is OFF. Therefore,

$$I_r = I_{cl} \text{ ----------2.36}$$

From Equations (2.29) and (2.25)

$$\frac{V}{R} = I_o e^{V_{cl}/\eta V_T}$$

$$e^{V_{cl}/\eta V_T} = \frac{V}{RI_o}$$

Taking logarithms to the natural base:

$$V_{cl}/\eta V_T = \ln \frac{V}{RI_o}$$

$$V_{cl} = \eta V_T \ln \frac{V}{RI_o} \text{ ----------2.37}$$

$$\frac{dV_{cl}}{dV} = \eta V_T \frac{RI_o}{V} \times \frac{1}{RI_o} = \frac{\eta V_T}{V}$$

$$dV_{cl} = \eta V_T \times \frac{dV}{V} \text{ ----------2.38}$$

Equation (2.37) gives the steady-state clamping voltage and Eq. (2.38) describes the variation in the clamping voltage with a change in the amplitude of the input signal. For a silicon diode used in a clamping circuit for which $Vcl = V\gamma = 0.5$ V, $\eta = 2$, $V = 10$ V and $dV = 1$ V:

$$dV_{cl} = 2 \times 26mV \times \frac{1}{10} = 5.2\,mV$$

Equation (2.26) suggests that as *V* increases, the change in the clamping voltage, *dVcl*, becomes smaller. Also, when the diode is ON, *V* is the forward-bias. Hence, to ensure that the clamping voltage remains unaltered, the diode must be forward-biased by a larger voltage. The circuit for this is represented in Figure 2.54 (a).

Let us now try to calculate *dVcl* for this circuit to verify whether this arrangement really ensures negligible change in *Vcl* or not. Redrawing the circuit in Figure 2.54(a) gives Figure 2.54(b). The equivalent circuit when the diode is ON, i.e., when *vs* = *V′*, is shown in Figure 2.54(c).

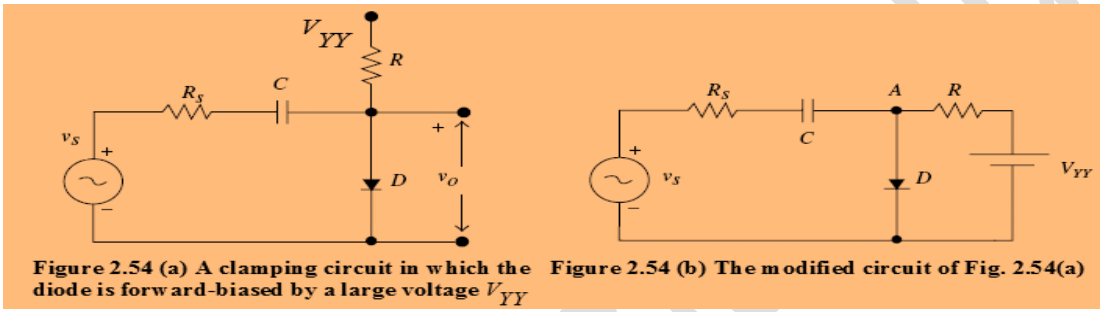


Figure 2.54 (a) A clamping circuit in which the diode is forward-biased by a large voltage V_{YY} **Figure 2.54 (b) The modified circuit of Fig. 2.54(a)**

From Eq. (2.29) $I_{cl} = I_o e^{V_{cl}/\eta V_T}$

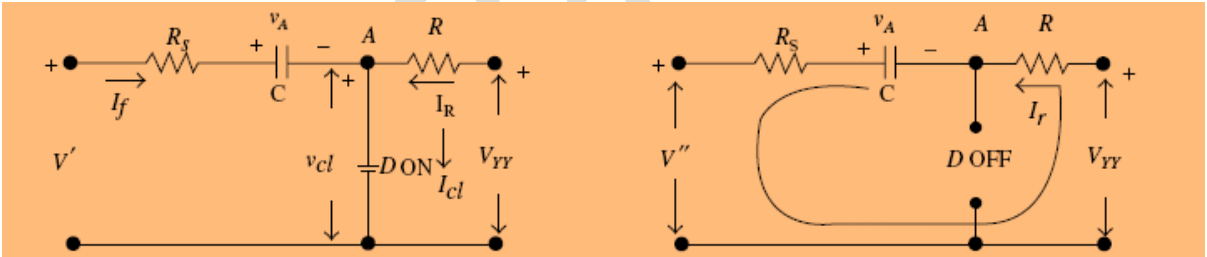


Figure 2.54(c) The equivalent circuit of Fig. 2.54(b) when the diode is forward-biased **Figure 2.54(d) The equivalent circuit of Fig. 2.54(b) when the diode is OFF**

From Figure 2.54(c)

$$I_r = \frac{V_{YY} - V_{cl}}{R} \approx \frac{V_{YY}}{R} \text{ ----------2.39}$$

as *Vcl* << *VYY*.

From Figure 2.54(c), writing the KCL equation at node *A* we get

$$I_f + I_R - I_{cl} = 0$$

$$I_f = I_{cl} - I_R = I_{cl} - \frac{V_{YY}}{R} \text{ ----------2.40}$$

Also, $v_A = V^{|} - V_{cl} - I_f R_s = V^{|} - V_{cl} - \left(I_{cl} - \frac{V_{YY}}{R} \right) R_s$ ----------2.41

When the input goes to *V*″, the diode is OFF and the equivalent circuit is as shown in Figure 2.54(d).

The discharging current *Ir* is:

$$I_r = \frac{V_{YY} - V^{||} + v_A}{R + R_s} = \frac{V_{YY} - V^{||} + v_A}{R}$$ ----------2.42

Since *R* >> *RS*, Put Equation (2.29) in (2.30)

$$I_r = \frac{1}{R}\left[V_{YY} - V^{||} + V^{|} - V_{cl} - \left(I_{cl} - \frac{V_{YY}}{R} \right) R_s \right] = \frac{1}{R}\left[V_{YY}\left(1 + \frac{R_s}{R} \right) - V^{||} + V^{|} - V_{cl} - I_{cl} R_s \right]$$

But *V*′ − *V*″ = *V*. Therefore

$$I_r = \frac{1}{R}\left[V_{YY}\left(1 + \frac{R_s}{R} \right) + V - V_{cl} - I_{cl} R_s \right]$$

We know that *V* >> *Vcl* and *RS* << *R*. Therefore,

$$I_r = \frac{1}{R}\left[V_{YY} + V - I_{cl} R_s \right]$$ ----------2.43

As the input is a symmetric square wave, *If* = *Ir*. Then from, from Equations (2.28) and (2.31)

$$I_{cl} - \frac{V_{YY}}{R} = \frac{1}{R}\left[V_{YY} + V - I_{cl} R_s \right]$$

$$I_{cl}\left(1 + \frac{R_s}{R} \right) = \frac{1}{R}\left[V_{YY} + V_{YY} + V \right] = \frac{1}{R}\left[2V_{YY} + V \right]$$

As *RS* << *R*,

$$I_{cl} = \frac{2V_{YY} + V}{R}$$ ----------2.44

From Eq. (2.29) $I_{cl} = I_o e^{V_{cl} / \eta V_T}$

Substituting this value in equation 2.32, we get

$$\frac{2V_{YY}+V}{R}=I_o e^{V_{cl}/\eta V_T}$$

Taking logarithms to the natural base:

$$V_{cl}=\eta V_T \ln\left(\frac{2V_{YY}+V}{I_o R}\right) \text{----------2.45}$$

Differentiating on both sides we get,

$$\frac{d}{dV}V_{cl}=\eta V_T \frac{I_o R}{2V_{YY}+V}\times\frac{1}{I_o R}$$

$$dV_{cl}=\eta V_T \frac{dV}{2V_{YY}+V} \text{----------2.46}$$

2.36 Synchronized Clamping:

In the clamping circuits examined in this chapter, the duration for which clamping is effective is controlled by the signal alone—the signal remains clamped as long as its amplitude remains unaltered. However, in some applications it may become necessary that the time of clamping be determined by the control or gating signal that occurs synchronously with the signal. Two or more signals are said to be synchronized if they arrive at a particular reference point in their cycles at the same time. The simultaneous presence of the gating signal during the period of constant amplitude input enables the two waveforms to be synchronized and the output to be referenced to V_R . One typical application could be in a CRO, where, for the spot to move vertically, the signal applied to the X-deflecting plates of the CRT varies in both directions but returns to a reference level V_R , as shown in Figure 2.55(a).

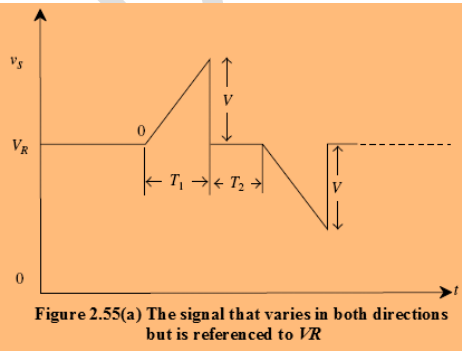


Figure 2.55(a) The signal that varies in both directions but is referenced to *VR*

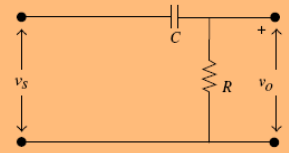


Figure 2.55 (b) A high-pass *RC* circuit

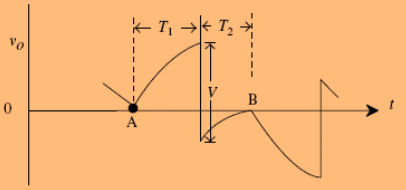


Figure 2.55 (c) The output of a capacitive coupling network (high-pass circuit)

Let the signal then be transmitted through a capacitive coupled network like a high-pass network shown in Figure 2.55(b).

For the duration 0 to T_1, when the input is a ramp, the output varies exponentially from point A with a time constant τ. At $t = T_1$, both the input and the output fall by V, giving rise to an undershoot. During the interval $T1$ to T_2, as the input remains constant, the output decays exponentially to zero (point B). A similar variation takes place during the period the signal is negative. The resultant output waveform *vo* is shown in Figure 2.55(c).

This output is devoid of a dc component. To reintroduce the dc component, we apply a signal referenced to the zero level [see Figure 2.56(a)] as input to the circuit, as shown in Figure 2.56(b). The output waveform of this circuit is shown in Figure 2.56(c).

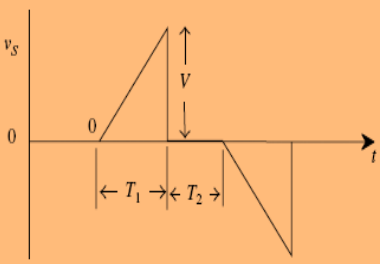


Figure 2.56 (a) The input signal

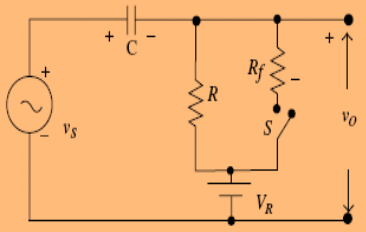


Figure 2.56 (b) The switch S operates in sync with the signal to clamp the output to *VR*

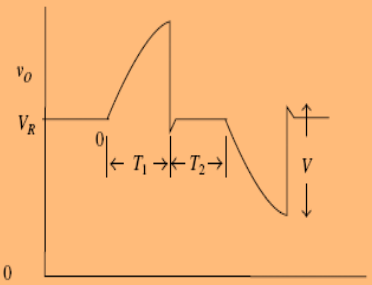


Figure 2.56 (c)The output of the circuit in Fig. 2.56(b)

When the switch *S* closes, during the interval T_2, $vo = V_R$. When the switch *S* opens during the interval T_1, *C* charges resulting in the waveform shown in Fig. 2.56(c). The small spikes can be reduced to negligible values if the switch has a zero resistance in the ON position.

The circuit in Fig. 2.56(b) can be implemented practically using diodes *D*1 and *D*2, and two control signals *v*1 and *v*2, with a 180° phase shift, as shown in Figures 2.57(a), 2.58(a) and 2.58(b). If the signal in Figure 2.58(c) is referenced to the zero level; the output in Figure 2.58(d) is referenced to V_R.

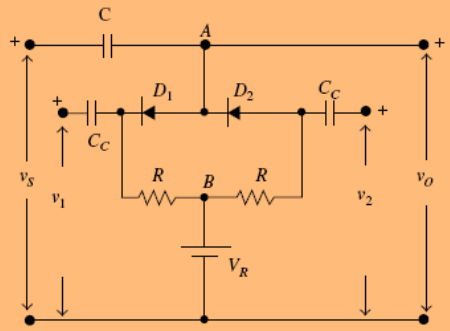


Figure 2.57 (a) A synchronized clamping circuit

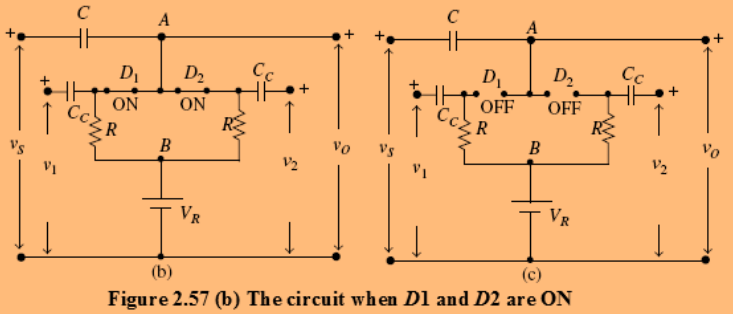


Figure 2.57 (b) The circuit when *D*1 and *D*2 are ON and (c) the circuit when *D*1 and *D*2 are OFF

T_C is the time duration of the control signals and *Tn* is the time period during which the control signals are zero. The input to the clamping circuit is synchronized with the control signals *v*1and *v*2. Since the input *vs* is referenced to the zero level, the purpose of this circuit is to introduce a dc voltage (V_R) so that the output *vo* is now referenced to V_R instead of the zero level. From the circuit in Figure 2.57(a), it is evident, for the given polarities of the control signals that the diodes *D*1 and *D*2 conduct during the period T_C, resulting in the circuit of Figure 2.57(b). As *v*1 and *v*2 are of equal magnitudes but of the opposite polarity, their net effect is zero at the output. The result is the output V_R. However, when the control signals are zero, diodes *D*1 and *D*2 are OFF,

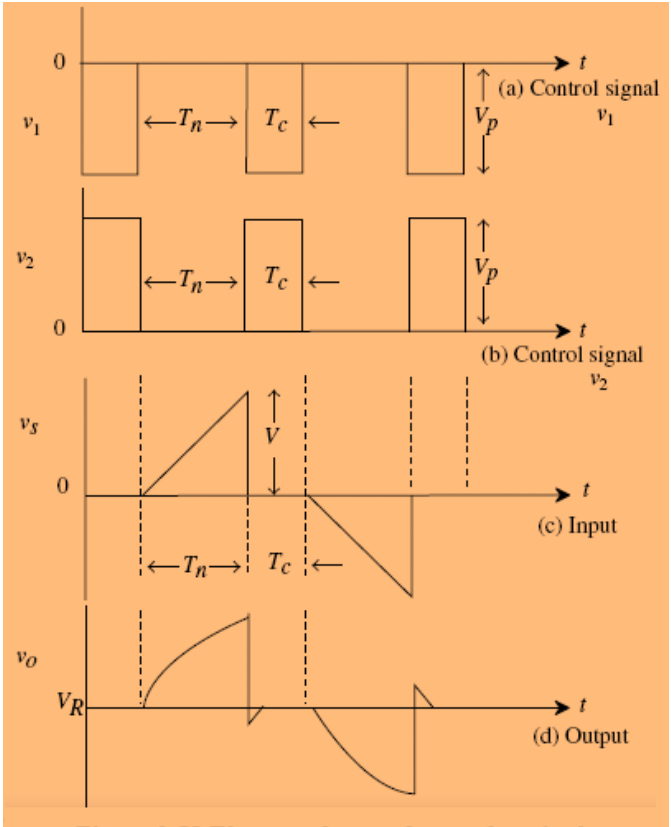


Figure 2.58 The waveforms of a synchronized clamping circuit

resulting in the circuit of Figure 2.57(c). The input is transmitted to the output terminals with a slight distortion in amplitude, as the capacitor charges exponentially. The output of this circuit is now referenced to V_R, meaning that a dc voltage V_R is introduced by the clamping circuit.

2.37 The Clamping Circuit Theorem:

This theorem enables us to calculate the voltage level to which the output is clamped by considering the areas above and below the reference level, when the values of *Rf* and *R* are known.

The clamping circuit theorem states that under steady-state conditions, for any input waveform, the ratio of the area under the output voltage curve in the forward direction to that in the reverse direction is equal to the ratio Rf/R. To prove the clamping circuit theorem, consider a typical steady-state output for the clamping circuit, represented in Figure 2.59. In the time interval *t*1 to *t*2, *D* is ON. Hence, during this period, the charge builds up on the capacitor *C*. If *if* is the diode current, the charge gained by the capacitor during the interval *t*1to *t*2 is:

$$q_1 = \int_{t_1}^{t_2} i_f \, dt \text{ ----------2.47}$$

However, *if* = *Vf* / *Rf*, where *Vf* is the diode forward voltage

$$q_1 = \frac{1}{R_f}\int_{t_1}^{t_2} V_f\,dt$$ ----------2.48

During the interval $t2$ to $t3$, D is OFF. Hence, the capacitor discharges and the charge lost by C is

$$q_2 = \int_{t_2}^{t_3} i_r\,dt$$ ----------2.49

Put $ir = Vr/R$, where Vr is the diode reverse voltage:

$$q_2 = \frac{1}{R}\int_{t_2}^{t_3} V_r\,dt$$ ----------2.38

At steady state, the charge gained is equal to the charge lost. In other words, $q1 = q2$.

Therefore,

$$\frac{1}{R_f}\int_{t_1}^{t_2} V_f\,dt = \frac{1}{R}\int_{t_2}^{t_3} V_r\,dt$$ ----------2.39

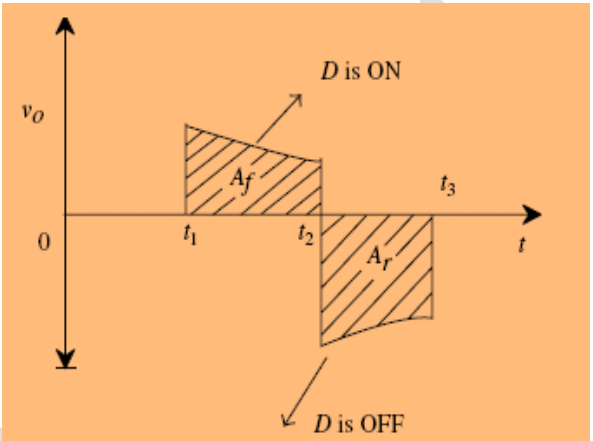


Figure 2.59 Typical steady-state output of the clamping circuit

However,

$$A_f = \int_{t_1}^{t_2} V_f\,dt \quad and \quad A_r = \int_{t_2}^{t_3} V_r\,dt$$ ----------2.50

Here, Af is the area with D in the ON state and Ar is the area under the output curve with D in the OFF state.

From Equations (2.39) and (2.40):

$$\frac{A_f}{R_f} = \frac{A_r}{R} \quad \text{or} \quad \frac{A_f}{A_r} = \frac{R_f}{R}$$ ----------2.51

This relation is known as the clamping circuit theorem.

Consider Figure 2.60 in which the output of the clamping circuit is assumed to remain almost constant during the periods $T1$ and $T2$ when the diode D is ON and OFF by choosing large values of C. If $V1$ and $T1$ are the voltage and time duration above the reference level and $V2$ and $T2$ are the voltage and time duration below the reference level under steady-state, then as per this theorem:

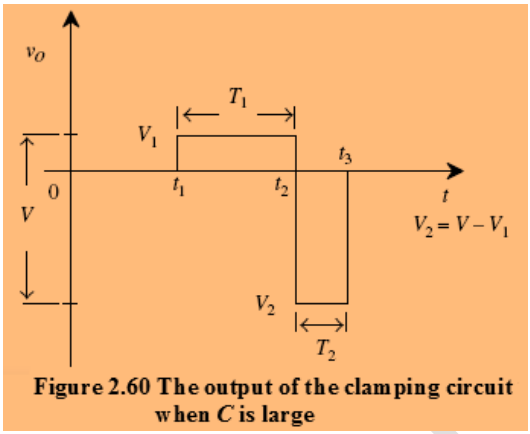


Figure 2.60 The output of the clamping circuit when C is large

$$\frac{A_f}{A_r} = \frac{V_1 T_1}{V_2 T_2} = \frac{V_1 T_1}{(V - V_1) T_2} = \frac{R_f}{R} \quad \text{----------2.52}$$

Assuming that T_1, T_2, Rf, R and the amplitude of the signal V are known, it is possible to compute the voltage level V_1 to which the signal is clamped at the output.

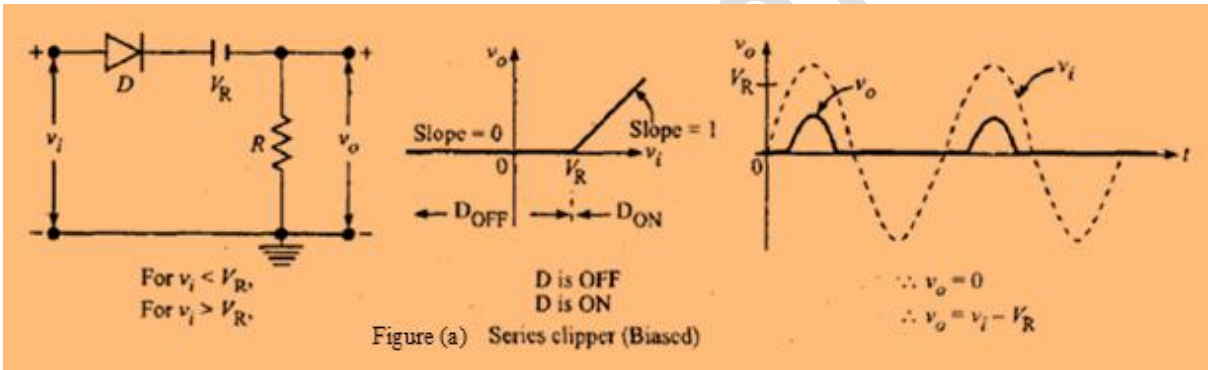


Figure (a) Series clipper (Biased)

Considering the above series clipper circuits shown in Figure (a),

$v_i < V_R$ *Diode is OFF* $v_o = 0$ *slope* $= 0$

$v_i \geq V_R$ *Diode is ON* $v_o = v_i - V_R$ *slope* $= 1$

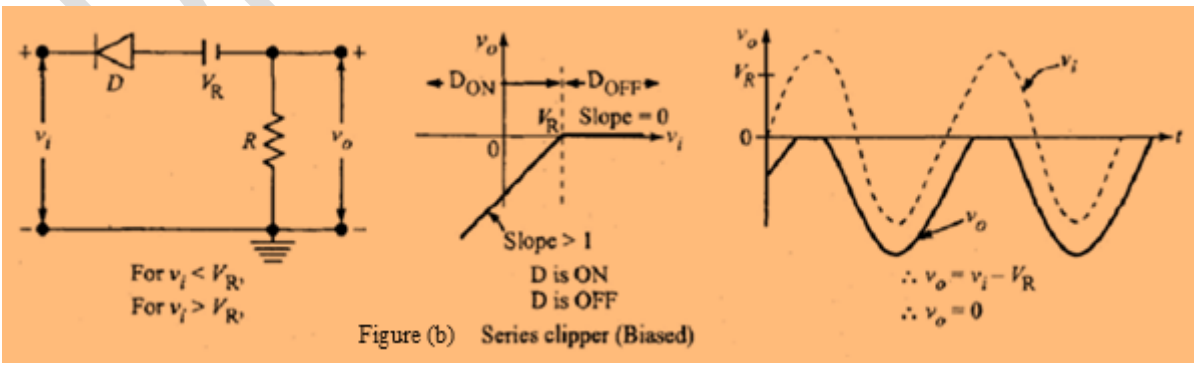


Figure (b) Series clipper (Biased)

Considering the above series clipper circuits shown in Figure (b)

$v_i \le V_R$ *Diode is ON* $v_o = v_i - V_R$ *slope* $= 1$

$v_i > V_R$ *Diode is OFF* $v_o = 0$ *slope* $= 0$

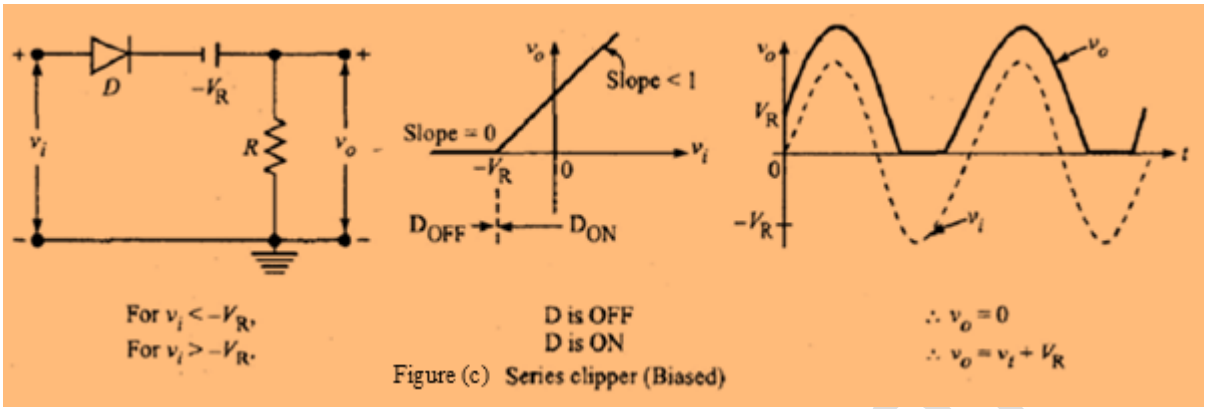


Figure (c) Series clipper (Biased)

Considering the above series clipper circuits shown in Figure (c)

$v_i < -V_R$ *Diode is OFF* $v_o = 0$ *slope* $= 0$

$v_i \ge -V_R$ *Diode is ON* $v_o = v_i + V_R$ *slope* $= 1$

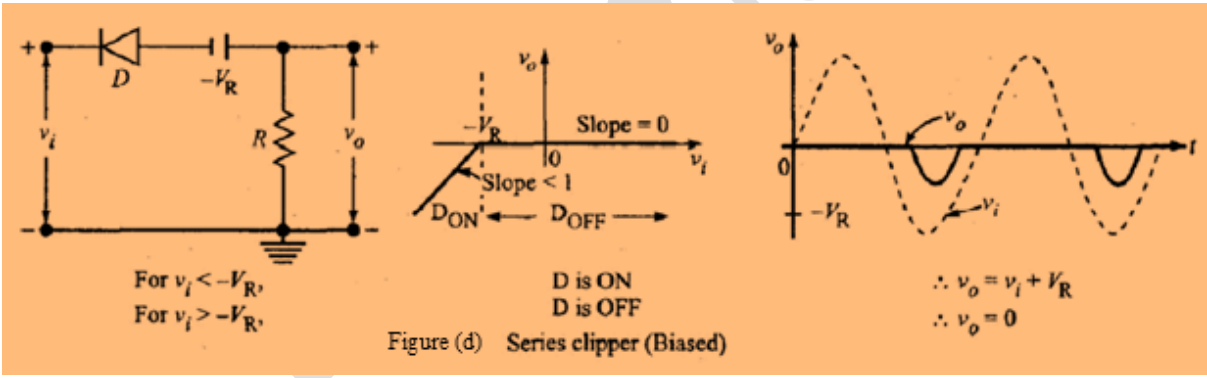


Figure (d) Series clipper (Biased)

Considering the above series clipper circuits shown in Figure (d)

$v_i \le -V_R$ *Diode is ON* $v_o = v_i + V_R$ *slope* $= 1$

$v_i > -V_R$ *Diode is OFF* $v_o = 0$ *slope* $= 0$

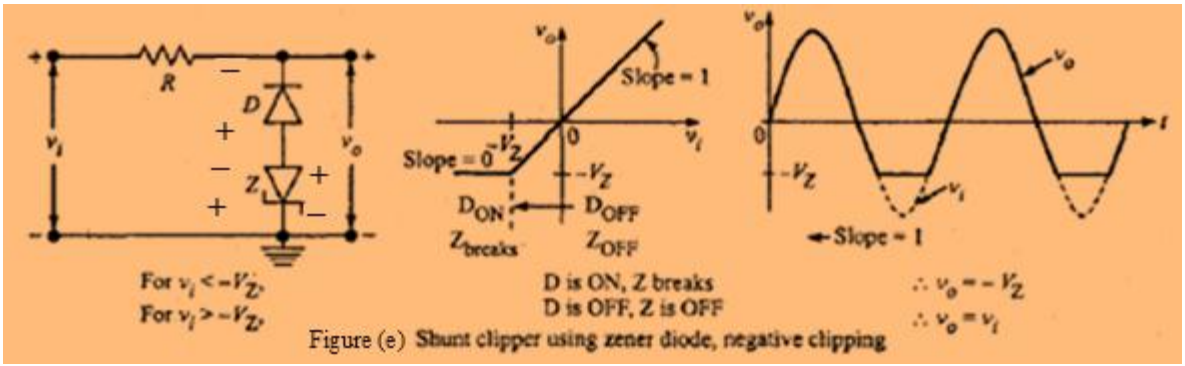


Figure (e) Shunt clipper using zener diode, negative clipping

Considering the above series clipper circuits shown in Figure (e)

$v_i \le -V_Z$ *Diode is ON Z is breaks* $v_o = -V_Z$ *slope* $= 0$

$v_i > -V_Z$ *Diode is OFF Z is OFF* $v_o = v_i$ *slope* $= 1$

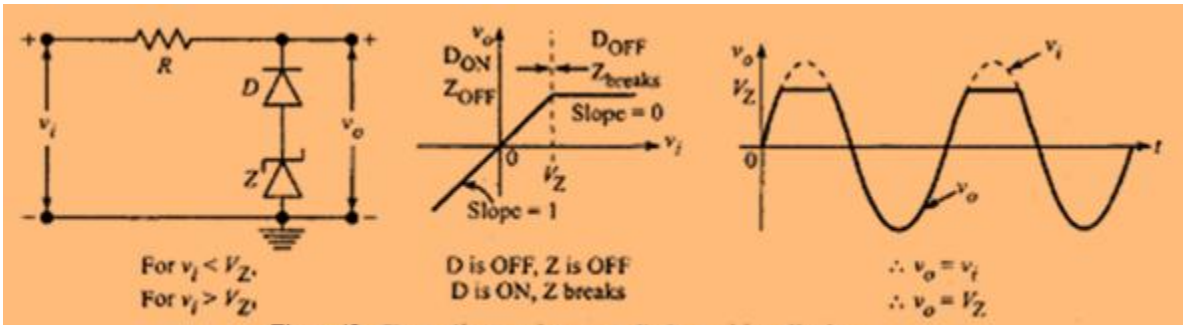
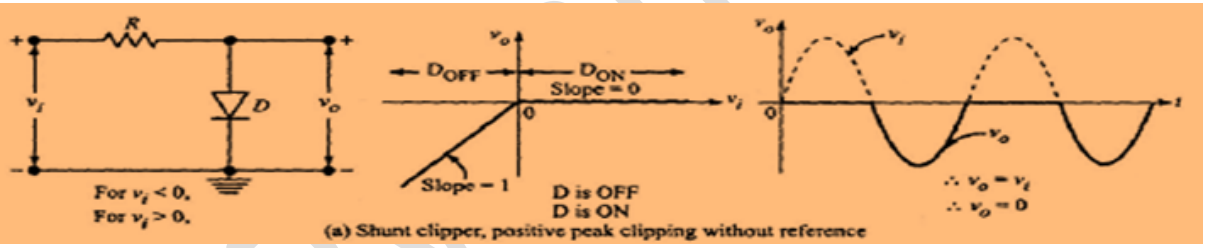


Figure (f) Shunt clipper using zener diode, positive clipping

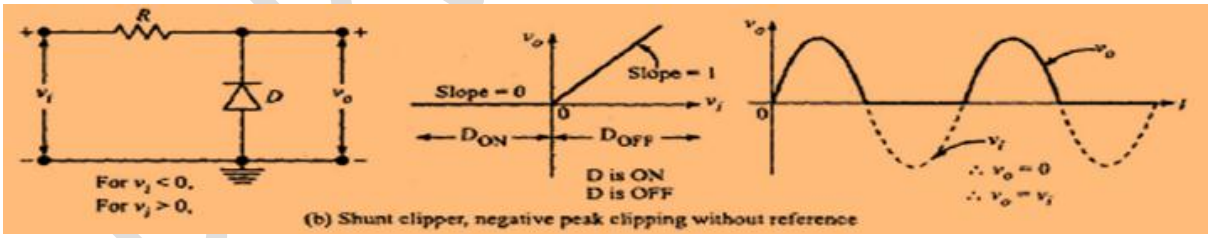
Considering the above series clipper circuits shown in Figure (f)

$v_i < V_Z$ *Diode is OFF Z is OFF* $v_o = v_i$ *slope* $= 1$

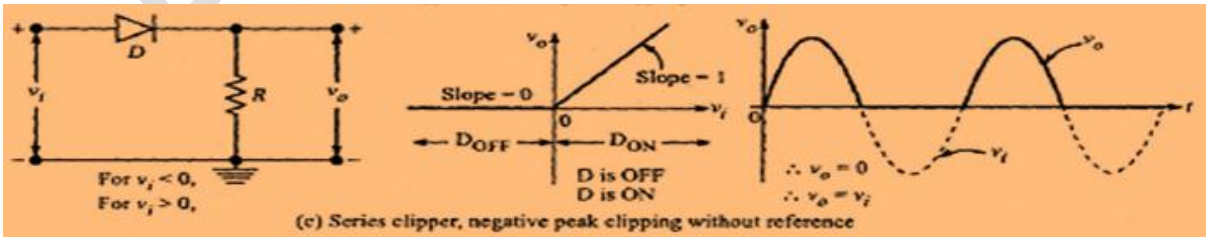
$v_i \ge V_Z$ *Diode is ON Z is breaks* $v_o = V_Z$ *slope* $= 0$



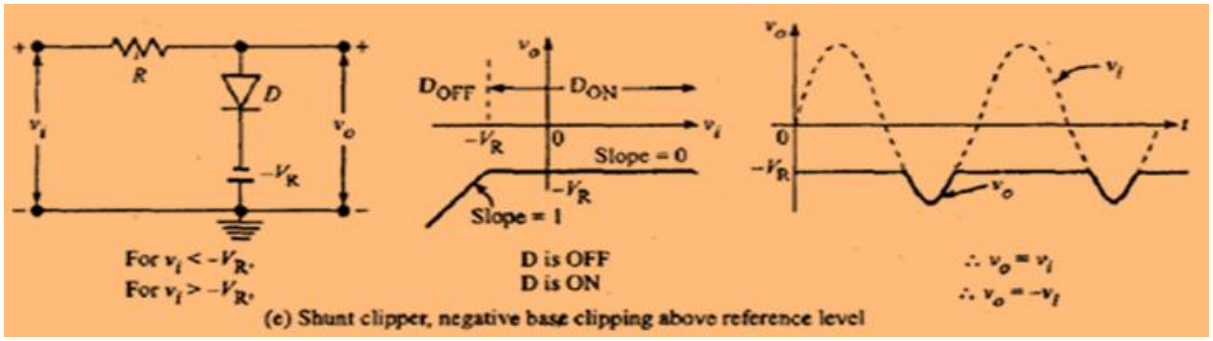
(a) Shunt clipper, positive peak clipping without reference



(b) Shunt clipper, negative peak clipping without reference

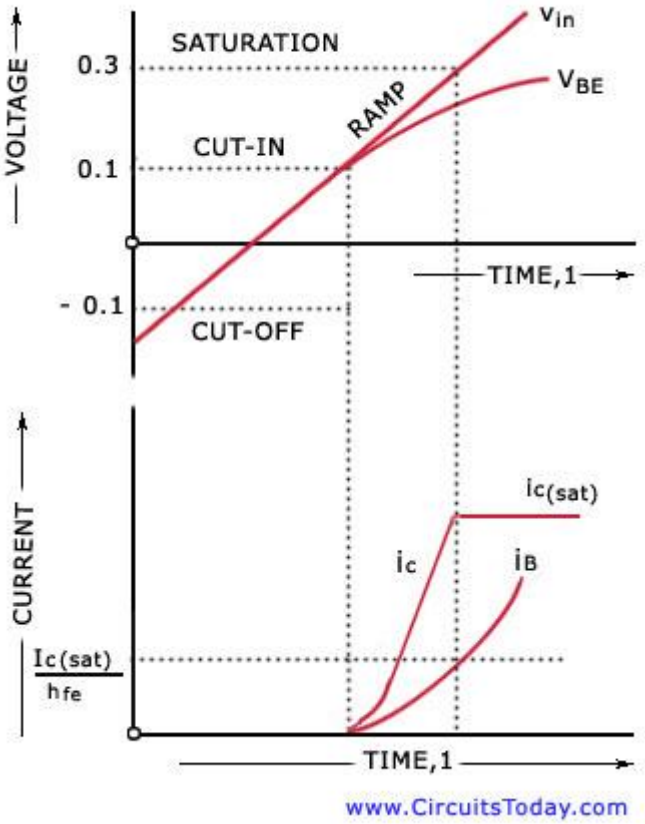


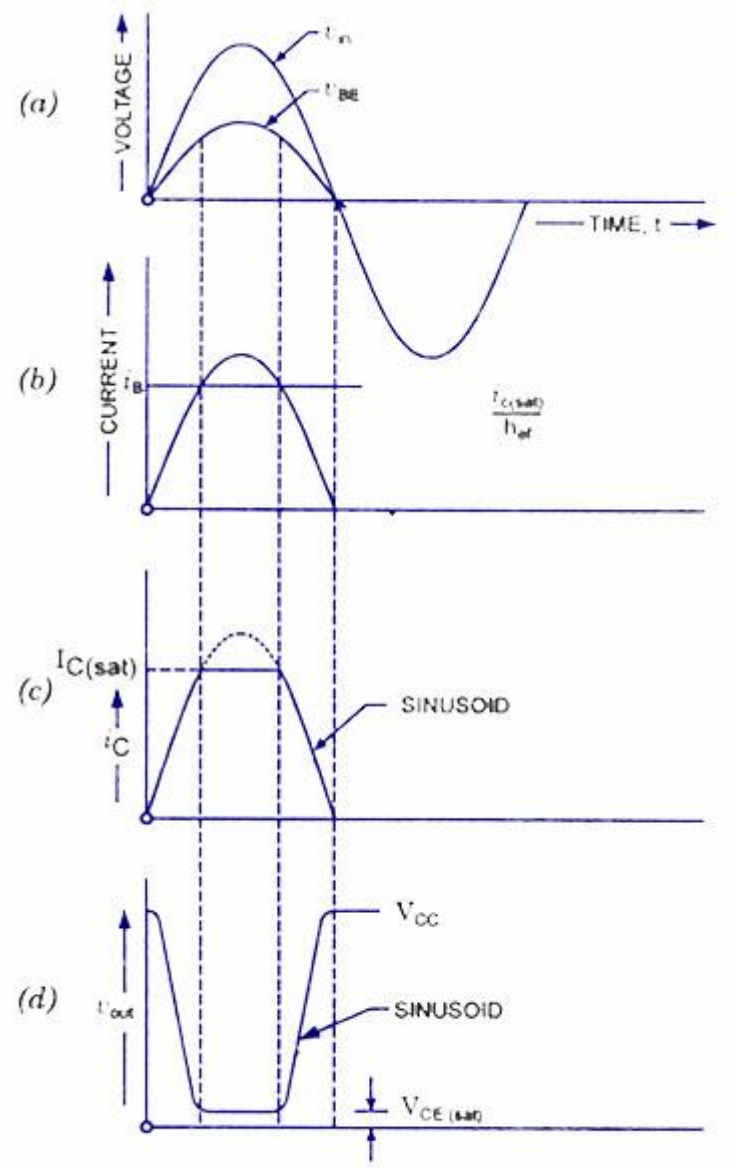
(c) Series clipper, negative peak clipping without reference



(e) Shunt clipper, negative base clipping above reference level

TRANSISTOR CLIPPER WAVEFORMS





Transistor Clipper Waveforms For Sinusoidal Input

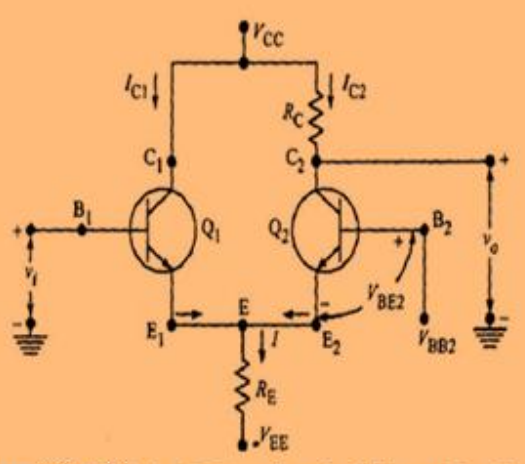


Figure 2.25 (a) An Emitter-Coupled Clipper(Double Clipper)

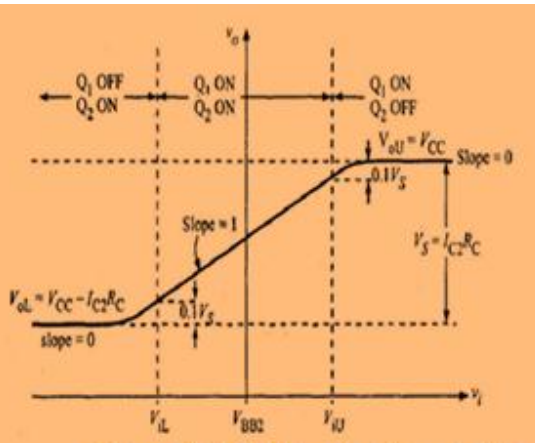


Figure 2.25(b) Transfer Charecteristics of the Emitter-Coupled Clipper

- From the above figure writing KVL around V_{BB2},V_{BE2} and $-V_{EE}$, the emitter current I is given by $I = I_1 + I_2 = \dfrac{V_{BB2} + V_{EE} - V_{BE2}}{R_E}$
- Here the base to emitter voltage V_{BE2} is $V_{BE} = V_\gamma << V_{BB2}$ *and* V_{EE}.
- Hence $I \approx I_1 + I_2 = \dfrac{V_{BB2} + V_{EE}}{R_E}$, which is constant for all time being the two voltages are constant dc voltages for a given circuit.
- When Q_1 ON and Q_2 OFF, i.e. $I_2 = 0$ and $I_1 = I$, the upper output limited level is $V_{OU} = V_{CC}$.
- And when Q_1 OFF and Q_2 ON, i.e. $I_1 = 0$ and $I_2 = I$, the lower output limited level is $V_{OL} = V_{CC} - I_{C2}R_C$.
- From the above circuit, we know that the emitter current $I_{E2} = I_2$ and is given by $I_2 = I_{B2} + I_{C2} = I_{C2}\left(1 + \dfrac{1}{h_{fe}}\right)$. And hence
- $I_{C2} = I_2 \Big/ \left(1 + \dfrac{1}{h_{fe}}\right)$. When $I_1 = 0$ and $I_2 = I$ i.e. Q_1 OFF and Q_2 ON
- $\therefore I_{C2} = I \Big/ \left(1 + \dfrac{1}{h_{fe}}\right)$.

- From the above Figure2.25 (a), writing KVL around the base to emitter of Q_1, emitter to base of Q_2 and the biasing voltage V_{BB2}, we get
- $v_i = V_{BE1} - V_{BE2} + V_{BB2}$ ---------- (A)
- Since the current varies exponentially with base to emitter voltage, the cutoff levels are approached asymptotically.
- Now, the upper input level V_{iU} to correspond to $I_1 = 0.9$ I and $I_2 = 0.1$ I, Q_1 ON and Q_2 OFF
- Similarly, the lower input level V_{iL} to correspond to $I_1 = 0.1$ and $I_2 = 0.9$ I, Q_1 OFF and Q_2 ON. We know that the base to emitter voltage is given by
- $V_E = \eta V_T \ln\left(1 - \frac{I_E + \alpha_I I_C}{I_{EO}}\right)$.
- Neglecting the small base current in the active region, $I_C \approx -I_E$, and since the second term in the parentheses is large compared with the first term, we can write
- $V_E \approx \eta V_T \ln\left(-\frac{(1-\alpha_I) I_E}{I_{EO}}\right)$.
- Since $V_{BE1} = V_E$ if $I_1 = -I_E$ and $V_{BE2} = V_E$ if $I_2 = -I_E$, considering the equation (A) we can write,
- $v_i = V_{BE1} - V_{BE2} + V_{BB2}$. Wring the values of V_{BE1} and V_{BE2} we get
- $v_i = V_{BB2} + \eta V_T \ln\left(\frac{(1-\alpha_I) I_1}{I_{EO}}\right) - \eta V_T \ln\left(\frac{(1-\alpha_I) I_2}{I_{EO}}\right) = V_{BB2} + \eta V_T \ln\left(\frac{I_1}{I_2}\right)$
- At $I_1 = 0.9$ I and $I_2 = 0.1$ I,
- $v_{iU} = V_{BB2} + \eta V_T \ln\left(\frac{0.9I}{0.1I}\right) = V_{BB2} + \eta V_T \ln 9$.
- Similarly, at $I_1 = 0.1$ I and $I_2 = 0.9$ I,

  $v_{iL} = V_{BB2} + \eta V_T \ln\left(\frac{0.1I}{0.9I}\right) = V_{BB2} - \eta V_T \ln 9$.
- In general, the total input voltage swing is $\Delta v_i = v_{iu} - v_{iL}$

- Which carry the output through its entire swing by $\Delta v_O = V_S = I_{C2} R_C$.
- $\therefore \Delta v_i = 2\eta V_T \ln 9 = 4.4\,\eta\, V_T$.
- This increment is proportional to the temperature, as V_T is volt equivalent temperature which depends on temperature.
- Here we assumed that the two transistors are identical.
- If this is not the case then the transfer characteristic will not be symmetrical with respect to V_{BB2}.
- Since the current switches from Q_2 to Q_1, with the total emitter current remaining constant, this circuit is often referred to as a "current – mode switch".

$$\left[V - 2v_O\left(\frac{T}{2}\right)\right]$$