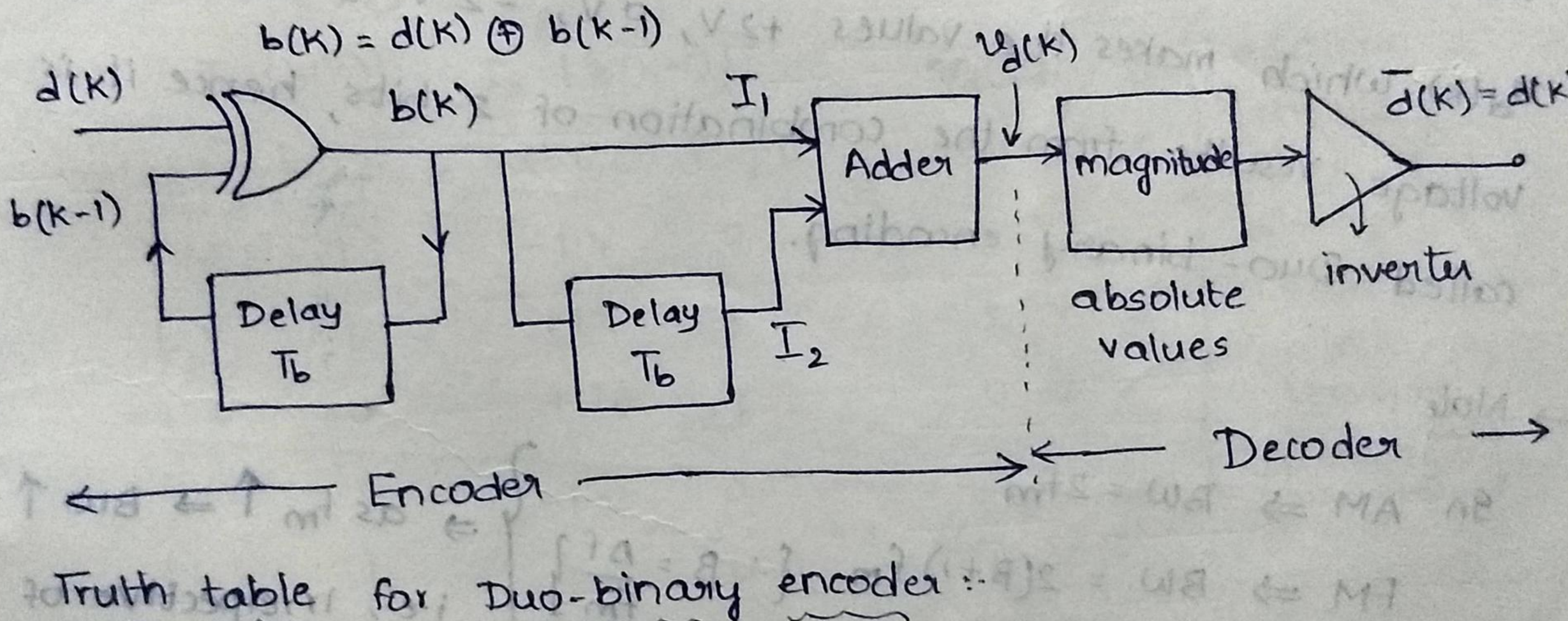
→ Duo-binary encoding :-



Truth table for Duo-binary encoder :-

Adder i/p 1 I_1		Adder i/p 2 I_2		Adder o/p $v_d(K)$	Magnitude o/p (inverter i/p)		inverter o/p $\bar{d}(K)$
voltage	logic	voltage	logic	voltage	voltage	logic	logic
-1 V	0	-1 V	0	-2 V	2 V	1	0
-1 V	0	+1 V	1	0 V	0 V	0	1
+1 V	1	-1 V	0	0 V	0 V	0	1
+1 V	1	+1 V	1	+2 V	2 V	1	0

From above truth table, $\bar{d}(k) = I_1 \oplus I_2$

$= b(k) \oplus b(k-1)$

From block diagram, $b(k) = d(k) \oplus b(k-1)$ $\Longrightarrow$ $= b(k) \oplus [b(k-1)]$

$= \{d(k) \oplus b(k-1)\} \oplus b(k-1)$

$= d(k) \oplus 0$

$\Rightarrow \boxed{\bar{d}(k) = d(k)}$ ie., d(k) is recovered back.

Let the bit sequence d(k) is having voltage representation as

d(k)	
voltage	logic
-1 V	0
+1 V	1

Hence the o/p of EX-OR gate b(k) makes excursion b/w -1 V & +1 V. Let I_1 & I_2 are the voltage representations for the bits b(k) & b(k-1) respectively.

The adder adds the i/p voltages I_1 & I_2 & provides o/p voltage $v_{d(k)}$ which makes the values +2 V, 0 V, -2 V & since $v_{d(k)}$ voltage results from the combination of 2 bits, hence it is called Duo-binary encoding.

→ Note :-

In AM $\Rightarrow$ BW = 2fm

FM $\Rightarrow$ BW = $2(\beta+1) f_m$ $\left\{\because \beta = \frac{\Delta f}{f_m}\right\}$

$= 2\Delta f + 2f_m$

$\Rightarrow$ as $f_m \uparrow \Rightarrow$ BW $\uparrow$ i.e., irrespective of modulation technique used as $f_m \uparrow \Rightarrow$ BW $\uparrow$

Duo binary encoding is a method of encoding a binary bit stream, which effects a reduction of max freq in comparison to max freq of unencoded data. Thus, if a carrier is amplitude or freq modulated by a duobinary encoded waveform, the BW of modulated waveform

will be smaller than if the unencoded data were used to AM or FM modulate the carrier.

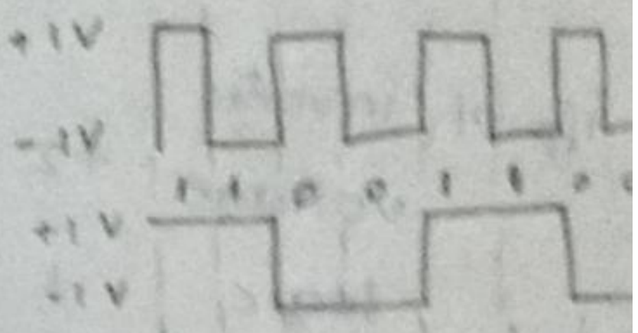
→ Let the original bit sequence (unencoded data) which is to be Txed using duo-binary encoding is $d(K)$ = 1 0 1 0 1 0 1 0 1 0. Find $b(K)$ & $v_d(K)$ with initial value of $b(K)$ as 0.

Ans] $d(K)$ 1 0 1 0 1 0 1 0 1 0

$b(K-1)$ 0 [1 1 0 0 1 1 0 0 1 1] → $b(K)$ 1 0 1 0 1 0 1 1

$\therefore b(K) = d(K) \oplus b(K-1)$

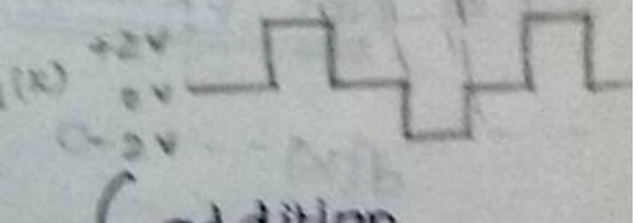
$= 1\ 1\ 0\ 0\ 1\ 1\ 0\ 0\ 1\ 1$



$I_1[b(K)]$ 1 1 -1 -1 1 1 -1 -1 1 1

$I_2[b(K-1)]$ -1 1 1 -1 -1 1 1 -1 -1 1

$v_d(K)$ 0 2 0 -2 0 2 0 -2 0 2



$v_d(K) = I_1 + I_2$ {in terms of voltages}

(or)

$I_1(b(K))$		$I_2[b(K-1)]$		$v_d(K)$	
voltage	logic	voltage	logic	voltage	addition should be always done in terms of Voltages
1 V	1	-1 V	0	0 V	
1 V	1	+1 V	1	2 V	
-1 V	0	+1 V	1	0 V	
-1 V	0	-1 V	0	-2 V	
+1 V	1	-1 V	0	0 V	
+1 V	1	+1 V	1	+2 V	
-1 V	0	+1 V	1	0 V	
-1 V	0	-1 V	0	-2 V	
+1 V	1	-1 V	0	0 V	
+1 V	1	+1 V	1	+2 V	

→ Show how duo-binary decoding is done when i/p $d(K)$ 0 1 1 1 0 1 0 1 1 is

a) precoded b) Not precoded.

Ans] a) precoded :- Assuming previous bit as '0'

d(k)		0	1	1	1	0	1	0	1	1
b(k-1)	0	[0	1	0	1	1	0	0	1	0] → b(k)
b(K)		-1	+1	-1	+1	+1	-1	-1	+1	-1
b(k-1)		-1	-1	+1	-1	+1	+1	-1	-1	+1
$v_d(k)$		-2	0	0	0	+2	0	-2	0	0

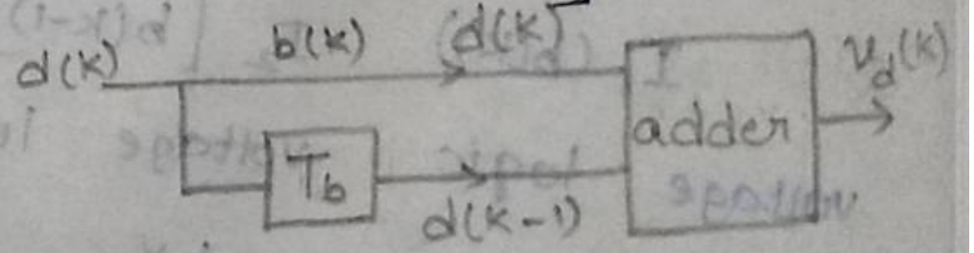
i/p of inverter voltage		+2	0	0	0	+2	0	+2	0	0
logic		1	0	0	0	1	0	1	0	0
o/p of inverter		0	1	1	1	0	1	0	1	1

$\therefore \quad \bar{d}(K) = d(K)$

b) Not precoded :- (without Ex-OR logic)

d(K)		0	1	1	1	0	1	0	1	1
d(k-1)	0	[0	1	1	1	0	1	0	1	1] → d(k)

↓ previous bit



d(k) voltage		-1	+1	+1	+1	-1	+1	-1	+1	+1
d(k-1) voltage		-1	-1	+1	+1	+1	-1	+1	-1	+1
		-2	0	+2	+2	0	0	0	0	+2

without Ex-OR logic we select

$v_d(K)$ = +2 V (1 bit)

= −2 V (0 bit)

= 0 V (bit is reversed from the previous state)

⇒ $v_d(K)$		-2	0	+2	+2	0	0	0	0	+2
∴ $\bar{d}(K)$		0	1	1	1	0	1	0	1	1

reverse state (0 → 1) reverse state (0 → 1)

$\therefore \bar{d}(K) = d(K)$