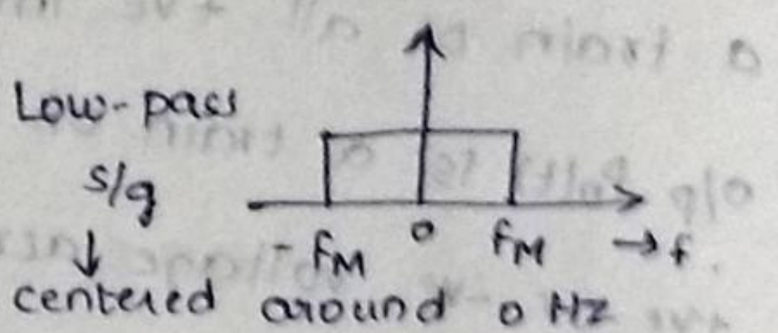
2. Digital Modulation Techniques

2. Digital Modulation and Transmission

Modulation: It is defined as the process by which some characteristics of a carrier are varied in accordance with a modulating s/g.

In digital comms, the modulating s/g consists of binary data or a M-ary encoded version of it. This data is used to modulate a carrier wave (usually sinusoidal) with fixed freq.

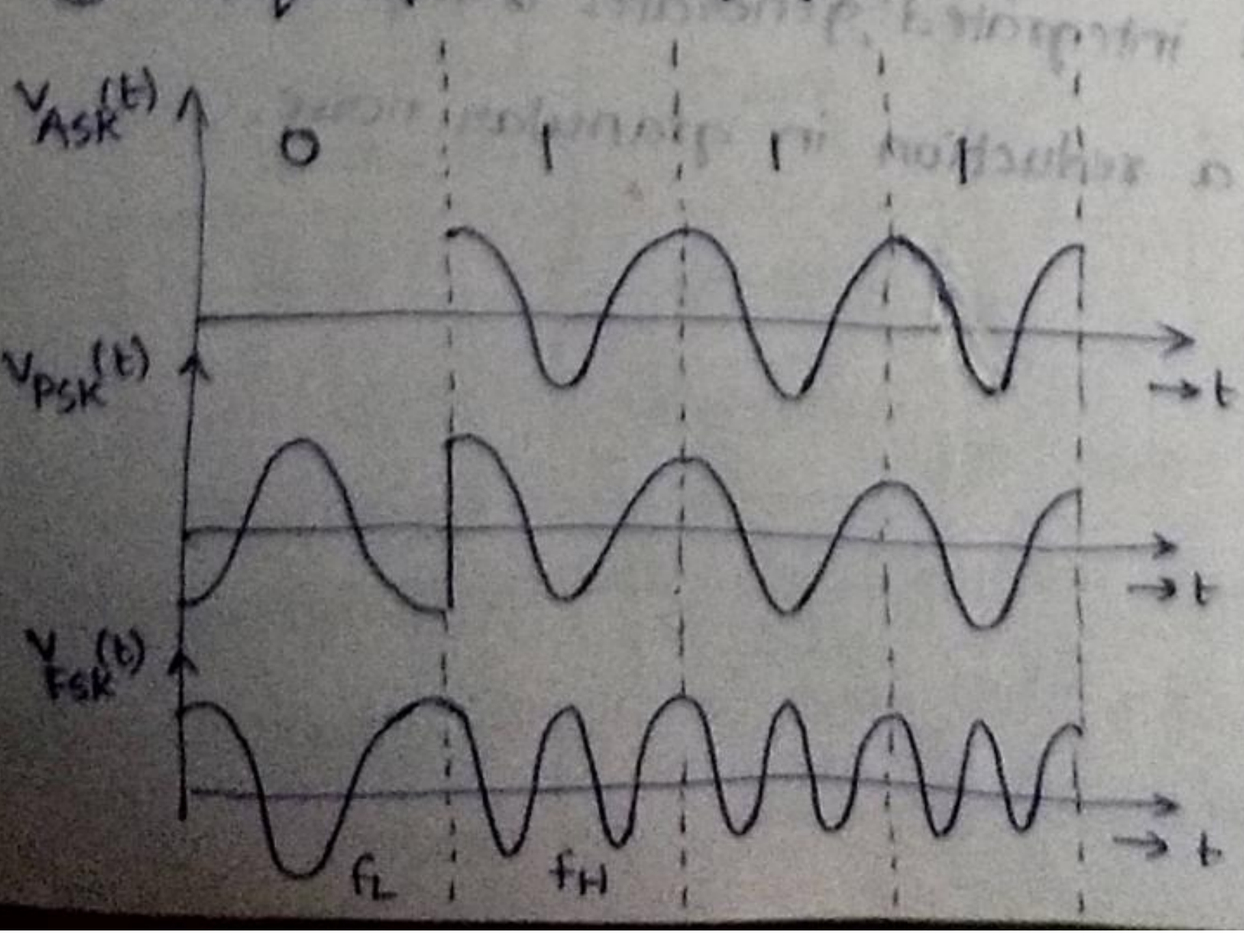
→ When it is required to Tx digital s/g's on Bandpass channel, amp or freq or phase of sinusoidal carrier is varied in accordance with the incoming digital data.

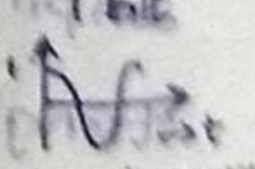


Since the digital data is in discrete steps, the modulation of bandpass sinusoidal carrier is also done in discrete steps. Due to this reason, this type of modulation (i.e., Digital modulation) is also known as switching or signalling.

→ There are 3 basic digital modulation techniques :-

1. Amplitude shift keying (ASK) ⟺ analogous to AM
2. Phase shift keying (PSK) ⟺ " " PM
3. Frequency shift keying (FSK) ⟺ " " FM





Carrier : $\cos \omega_0 t$

ASK : Noise interference is more.

1 bit → presence of carrier

0 bit → absence of carrier

PSK :-

1 bit → 0 phase

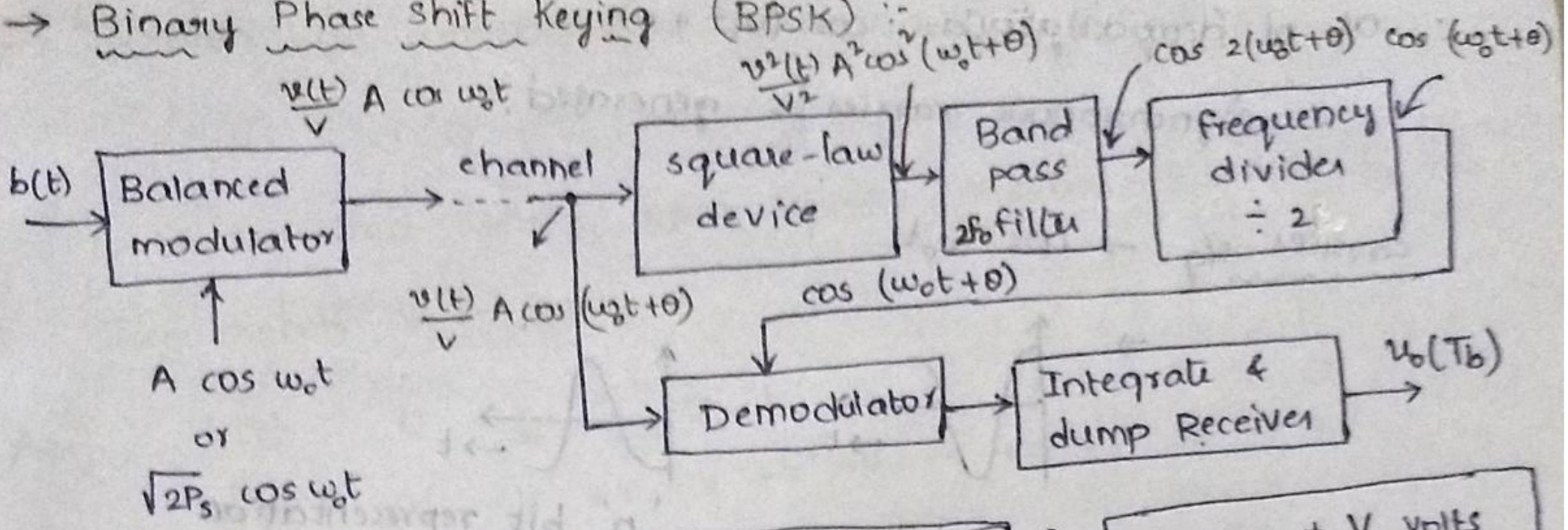
0 bit → π phase

FSK :-

1 bit → f_H ⇒ time ↓ of 1 cycle

0 bit ⇒ f_L

→ Binary Phase shift keying (BPSK) :-



Binary s/g, $b(t)$ = 1 represents $+V$ volts
= 0 represents $-V$ volts
↓
stream of binary digits

$\therefore v(t) = \pm V$ volts
$b(t)$ = '1' or '0' bit

$$v_{BPSK}(t) = \pm A \cos \omega_0 t$$
or
$$\sqrt{2P_s} \cos(\omega_0 t + \phi)$$

carrier angular freq $\omega_0 = 2\pi f_0$ → carrier freq

where $\phi = 0$ for Txion of 1 bit
$= \pi$ for Txion of 0 bit

$\Rightarrow$ A is amplitude

P_s is power of s/g

$P_s = A^2/2 \Rightarrow A = \sqrt{2P_s}$

// Balanced modulator o/p $(v_{BPSK}(t))$

= product s/g

$= b(t) A \cos \omega_0 t$ (or) $\sqrt{2P_s}\, b(t) \cos \omega_0 t$

$= \frac{v(t)}{V} A \cos \omega_0 t$ $\{\because A = \sqrt{2P_s}\}$

$\{\because v(t) = \pm V$ volts $\Rightarrow \frac{v(t)}{V} = \frac{\pm V}{V} = \pm\}$

$\pm \pm A \cos \omega_0 t$ or $\sqrt{2P_s}\, b(t) \cos \omega_0 t$

$\therefore b(t)$ is '1' $\Rightarrow \phi = 0 \Rightarrow \sqrt{2P_s} \cos \omega_0 t$ ✓

'0' $\Rightarrow \phi = \pi \Rightarrow \sqrt{2P_s} \cos(\omega_0 t + \pi)$

$\Rightarrow -\sqrt{2P_s} \cos \omega_0 t$ ✓

P_s → mean square value of $A \cos \omega_0 t$

$$P_s = \frac{1}{T_s} \int_0^{T_s} A^2 \cos^2 \omega_0 t \, dt$$

$$= \frac{A^2}{T_s} \int_0^{T_s} \left(\frac{1+\cos 2\omega_0 t}{2}\right)$$

$$= \frac{A^2}{2T_s} [T_s + 0]$$

$= A^2/2$ ✓

$\Rightarrow \pm \sqrt{2P_s} \cos \omega_0 t$

$\Rightarrow \pm A \cos \omega_0 t$ //

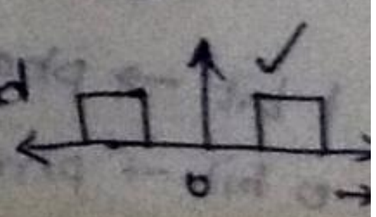
At Rxing end :-

o/p of square-law device $= \frac{v^2(t)}{V^2} A^2 \cos^2(\omega_0 t + \theta)$

$= \frac{v^2(t)}{V^2} A^2 \left[\frac{1 + \cos 2(\omega_0 t + \theta)}{2}\right]$

$\therefore$ o/p of BPF $\simeq \cos 2(\omega_0 t + \theta)$

{BPF allows band of frequencies

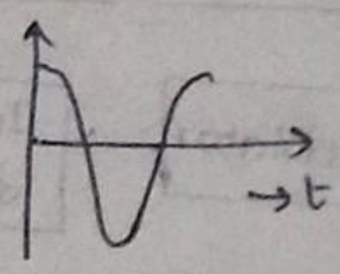


∴ O/p of frequency divider = $\cos(\omega_0 t + \theta)$

∴ Synchronous carrier is generated.

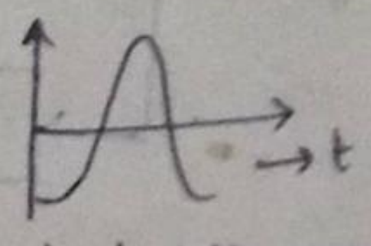
carrier s/g → $\cos \omega_0 t$

⇒



1 bit

⇒ phase $\phi = 0$



'0' bit representation

$\phi = \pi$

adv :- 1) efficient
2) Have high bit rates
3) P_e is low i.e, min probability of error

disad :- Hardware design { synchronous carrier is to be generated for recovery of b(t) }

Notes :-

To modulate a binary PCM s/g generate a binary s/g b(t) which takes the values ± V volts over 'i' bit interval

The phase of the carrier is '0' for Txion of '1' bit & is 'π' radians for Txion of '0' bit.

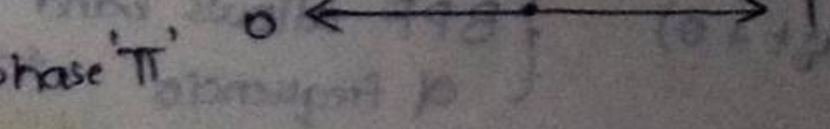
The Rxed s/g is in the form of $\frac{v(t)}{V} A \cos(\omega_0 t + \theta)$

where θ is phase angle which depends on effective length of the channel.

In BPSK, a synchronous carrier is needed to be generated & applied to a demodulator along with the Rxed s/g. An integrate & dump Rxer detects status of incoming each bit by collecting the sample value over each bit interval.

Hence the BPSK Rxer requires hardware to generate a carrier but it provides min. bit error probability.

1 bit → phase '0'
0 bit → phase 'π'



phasor diagram for BPSK

→ The data b(t) consists of a bit string in which

b(t) = 0 0 1 0 1 0 0 1 1 0 1 0

is to be fixed using BPSK system. Assume bit rate $F_b = f_0$

Then sketch $V_{BPSK}(t)$.

Ans]

b(t)	0	0	1	0	1	0	0	1	1	0	1	0
v(t)	-V	-V	+V	-V	+V	-V	-V	+V	+V	-V	+V	-V

$V_{BPSK}(t) = \frac{V(t)}{V} \cos \omega_0 t$ where $V(t) = \pm V$ volts

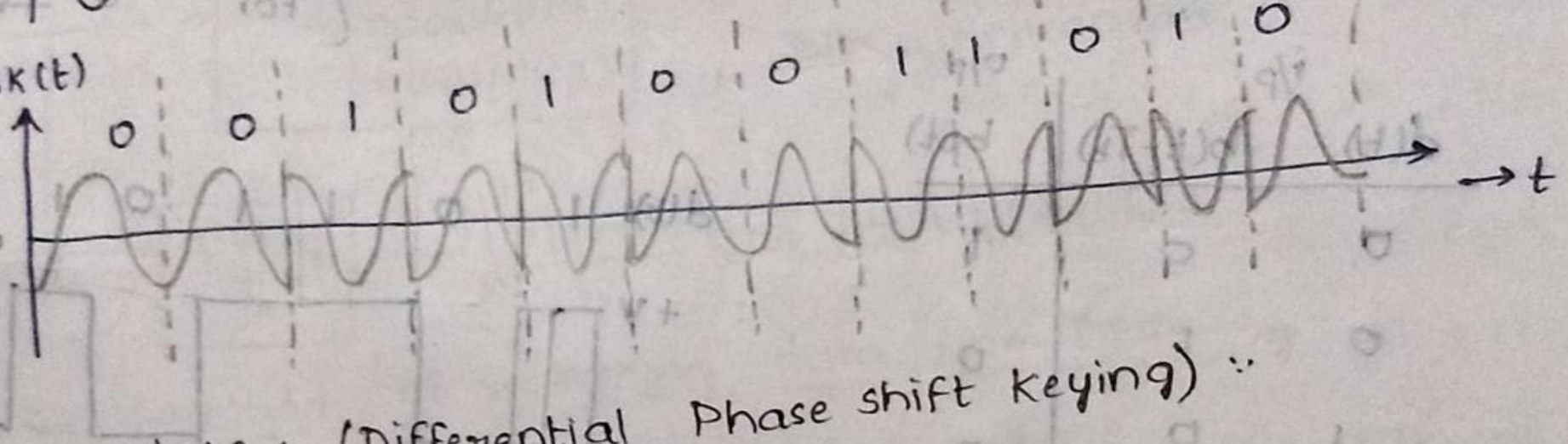
$\omega_0 = 2\pi f_0$

↓ carrier angular freq

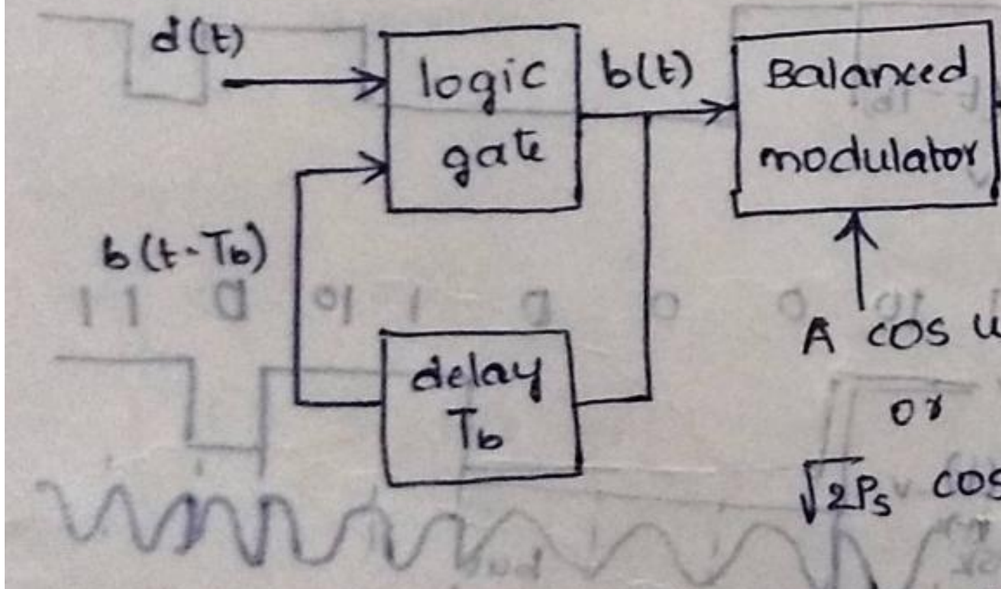
↓ carrier freq.

'1' bit

'0' bit



→ DPSK system :- (Differential Phase shift keying) :-



$V_{DPSK}(t) = b(t)\sqrt{2P_s}\cos\omega_0 t$

$= \pm\sqrt{2P_s}\cos\omega_0 t$

Txer

$\frac{V(t)}{V} = b(t)$

$\Rightarrow \frac{\pm V}{V} = b(t)$

$\Rightarrow b(t) = \pm$ ✓

where d(t) is actual bit sequence

b(t) is modified bit sequence.

DPSK requires less hardware compared to BPSK [∵ there is no generation of carriers at the end i.e, the need to provide sync at demodulator to detect BPSK s/g], it avoids carriers but the s/g in DPSK is determined on the basis of s/g Rxed in 2 bit intervals. Hence noise in one bit interval causes errors in 2-bit determination & hence causes more bit error probability.

At the Rxing end, if the DPSK sequence b(t) is received then by using a logic gate law to that of gate used in Txer, the actual bit sequence d(t) can be recovered.

logic-1 :- when d(t) = 1, there is no change in state of b(t) but when d(t) = 0, there is change in state of b(t) during that interval.

{ d(t) = 1 ⇒ change in b(t) ✗
{ d(t) = 0 ✓

d(t) 1 0 1 1 0 1 0 0 1

b(t) 1 1 0 0 0 1 1 0 1 1 ← b(t)

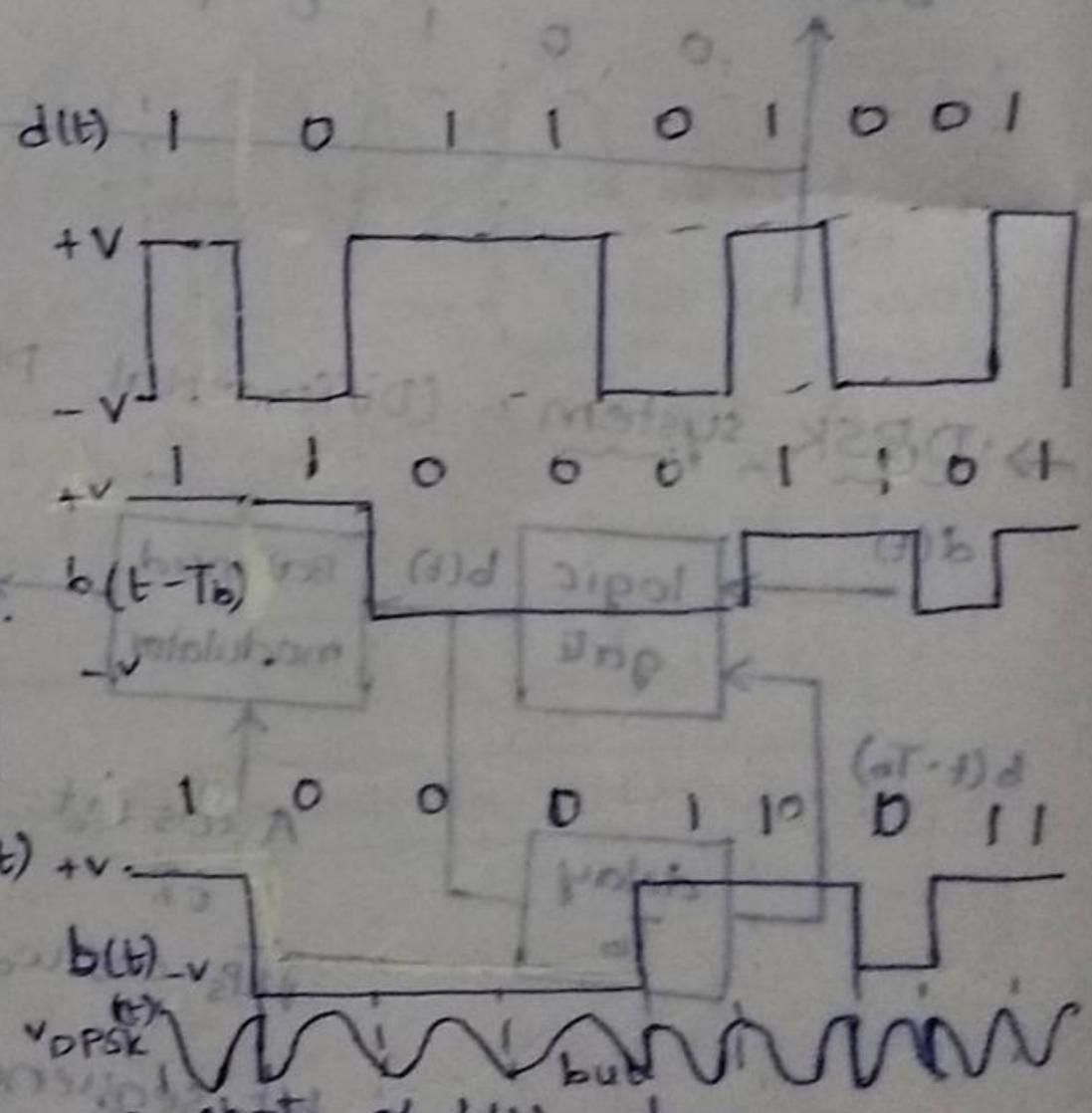
Phase 0 0 π π π 0 0 π 0 0

{ Phase for bit '1' → 0, '0' → π

i/p d(t)	i/p b(t-Tb)	o/p b(t)
0	0	1
0	1	0
1	0	0
1	1	1

∴ Ex-NOR logic is used.

⇒ if d(t) = 1; b(t) = b(t-Tb)
= 0; b(t) = $\overline{b(t-T_b)}$



logic-2 :-

when d(t) = 1, there is change in state of b(t), when d(t) = 0, there is no change in state of b(t)

d(t) 1 0 1 1 0 1 0 0 1

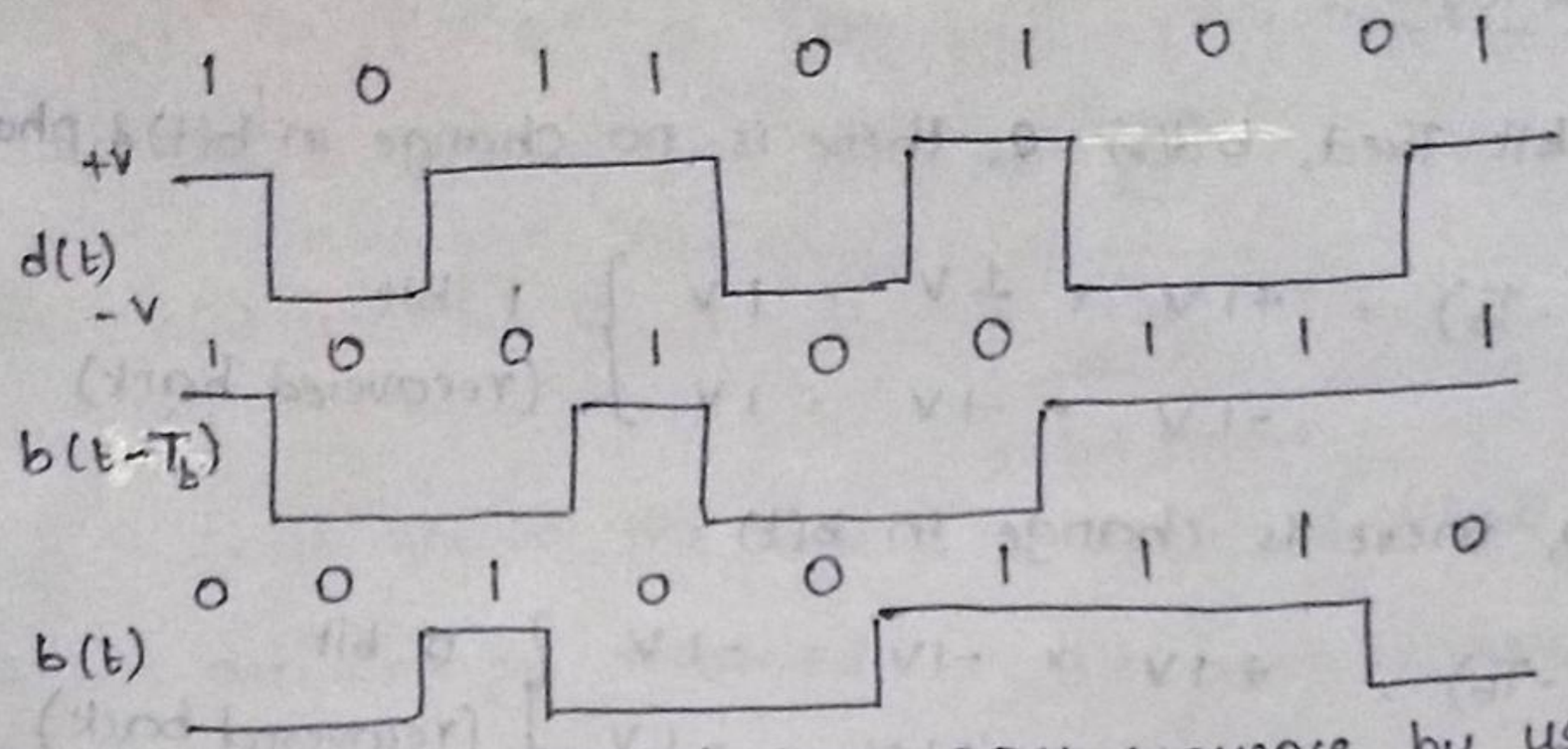
b(t) 1 0 0 0 1 1 0 1 1

{ d(t) = 1 ✓
{ = 0 ✗

i/p d(t)	i/p b(t-Tb)	o/p b(t)
0	0	0
0	1	1
1	0	1
1	1	0

⇒ if d(t) = 1, b(t) = $\overline{b(t-T_b)}$
d(t) = 0, b(t) = b(t-Tb)

∴ EX-OR logic is used



→ d(t) can be recovered from DPSK sequence by using 2 methods :-

→ ① DPSK Rxer :-

① DPSK Rxer

② DEPSK Rxer

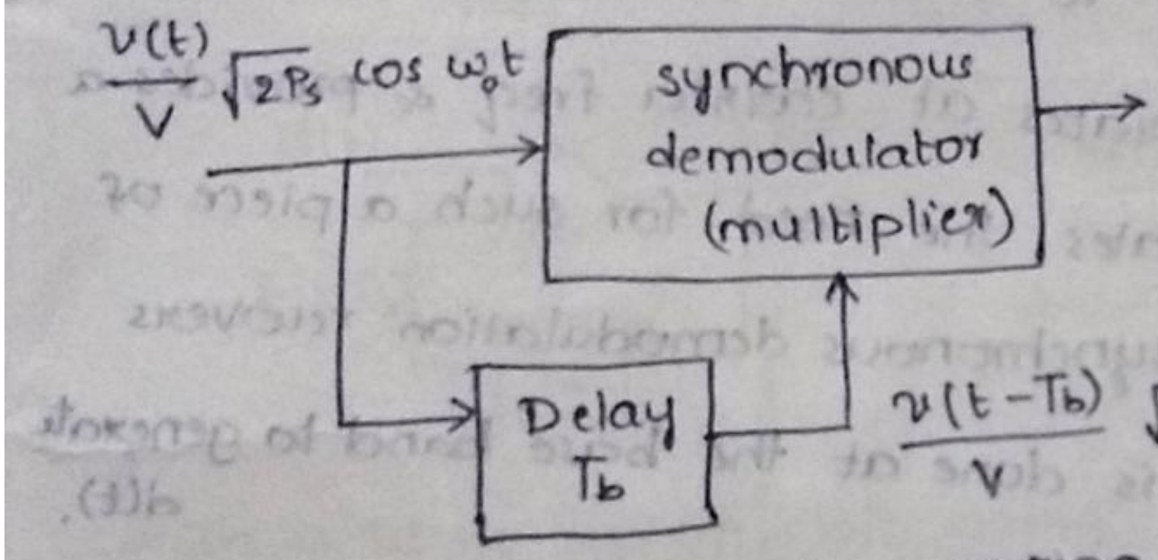


fig :- Method of recovering data from DPSK s/g

O/p of demodulator = $\frac{v(t)}{V}\sqrt{2P_s}\cos\omega_0 t \cdot \frac{v(t-T_b)}{V}\sqrt{2P_s}\cos\omega_0(t-T_b)$

$= b(t)\,b(t-T_b)\,P_s\,2\cos\omega_0 t\cos\omega_0(t-T_b)$

$= b(t)\,b(t-T_b)\,P_s\left[\cos(2\omega_0 t-\omega_0 T_b)+\cos\omega_0 T_b\right]$

$= b(t)\,b(t-T_b)\,P_s\left[\cos 2\omega_0\left(t-\frac{T_b}{2}\right)+\cos\omega_0 T_b\right]$

$= b(t)\,b(t-T_b)\,P_s\underbrace{\left[\cos\omega_0 T_b\right.}_{\text{required o/p s/g}} + \underbrace{\left.\cos 2\omega_0\left(t-\frac{T_b}{2}\right)\right]}_{\text{double freq term suppressed by o/p integrator}}$

$\left\{\frac{v(t)}{V}=b(t),\ \frac{v(t-T_b)}{V}=b(t-T_b)\right\}$

The double freq term is suppressed by o/p integrator & select $\boxed{\omega_0 T_b = 2n\pi}$

where n is integer, such that $\boxed{\cos\omega_0 T_b = 1}$ so that s/g will be as large as possible.

{ cos max value = 1
cos 0° or cos 360° = 1 ⇒ 2nπ ✓ }

For EX-NOR logic :-

① If actual bit Txed, d(t) = 1, there is no change in b(t) & phase

$$v(t)\,v(t-T_b) = \begin{cases} +1V \times 1V = 1V \\ -1V \times -1V = 1V \end{cases}$$ } 1 bit (recovered back)

② If d(t) = 0, there is change in b(t)

$$v(t)\,v(t-T_b) = \begin{cases} +1V \times -1V = -1V \\ -1V \times +1V = -1V \end{cases}$$ } 0 bit (recovered back)

② DEPSK Rxer :- (Differentially Encoded Phase Shift Keying) :-

It is the 2nd method to recover d(t). DPSK demodulator requires a device which operates at carrier freq & provides a delay T_b. But DEPSK eliminates the need for such a piece of hardware. In this system, synchronous demodulation recovers the s/g & decoding of b(t) is done at the base band to generate d(t).

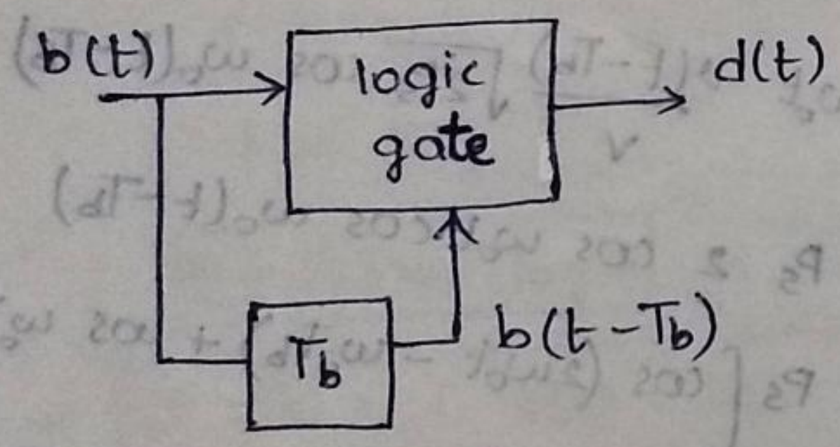


Fig :- Baseband decoder to obtain d(t) from b(t)

The Txer of DEPSK system is same as that of DPSK system but at the Rxing end DEPSK sequence b(t) can be recovered back just like BPSK Rxer. The recovered s/g b(t) is then applied to one of the i/ps of two i/p logic gate which is same as that of logic gate used at Txer & $b(t-T_b)$ is applied to the other i/p of this logic gate such that the actual bit sequence d(t) can be recovered back. Let X-OR logic is used

b(t)	1	1	0	0	0	1	1	0	1	1
$b(t-T_b)$		1	1	0	0	0	1	1	0	1
$d(t) = b(t) \oplus b(t-T_b)$		0	1	0	0	1	0	1	1	0

b(t)	b(t-T)	%
0	0	0
0	1	1
1	0	1
1	1	0

b(t)	1	1	0	0	[1]	1	1	0	1	1	
b(t-Tb)		1	1	0	0	[1]	1	1	0	1	1
d(t) = b(t) ⊕ b(t-Tb)	0	1	0	1	0	0	1	1	0		

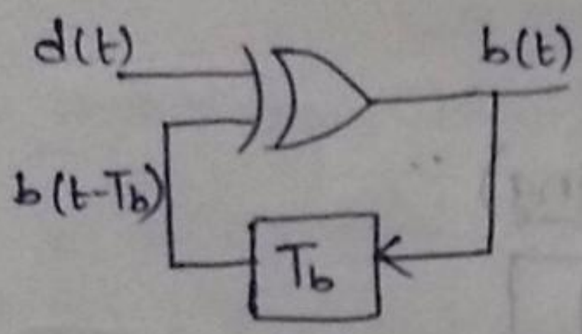
→ 1-bit error

2-bit errors

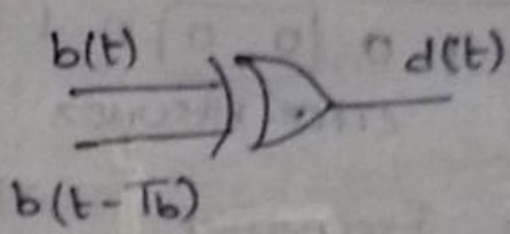
∴ if one of the bits is wrongly detected due to noise, 2 bits are wrongly recovered. ∴ Bit error is very high in this DPSK which is upto 2-bit extension, but in BPSK there is only 1 bit error.

→

Txer



Rxer



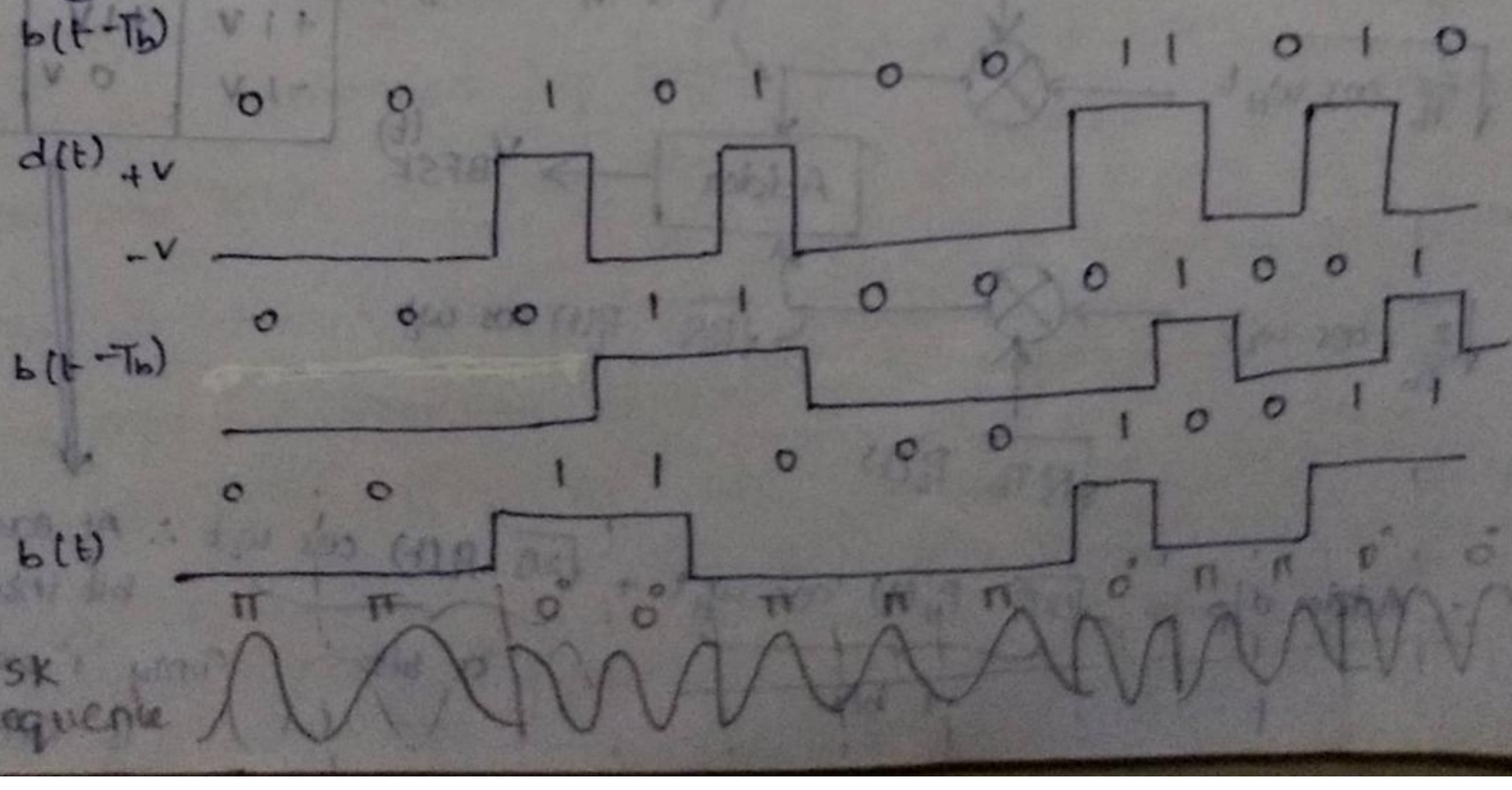
→ In a DPSK system, bit string d(t) : 0010100111010 is Txed, obtain b(t) & show that d(t) can be recovered back use x-OR logic.

Ans]

d(t)		0	0	1	0	1	0	0	1	1	0	1	0
b(t)	0	0	0	1	1	0	0	0	1	0	0	1	1
b(t-Tb)		0	0	0	1	1	0	0	0	1	0	0	1
		0	0	1	0	1	0	0	1	1	0	1	0

DPSK sequence
$b(t)\sqrt{2P_b}\cos\omega_0 t$
$= \pm\sqrt{2P_b}\cos\omega_0 t$

d(t) = b(t) ⊕ b(t-Tb)		
0	0	+V
0	1	-V
1	0	-V
1	1	+V



In a DEPSK Rxer, the received sequence, 0 1 1 0 1 1 0 0, then
→ Let b(t) using an X-OR logic is

a) Find reconstructed bit sequence.

b) Due to presence of noise, b(t) is recovered as 0 1 1 1 1 0 0

then detect d(t) & indicate the bits which are wrongly detected

Ans] @

b(t)	0	1	1	0	1	1	0	0
b(t-Tb)	0	1	1	0	1	1	0	0
d(t) = b(t) ⊕ b(t-Tb)	1	0	1	1	0	1	0	

(b)

b(t)	0	1	1	[1]	1	1	0	0
b(t-Tb)	0	1	1	[1]	1	1	0	0
	1	0	[0	0]	0	1	0	

error bits