→ Differential Pulse Code Modulation (DPCM)

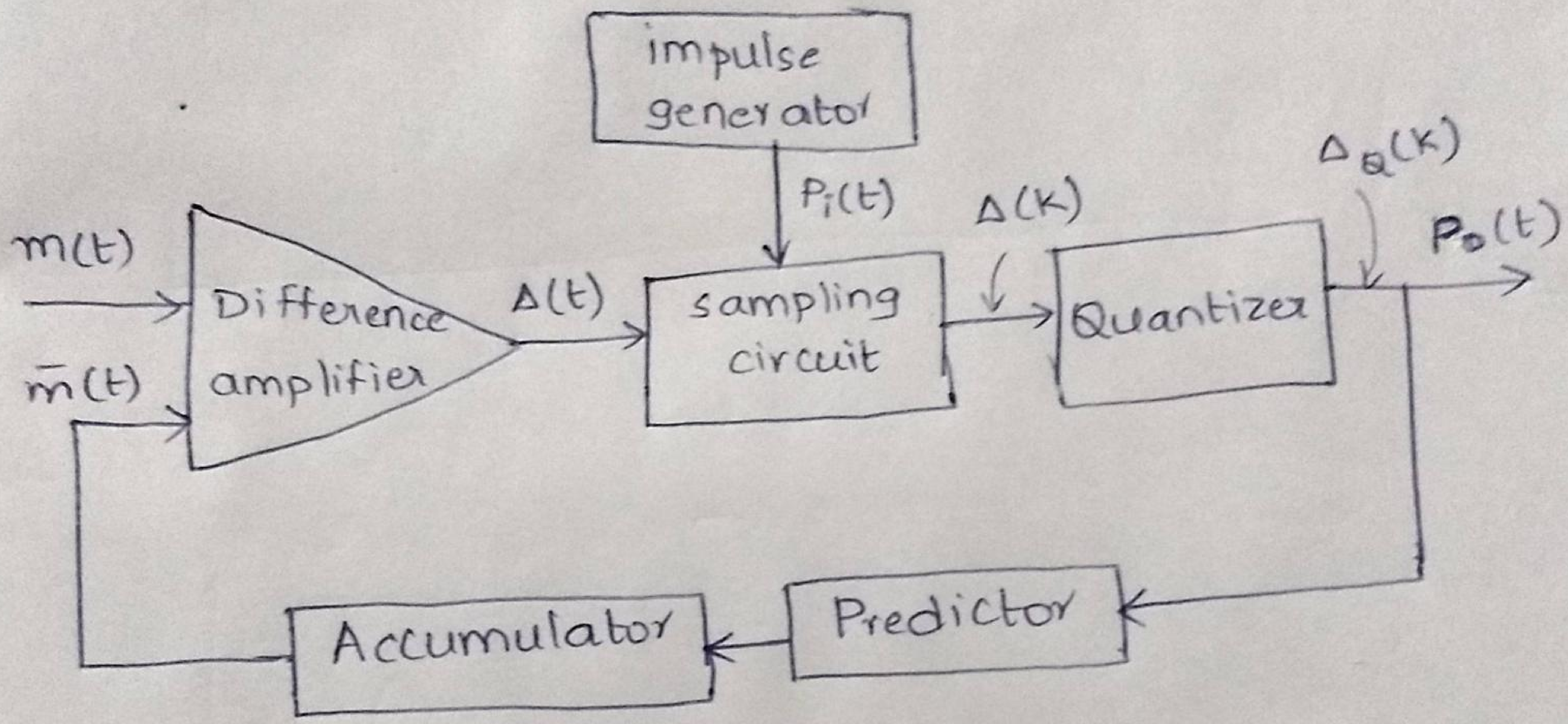


fig a) Transmitter

Here, $\Delta(t)$ is difference s/g ; $\bar{m}(t)$ is approximation of $m(t)$

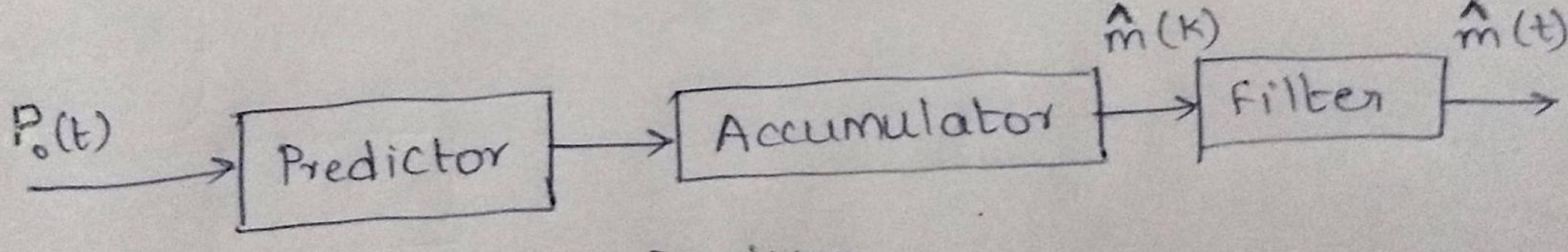


fig b) Receiver

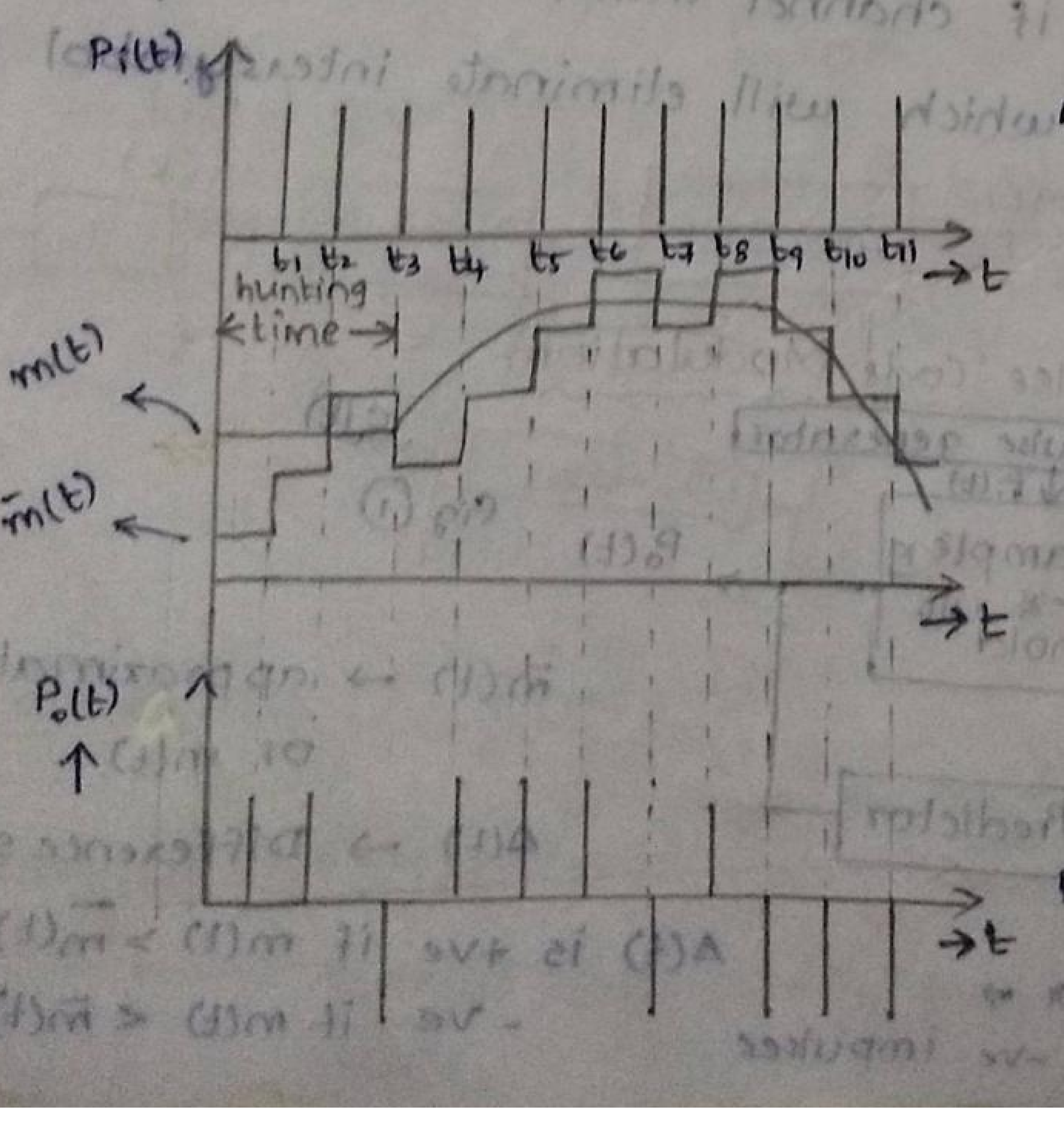
Fig : Representation of basic principle of differential PCM

In DPCM, instead of m(t) we Tx difference s/g $\Delta(t)$ so called DPCM. In DPCM, the word length is less than that of PCM system, since for PCM, the base band s/g m(t) lies in the voltage range V_H & V_L, but DPCM extends to a narrow range, hence it requires less no. of Quantization levels.

The o/p of difference amplifier can be determined from the s/g variations of m(t) over two successive clock intervals & $\Delta(t)$ is +ve if $m(t) > \bar{m}(t)$ &

$\Delta(t)$ is -ve if $m(t) < \bar{m}(t)$

Hence, the o/p of sampling ckt $P_o(t)$ represents a +ve impulse if $\Delta(t)$ is +ve & represents a -ve impulse if $\Delta(t)$ is -ve. By using the knowledge of previous samples, predictor allows to predict with some probability being correct & the range of next increment. {Predictor is a sophisticated system needed to incorporate the facility for storing past differences & for carrying out some algorithm to predict the next required increment}.



At $t = t_1$, $\Delta(t)$ is +ve

$t = t_2$, $\Delta(t)$ is +ve

$t = t_3$, $\Delta(t)$ is -ve

fig (2) indicates the generation of DPCM s/g $P_o(t)$ which represents the base band s/g m(t)

fig (2)

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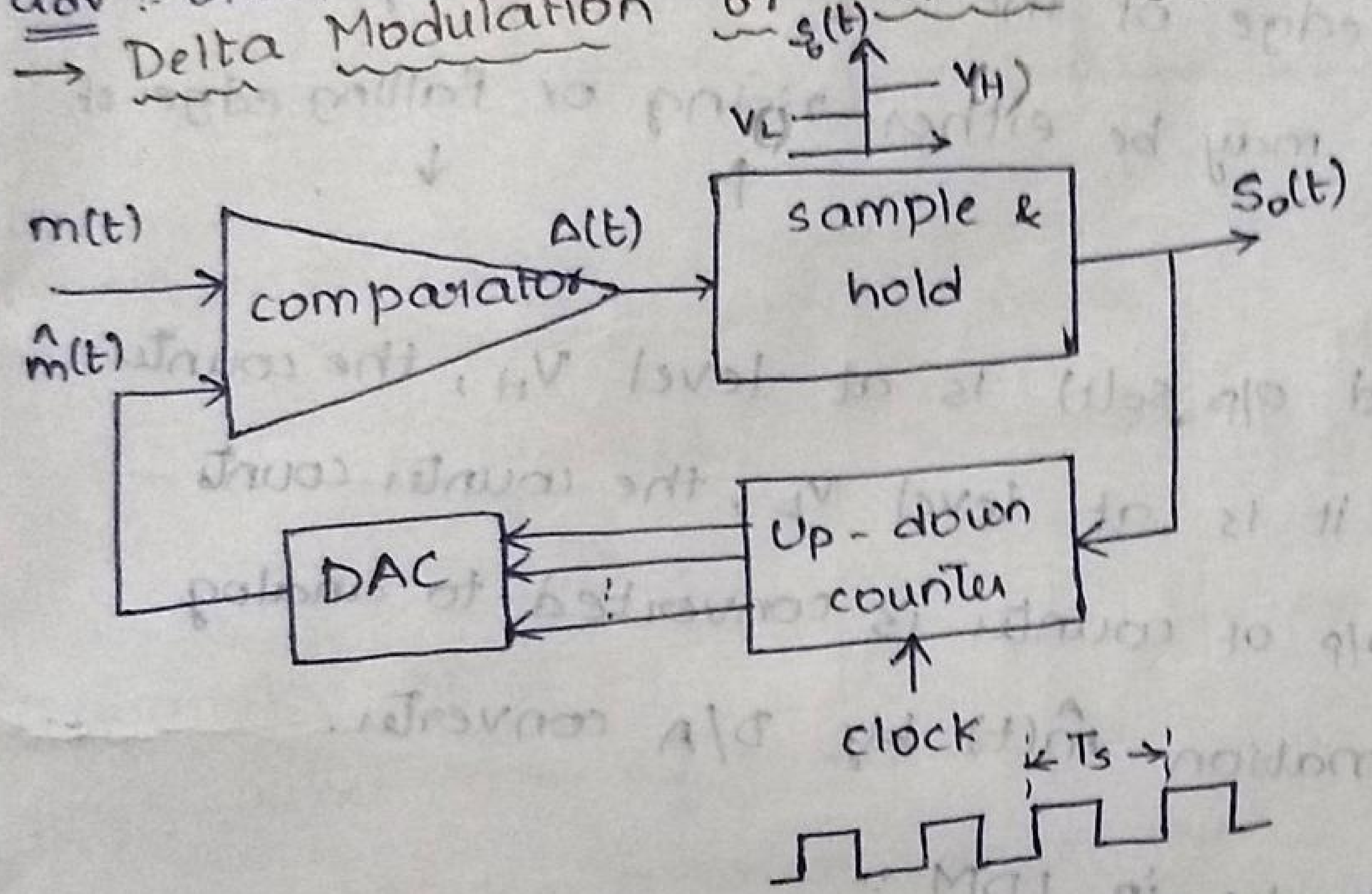
(The approximate s/g $\bar{m}(t)$ should follow the base band s/g $m(t)$ then $P_0(t)$ represents the base band s/g. Since the system is using <u>fixed step size</u>, when the s/g variation of $m(t)$ is higher than step size then $\bar{m}(t)$ may not follow $m(t)$. Hence during that interval $P_0(t)$ is not truly representing the base band s/g $m(t)$ in that interval.

<u>adv</u> :- DPCM can operate at $\simeq \frac{1}{2}$ of bit rate of PCM, thus saving spectral space

→ <u>Delta Modulation</u> <u>or</u> <u>Linear</u> <u>Delta Modulation</u> (LDM/DM) :-



$\Delta(t) = m(t) - \hat{m}(t)$

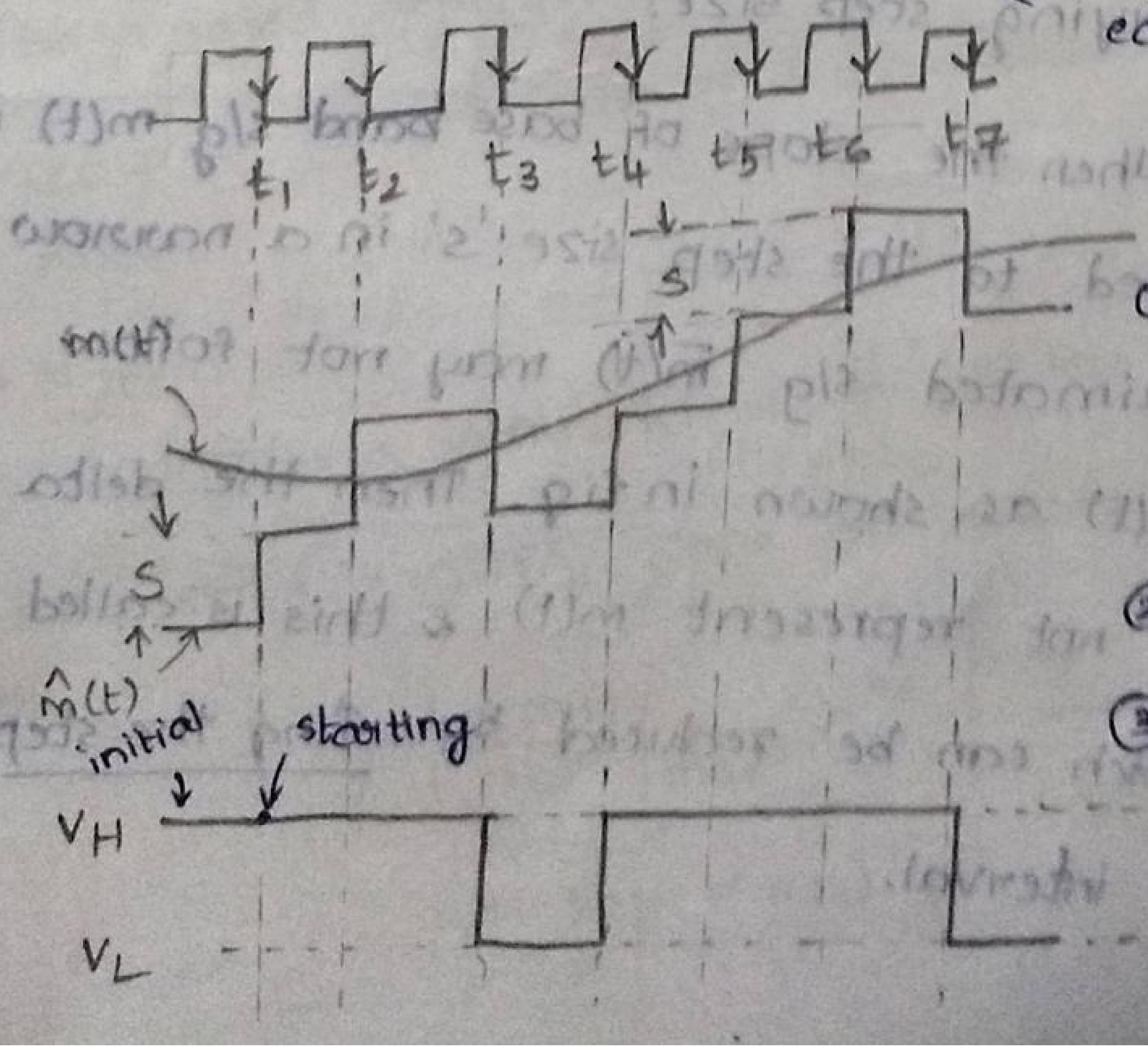
$S_o(t)$ is V_H if $\Delta(t)$ is +ve

is V_L if $\Delta(t)$ is −ve.

$\hat{m}(t)$ → Quantized approximation of $m(t)$

Delta modulation is a DPCM scheme, in which the difference s/g $\Delta(t)$ is encoded into just a single bit which provides just for two possibilities, used to increase or decrease the estimate $\hat{m}(t)$.

← Assuming the active clock edge is falling edge



For a time <u>preceeding</u>

① t_1, $m(t) > \hat{m}(t) \rightarrow S_o(t) = V_H$ & $\hat{m}(t)$ is incremented by s

② t_2, $m(t) > \hat{m}(t) \rightarrow$ "

③ t_3, $m(t) < \hat{m}(t) \rightarrow S_o(t)$ is V_L & $\hat{m}(t)$ is decremented by s.

The base band s/g m(t) & its quantized approximation $\hat{m}(t)$ are applied as i/ps to comparator which makes a comparison b/w i/ps. The comparator o/p $\Delta(t)$ is

$S_0(t)$ is V_H when $m(t) > \hat{m}(t)$ &

V_L when $m(t) < \hat{m}(t)$

The Up-down counter increments or decrements its count by 1 at each active edge of the clock (Depending on hardware design of counter, it may be either rising or falling edge of the clock).

When the Txed o/p $S_0(t)$ is at level V_H, the counter counts up & when it is at level V_L, the counter counts down. The digital o/p of counter is converted to analog quantized approximation $\hat{m}(t)$ by D/A converter.

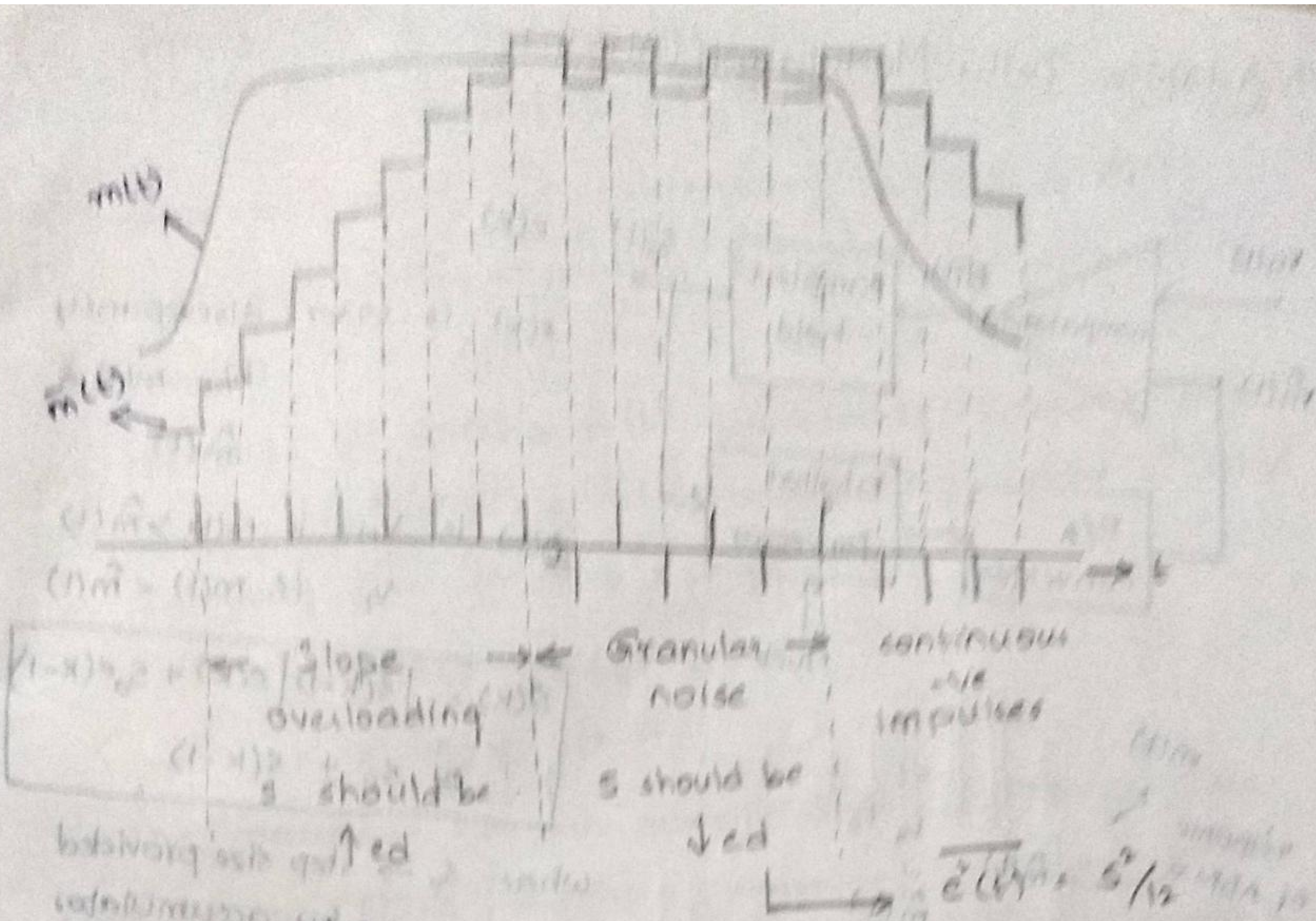
There are 2 drawbacks in LDM :-

① Slope overloading :- can be avoided by ↑ing step size at that particular time

② Granular noise :- can be reduced by ↓ing step size.

These two modifications are done in ADM system by taking continuously varying step size.

① Slope overloading :- When the slope of base band s/g m(t) is very high when compared to the step size 's' in a narrow rate, then the approximated s/g $\hat{m}(t)$ may not follow the base band s/g m(t) as shown in fig. Then the delta modulated o/p may not represent m(t) & this is called slope overloading which can be reduced by ↑ing the step size 's' during this interval.



② Granular noise :-

when the s/g variation is very small over a wide range, then by reducing step size, the approximate s/g m̃(t) follows m(t). The reduction in step size reduces the presence of Granular noise in that range.

Hence by using ADM or CVSDM, the step size 'S' can be varied depending upon the s/g variations of m(t) which reduces the effects of both slope overloading & granular noise.

→ **Note** :-

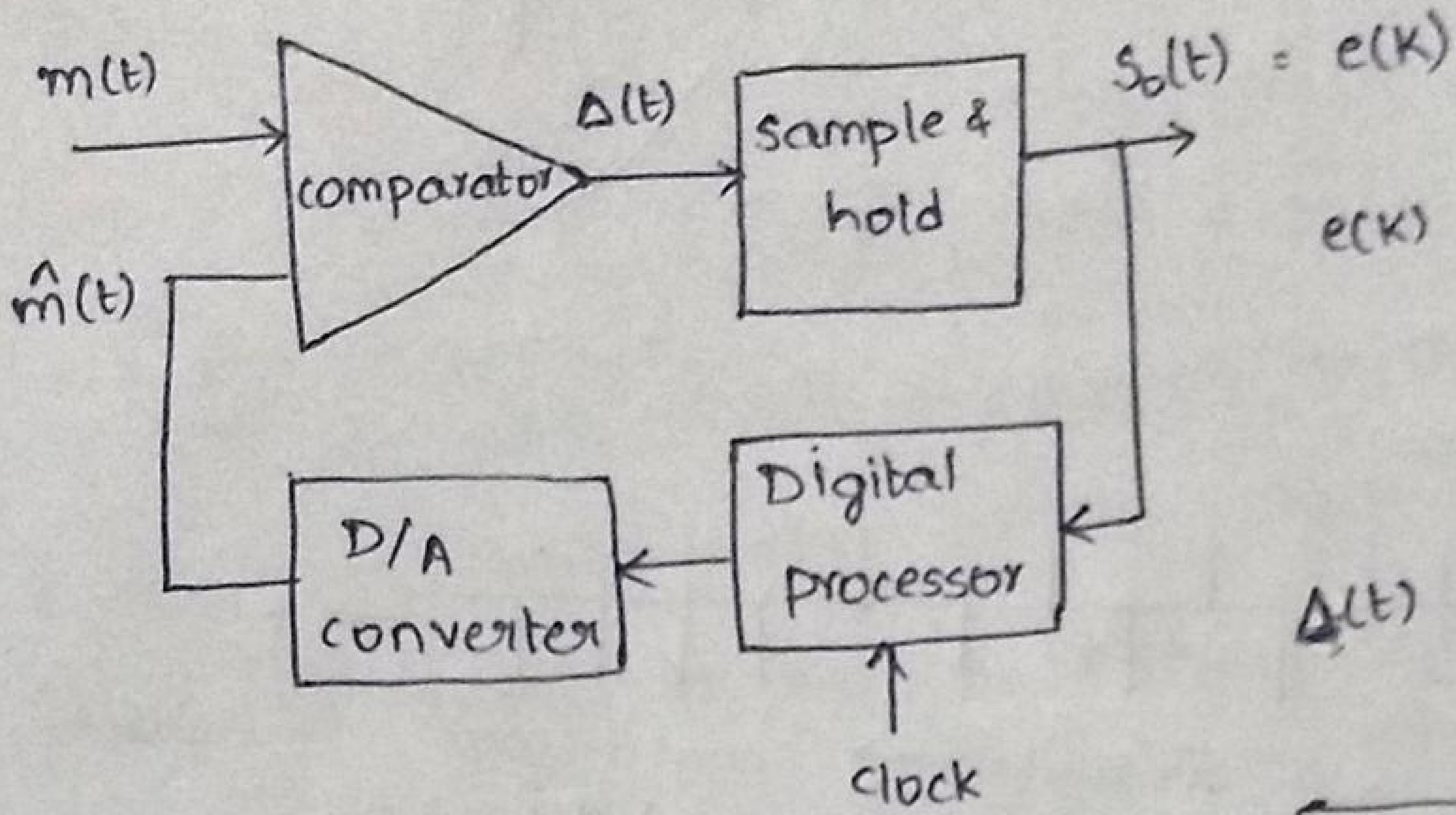
consider a sinusoid of Amplitude 'A' & frequency 'f' having max slope = $2\pi fA$. Slope overloading can be avoided

if $\frac{S}{T} \geq \underbrace{\left|\frac{d\,m(t)}{dt}\right|_{max}}_{\text{max slope of } m(t)}$ ⇒ $\boxed{Sf_s \geq 2\pi fA}$ ⇒ $f_s \geq \frac{2\pi fA}{S}$

where f_s is sampling rate

$f_s = 1/T_s$.

→ Adaptive Delta Modulation (ADM) :-



e(K) is error; discrepancy b/w m(t) & $\hat{m}(t)$

$\Delta(t)$ is V_H if $m(t) > \hat{m}(t)$

V_L if $m(t) < \hat{m}(t)$

$$\boxed{\begin{aligned} S(K) &= |S(K-1)|\, e(K) + S_o e(K-1) \\ &\simeq S_o \pm S(K-1) \end{aligned}}$$

where S_o → step size provided by accumulator

$S(K)$ → step size generated by processor at K^{th} clock edge

$S(K-1)$ → step size generated by processor at $(K-1)^{th}$ clock edge

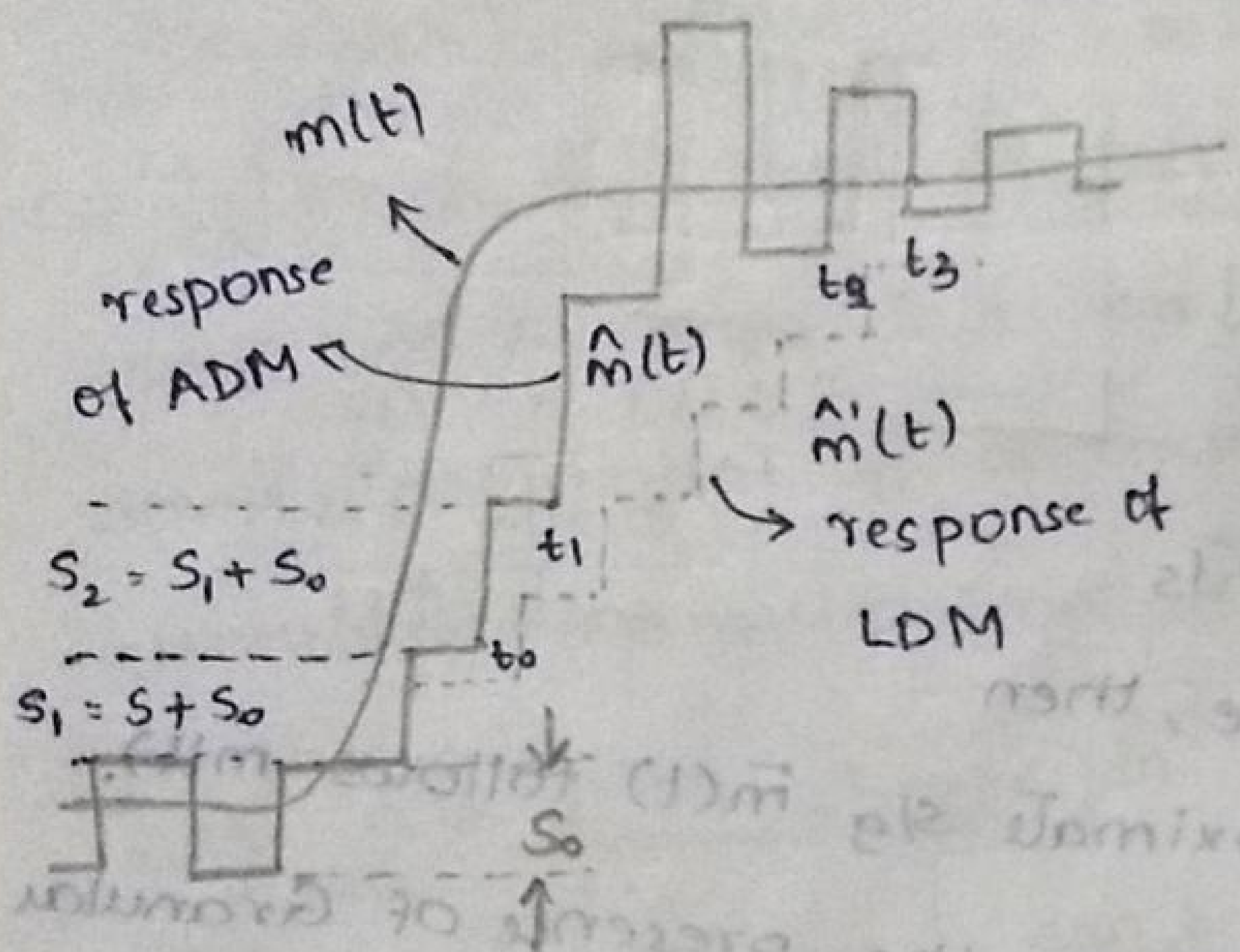


fig :- waveforms comparing the response of ADM & LDM

$e(K) = +1$ if $m(t) > \hat{m}(t)$

$\quad\quad\; -1$ if $m(t) < \hat{m}(t)$

From ① & ② : $\boxed{S(K) = S_o \pm S(K-1)}$

case ① :- clock edge At time

$K \rightarrow t = t_1 \rightarrow e(K) = 1$

$(K-1) \rightarrow t = t_0 \rightarrow e(K-1) = 1$

} ⇒ same directions

$\therefore S(K) = |S(K-1)|\, e(K) + S_o\, e(K-1)$

$= \boxed{S(K-1)}\,(1) + S_o(1) = \boxed{S_o + S(K-1)} \longrightarrow$ ①

case ② :- $K \rightarrow t = t_3 \rightarrow e(K) = -1$

$(K-1) \rightarrow t = t_2 \rightarrow e(K-1) = 1$

} opposite directions.

$\therefore S(K) = S(K-1)\,(-1) + S_o(1) = \boxed{S_o - S(K-1)} \rightarrow$ ②

$\Delta(t)$ is V_H if $m(t) > \hat{m}(t)$

V_L if $m(t) < \hat{m}(t)$

$e(k)$ is error i.e., discrepancy b/w $m(t)$ & $\hat{m}(t)$

To express the algorithm by which the step size is determined, it is convenient to arrange that

$e(k) = +1$ if $m(t) > \hat{m}(t)$ immediately before k^{th} edge

$= -1$ if $m(t) < \hat{m}(t)$ immediately before k^{th} edge

At sampling time t, step size $S(k)$ is

$$S(k) = |S(k-1)|\,e(k) + S_0\, e(k-1)$$

$$\simeq S_0 \pm S(k-1)$$

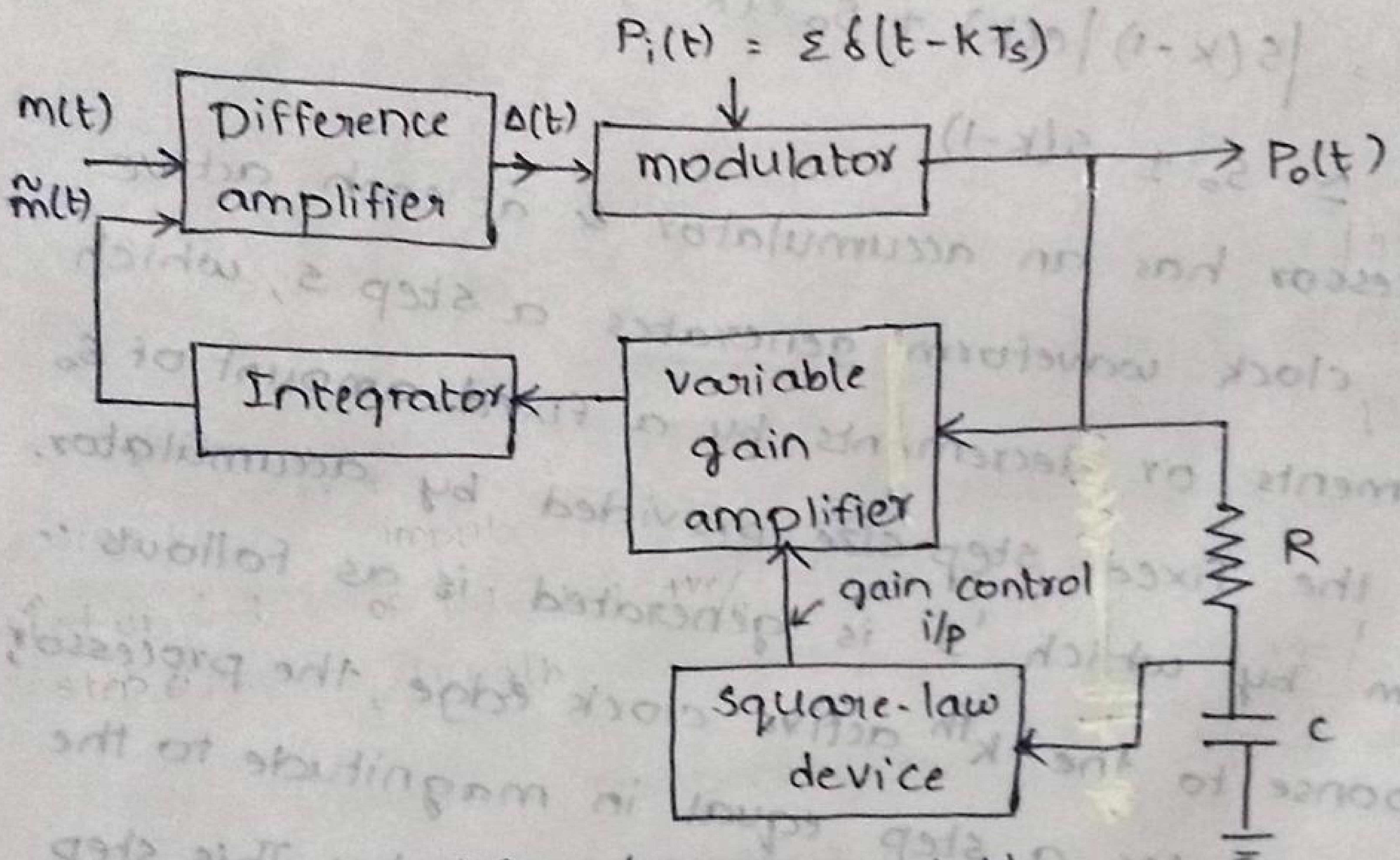
The processor has an accumulator & at each active edge of the clock waveform generates a step S, which either increments or decrements by a fixed amount of S_0 where S_0 is the fixed step size provided by accumulator. The algorithm by which 's' is generated is as follows :-

In response to the k^{th} active clock edge, the processor, to start with, generates a step equal in magnitude to the step generated in response to $(k-1)$th clock edge. This step is added to or subtracted from the accumulator as required to move $\hat{m}(t)$ towards $m(t)$.

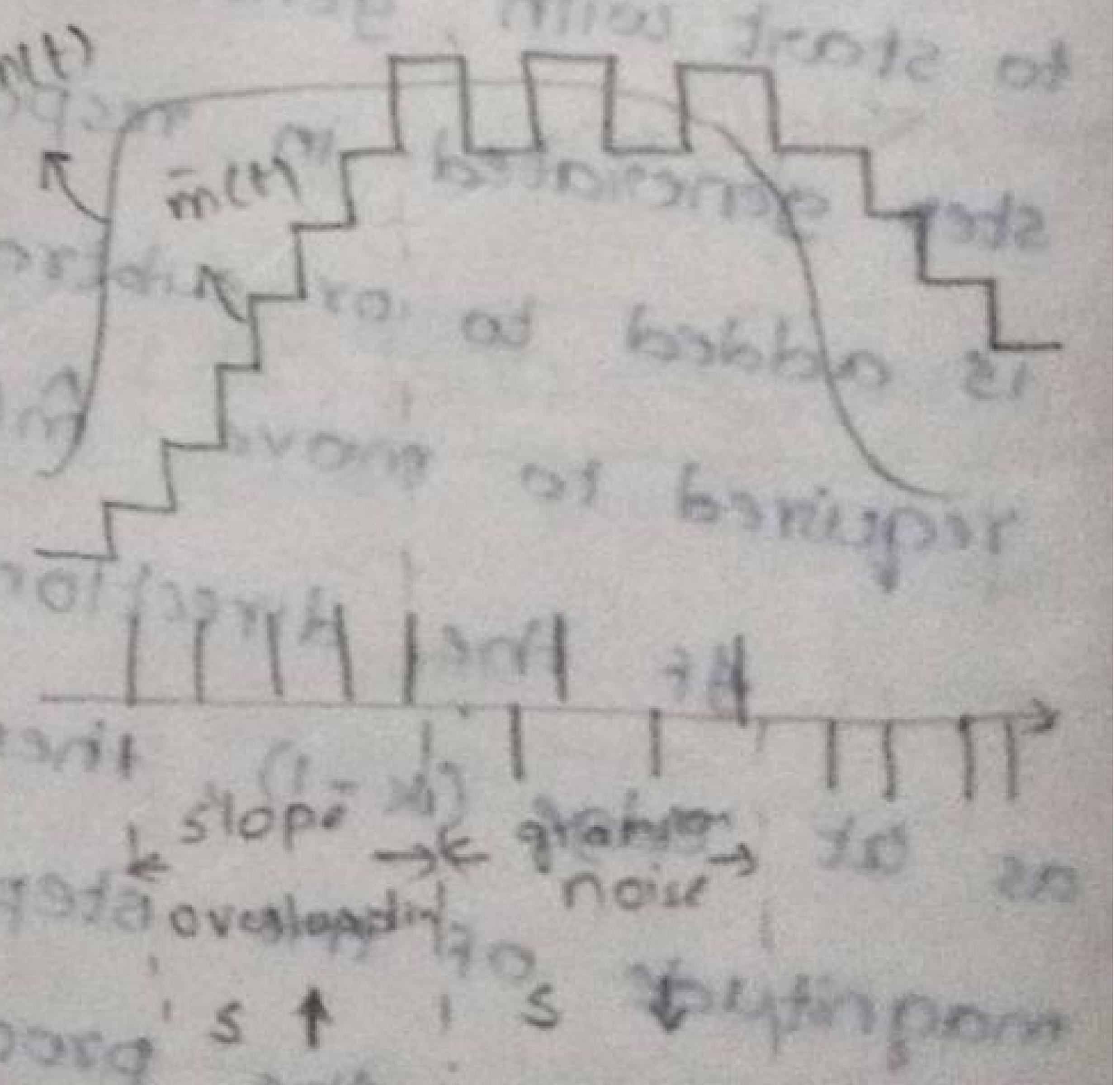
If the direction of step at clock edge k is same as at edge $(k-1)$, then the processor increases the magnitude of the step by amount S_0. If the directions are opposite, then the processor decreases the magnitude of step size by S_0. As the algorithm is carried out, there are clock edges when the total step $S=0$. In this case, at the next clock edge, the step is S_0 in a direction to move $\hat{m}(t)$ towards $m(t)$. In this way processor increments or decrements the step size by a fixed amount 'S_o' volts in order to reduce the effect of slope overloading & Granular noise.

Generally on average, over large no. of determinations 90% of variations results increase in step size by an amount of '$2S_o$' & only 1% of total measurements results an increase of '$15S_o$'.

→ CVSDM {Continuously Variable Slope Delta Modulation} system



The amplifier has a variable gain i.e., its gain is a fn of voltage applied at its gain-control terminal.



gain-control voltage	Gain
+ve	increases
'0'	decreases

The characteristics of amplifier are such that when the gain-control voltage is zero, its gain is low & that the gain ↑es with increasing +ve gain-control voltage.

The resistor - capacitor combination serves as an integrator, the voltage across 'C' being proportional to the integral of $P_o(t)$. The voltage across C is used to control the gain of amplifier. Despite of the polarity of voltage across 'C', a +ve voltage will be applied to the gain - control terminal of the amplifier, since o/p of square law device is always +ve.

When the variation of m(t) is very high, o/p $P_o(t)$ is a train of all +ve impulses & when m(t) is suddenly falling, o/p $P_o(t)$ is a train of all -ve impulses. This causes either a +ve or -ve voltage across the capacitor, but the o/p of square law device is always +ve, so that for +ve gain control voltage the gain of variable - gain amplifier increases. Hence the o/p of amplifier is an impulse of increased strength & when it is integrated causes a step of increased step size. This reduces the effect of slope overloading.

When the s/g variations are small, o/p $P_o(t)$ is a train of alternate +ve & -ve impulse sequence & when it is accumulated causes zero volts across capacitor. Hence the gain control voltage is zero which decreases the gain of amplifier. Hence the o/p of amplifier is an impulce of reduced strength & when it is integrated, generates a step of reduced step size. This causes a reduction in granular noise.