Unit-2 Problems

1. For the clipper circuit shown in Figure2.1, the input v_i = 100 sinωt. Plot the transfer characteristic and the input and output waveforms. Assume ideal diodes.

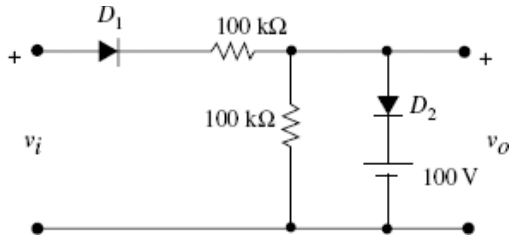

Figure 2.1 The given clipping circuit for problem 1

2. For the clipper circuit shown in Figure2.2, the input v_i = 50 sin ωt. Plot the transfer characteristic and the input and output waveforms. Assume ideal diodes.

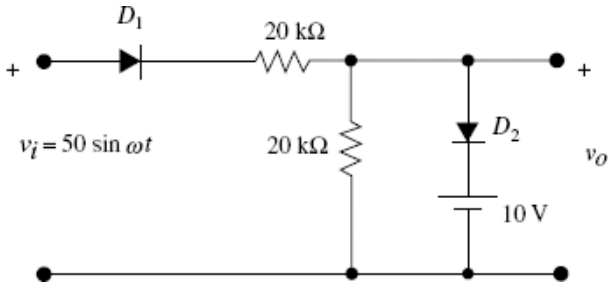

Figure 2.2 Clipping circuit

3. The input to the two-level clipper shown in Figure2.3, varies linearly from 0 to 100 V. Plot the transfer characteristic and obtain the output voltage. Assume ideal diodes.

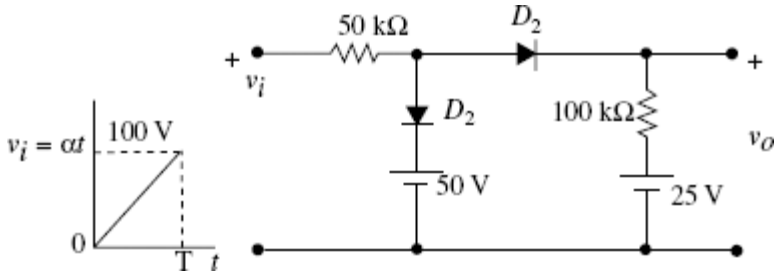

Figure 2.3 The given Clipping circuit for problem 3

4. For the circuit shown in Figure2.4, with v_i varying linearly up to 150 V, obtain the transfer characteristic and the output.

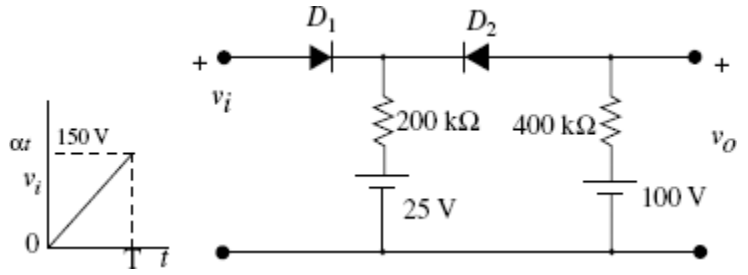

Figure 2.4 Clipping circuit with input

5. For the circuit shown in Figure2.5, v_i varies linearly up to 100 V. Obtain the transfer characteristic and the output.

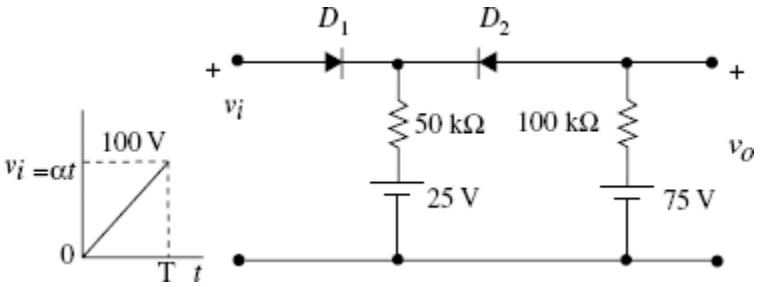

Figure 2.5 The clipping circuit for problem 5

6. For the circuit shown in Figure2.6, plot the transfer characteristic for v_i varying from 0 V to 75 V linearly.

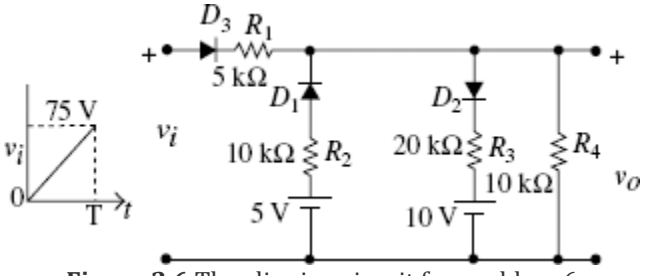

Figure 2.6 The clipping circuit for problem 6

7. For the circuit shown in Figure2.7, R_f = 200 Ω, R = 20 kΩ, V_γ = 0 V. Sketch the output waveform for the given input.

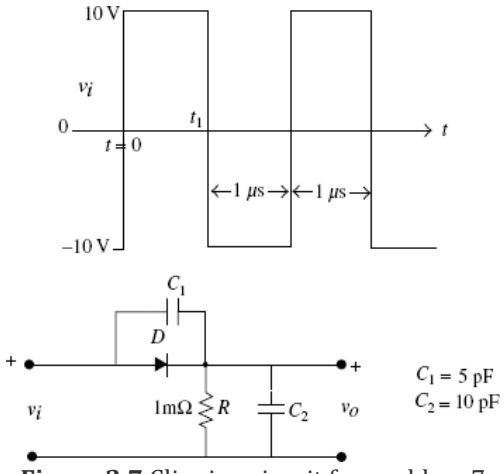

Figure 2.7 Clipping circuit for problem 7

8. For the circuit shown in Figure2.8, R_f = 100 Ω, R = 10 kΩ, V_γ = 0. Sketch the output waveform for the specified input.

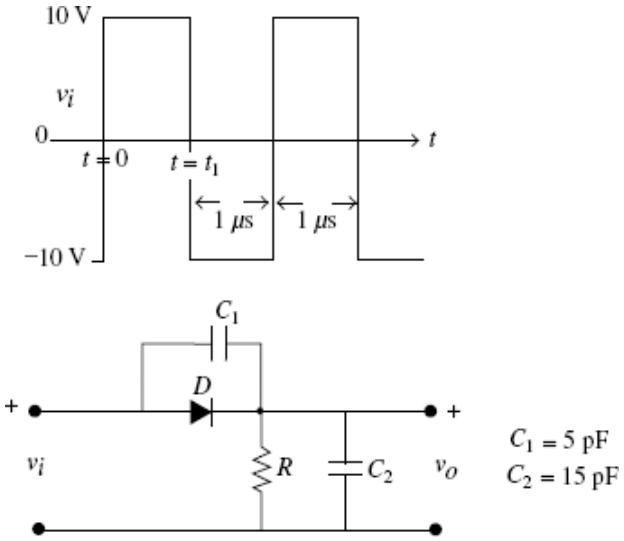

Figure 2.8 The given clipping circuit with input.

9. Design a diode clamper shown in Figure2.9 to restore the positive peaks of the input signal to a voltage level to 5 V. Assume the diode cut-in voltage is 0.5 V, f = 1 kHz, R_f = 1 kΩ, R_r = 200 kΩ and RC = 20 T.

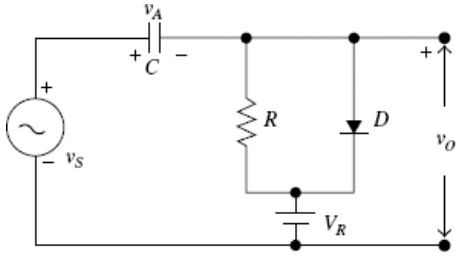

Figure 2.9 The given clamping circuit with reference voltage V_R

10. For the excitation as shown in Figure2.10(a) and the clamping circuit [see Figure2.10(b)], calculate and plot to scale, the steady-state output.

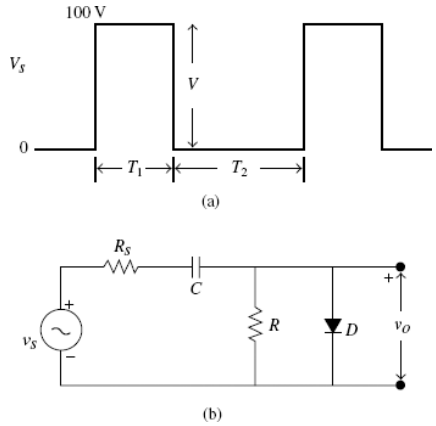

Figure2.10(a) The given Input, and (b) the clamping circuit

11. Sketch the steady-state output voltage for the clamper circuit shown in Figure2.11 and locate the output dc level and the zero level. The diode used has $\boldsymbol{R_f}$ = 100 Ω, $\boldsymbol{R_r}$ = 500 kΩ, $\boldsymbol{V_\gamma}$ = 0.$\boldsymbol{C}$ is arbitrarily large and $\boldsymbol{R}$ = 20 kΩ. The input is a ±20V square wave with 50 per cent duty cycle.

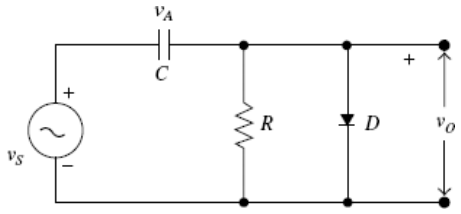

Figure 2.11 The given clamping circuit

12. For the circuit shown in Figure2.12(a), $\boldsymbol{R_s}$ = $\boldsymbol{R_f}$ = 50 Ω, $\boldsymbol{R}$ = 10 kΩ, $\boldsymbol{R_r}$ = ∞, $\boldsymbol{C}$ = 2.0 $\boldsymbol{\mu}$F, the input varies as shown in Figure2.12(b). Plot the output waveform.

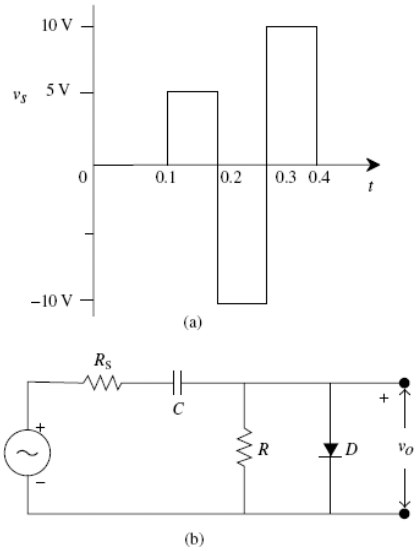

Figure2.12 (a) The given input; and (b) the given clamping circuit

13. The input as shown in Figure2.13(a) is applied to the clamping circuit shown in Figure2.13(b) with $R_s = R_f = 100\ \Omega$, $R = 10\ k\Omega$, $R_r = \infty$, $C = 1.0\ \mu F$; $V_\gamma = 0$. Draw the output waveform and label all the voltages.

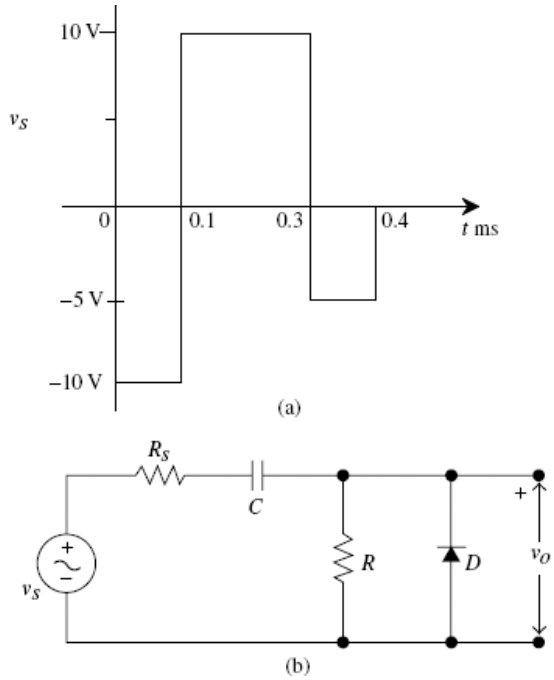

Figure2.13(a) The given input; and (b) the given clamping circuit

14. A clamping circuit and input applied to it are shown in Figure2.14. Assume that C is quite large. Find at which voltage level the positive peak is clamped in the output if $T_1 = 1$ ms, $T_2 = 1\mu s$, $R_f = 100\ \Omega$ and $R = 100\ k\Omega$.

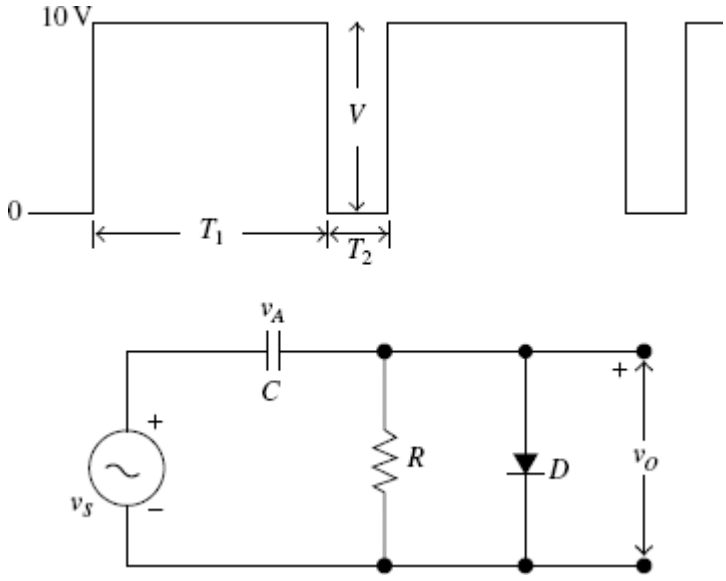

Figure 2.14 The given input and clamping circuit (Hint: Use the clamping Theorem.)

15. Calculate and draw the steady-state output waveform of the circuit in Figure2.15. Assume R_f = 50 Ω, R_r = 500 kΩ and $T_1 = T_2$ = 1 ms.

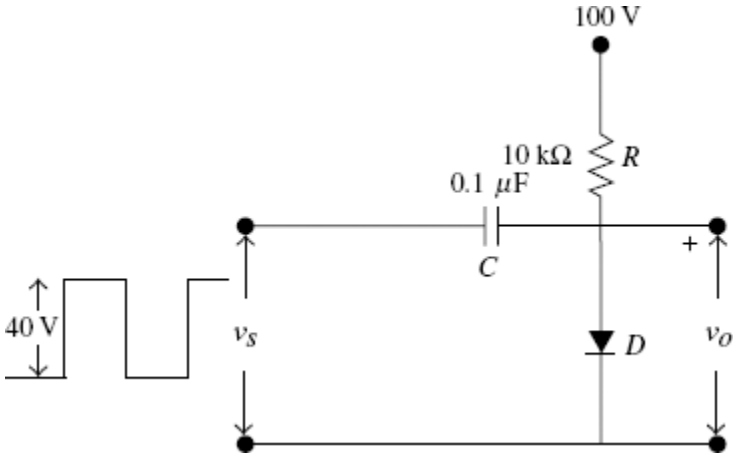

Figure2.15 The given clamping circuit with large

16. Design a biased clamping circuit to derive the output voltage as shown in Figure2.16 (b), given the input as shown in Figure2.16 (a) f = 1000 Hz, R_f = 100 Ω, R_r = 1MΩ and RC/T = 10. Assume that D is ideal.

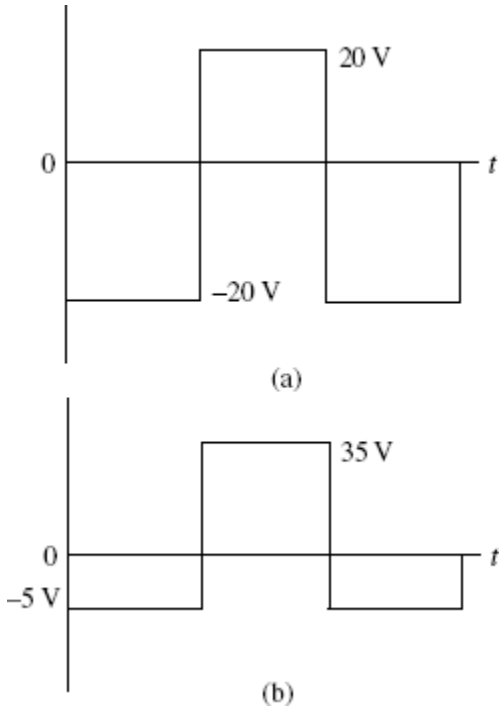

Figure2.16(a) The given input to the clamping circuit; and (b) the required output