UNIT – V: Part-B

Digital Logic Families: Introduction, RTL, DTL, TTL, ECL, NMOS Logic, PMOS Logic, CMOS Logic-Analysis

Introduction:

In digital applications, data is in the form of binary bits—0s and 1s. A logic gate is a digital circuit that gives a specific discrete output (0 or 1) depending on the input conditions. These logic gates can be wired using discrete components such as resistors, diodes, transistors, FETs, and their combinations. The simplest logic gate, say a two-input AND / OR gate (diode–resistance logic gate), may be constructed using two diodes, a resistance and a dc source. The important logic families are diode–transistor logic (DTL), transistor–transistor logic (TTL), *p*-channel and *n*-channel MOSFET logic (PMOS and NMOS) and complementary MOSFET logic (CMOS). The TTL family is further subdivided into open-collector TTL, emitter-coupled logic (ECL) or integrated injection logic (I^2L). TTL and CMOS are the two most important logic families. TTL gates are preferred where there is a need for faster switching speed and CMOS gates are used where the requirement is lower power dissipation per gate. The suitability of a logic gate, for a specific application, is evaluated in terms of the number of requirements. This chapter presents the relative performance of these gates. Also, sometimes, it becomes necessary to connect the output of one type of gate (say, a TTL gate which operates with a 5 V supply) to the input of another gate (say, a CMOS gate that operates with a 30 V supply). In such cases, the output requirements of the driving gate should be compatible with the input requirements of the driven gate. Hence, interfacing methods are also discussed. Normally, designing and constructing logic gates using discrete components is meaningful only for small circuits. As the complexity increases, these circuits are best fabricated on a chip called the digital integrated circuit. Depending on the level of integration, these are classified as under:

1. Small-scale integration (SSI): 1 to 20 gates or transistors per package
2. Medium-scale integration (MSI): 20 to 200 gates or transistors per package
3. Large-scale integration (LSI): 200 to 200,000 gates or transistors per package
4. Very large-scale integration (VLSI): More than 1 million gates or transistors
5. Ultra large-scale integration (ULSI): 1 billion gates or transistors

- Propagation delay is the average transition delay time for a pulse to propagate from input to output of a switching circuit.
- Fan-in is the number of inputs to the gate which it can handle.
- Fan-out is the number of loads the output of a gate can drive without effecting its operation.
- Power dissipation is the supply voltage required by the gate to operate with 50% duty cycle at a given frequency
- RTL, DTL, DTL are the logic families which are now obsolete.
- TTL is the most widely used logic family.
- TTL gates may be:

a) Totem pole
b) Open collector
c) Tri-state .

- TTL is used in SSI and MSI Integrated circuits and is the fastest of all standard logic families.
- Totem pole TTL has the advantage of high speed and low power dissipation but its disadvantage is that it cannot be wired ANDed because of current spikes generation.
- Tri-state has three states : .

a) High
b) Low
c) High Impedance

- ECL is the fastest of all logic families because its propagation delay is very small i.e. of about 2 nsec.
- ECL can be wired ORed.
- MOS logic is the simplest to fabricate.
- MOS transistor can be connected as a resistor.
- MOSFET circuitries are normally constructed from NMOS devices because they are 3 times faster than PMOS devices.
- CMOS uses both P-MOS and N-MOS.
- CMOS needs less power as compared to ECL as they need maximum power.
- Both NMOS and PMOS are more economical than CMOS because of their greater packing densities.
- Speed of CMOS gates increases with increase in VDD.
- CMOS has large fan-out because of its low output resistance.

Logic Gates:

A logic gate is a circuit that gives either '0' (LOW) level or '1' (HIGH) level at the output, depending on the input conditions. The basic logic gates can be wired using discrete components such as resistors, diodes, transistors and FETs. The wiring of a complex gate circuit is unthinkable using discrete components. When the complexity of the gate circuit increases, it is preferable to wire the logic gate in an integrated circuit form. In this section, we basically describe the different types of logic gates using discrete components only, in order to understand the principle of operation of logic circuits of different logic families.

1. Simple Diode Gates:

AND and OR are the two basic gates from which NAND and NOR gates can be derived. Here, we describe two types of diode gates—diode AND gates and diode OR gates.

Diode AND Gates:

An AND gate is a digital circuit which gives a high output only when all the inputs are simultaneously high (1), otherwise the output is low (0). Consider a simple two-input AND gate using diodes (See Fig. 5.1).

Assuming *D*1 and *D*2 to be ideal diodes, the following cases are possible:

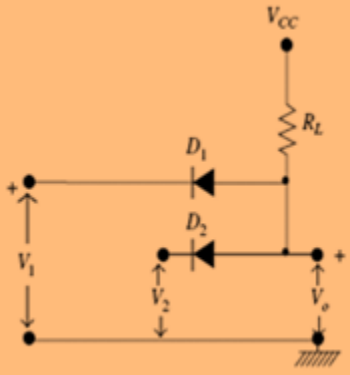


FIGURE 5.1 A two-input AND gate

Y=AB

V1	V2	Vo
0	0	0
0	1	0
1	0	0
1	1	1

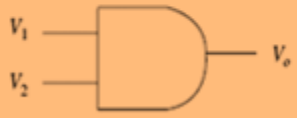


FIGURE 5.2(a) The schematic diagram for the two-input AND gate

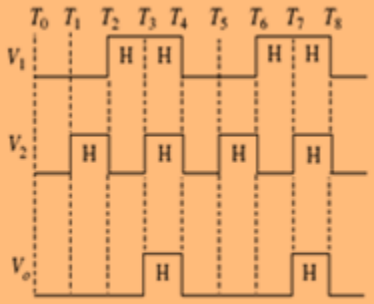


FIGURE 5.2(b) The timing diagram for two-input AND gate

1. Both the inputs are zero, the diodes are ON and $Vo = 0$.
2. $V1 = 0$, $V2 = 1$, $D1$ is ON, $D2$ is OFF, $Vo = 0$.
3. $V1 = 1$, $V2 = 0$, $D1$ is OFF, $D2$ is ON, $Vo = 0$.
4. $V1 = 1$, $V2 = 1$, $D1$ and $D2$ are OFF, $Vo = 1$.

Y=AB

V1	V2	Vo
0	0	0
0	1	0
1	0	0
1	1	1

TABLE5.1 The truth table for the AND gate

The truth table for the gate is given in Table 5.1. The schematic representation of the AND gate is shown in Fig 5.2(a).

The timing diagram for the two-input AND gate is shown in Fig 5.2(b). As mentioned in the preceding section, in an AND gate, the output is 1 only when all the inputs are 1 and, 0 if any one of the inputs is 0. Hence, in Fig. 5.2(b), at the instant $T0$, when both the inputs $V1$ and $V2$ are 0, the output $Vo = 0$. At $T1$, $V1 = 0$ and $V2 = 1$. Since one of the inputs is zero, the output $Vo = 0$. At the instant $T3$, $V1 = 1$ and $V2 = 1$. Since both the inputs are 1, the output $Vo = 1$ and so on. In general, there can be a large number of inputs to a gate.

NOT Gate: Y= $\overline{A}$: A NOT gate, also called an inverter in digital circuits, is schematically represented as in Figure 5.2(c). Figure 5.2(d) shows the timing diagram for a NOT gate.

A	Y=$\overline{A}$
0	1
1	0

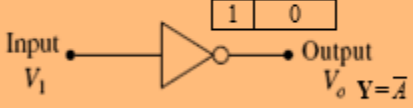


FIGURE 5.2(c) A NOT gate

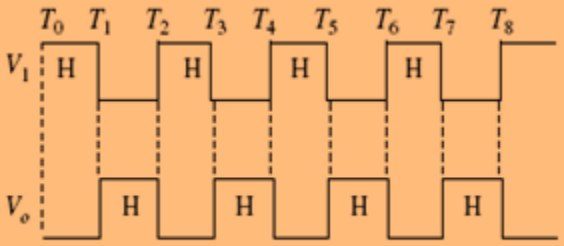


FIGURE 5.2(d) The timing diagram for a NOT gate

In a NOT gate, the output is the complement of the input. This means, that if the input is 1, the output is 0; and if the input is 0, the output is 1. At *To*, the input *V*1 = 1; therefore, the output *Vo* = 0. At *T*1, the input *V*1 = 0 and output *Vo* = 1 and so on. **Y=** $\overline{A}$ **.**

A	**Y=** $\overline{A}$
0	1
1	0

An AND gate cascaded with a NOT gate is called a NAND gate. Figures 5.3(a) and (b) show the schematic representation and the timing diagram of a NAND gate, respectively.

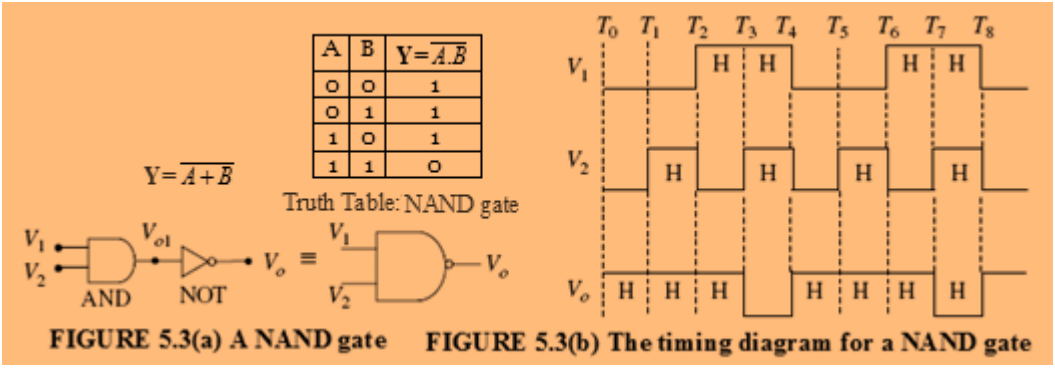


FIGURE 5.3(a) A NAND gate **FIGURE 5.3(b) The timing diagram for a NAND gate**

In a NAND gate, the output is 0 only when all the inputs are 1. If any one of the inputs is 0, **the output is 1. As shown in Fig. 5.3(b), at the instant *T*0, both the inputs *V*1 and *V*2 are 0** and therefore, the output *Vo* is 1. At *T*1, *V*1 = 0 and *V*2 = 1. Since one of the inputs is 0, the output *Vo* is 1. At *T*3 both the inputs *V*1 and *V*2 are equal to 1 and therefore the output *Vo* = 0. **Y=** $\overline{A.B}$ **.**

A	B	**Y=** $\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

Diode OR Gates: An OR gate is a digital circuit which gives a high output when either one or all the inputs are high (1). In other words, the output is low (0) only when both the inputs are low. A two-input diode OR gate is shown in Figure 5.4. Here too, we assume the diodes to be ideal. The following cases are possible:

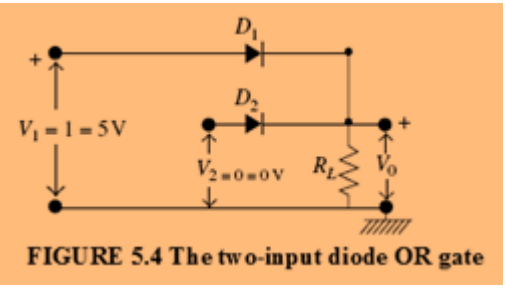


FIGURE 5.4 The two-input diode OR gate

1. *V*1 = *V*2 = 0, *D*1 and *D*2 are OFF, *Vo* = 0
2. *V*1 = 0, *V*2 = 1, *D*1 is OFF, *D*2 is ON, *Vo* = 1
3. *V*1 = 1, *V*2 = 0, *D*1 is ON, *D*2 is OFF, *Vo* = 1
4. *V*1 = 1, *V*2 = 1, *D*1 and *D*2 are ON and *Vo* = 1

The truth table for an OR gate is shown in Table 5.2. An OR gate is schematically represented as in Figure 5.5(a).

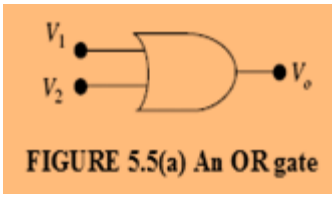


FIGURE 5.5(a) An OR gate

Y=A+B

V1	V2	Vo
0	0	0
0	1	1
1	0	1
1	1	1

TABLE 5.2 The truth table for an OR gate

The timing diagram for a two-input OR gate is shown in Figure 5.5(b). In an OR gate, when any one of the inputs is 1, the output is 1. It is 0 only if all the inputs are 0. Hence, in Figure 5.5(b), at the instant *T*0, both the inputs *V*1 and *V*2 are 0; therefore, the output *Vo* is 0. At *T*1, *V*1 is 0 whereas *V*2 = 1. Since one of the inputs is 1, the output *Vo* = 1. At the instant *T*3,*V*1 is 1 and *V*2 is 1. Since both the inputs are 1, the output

Vo = 1.

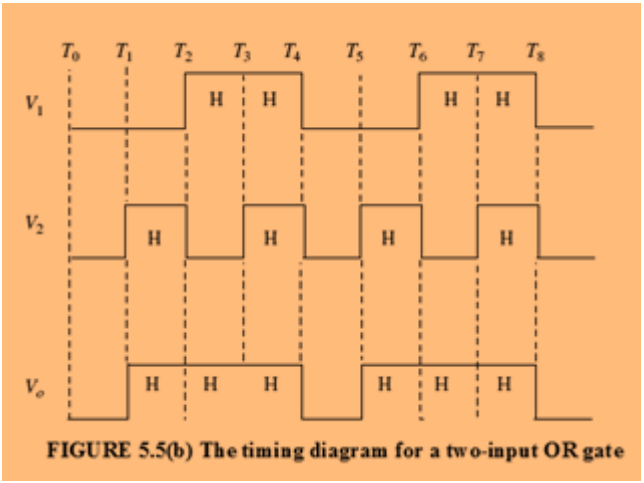
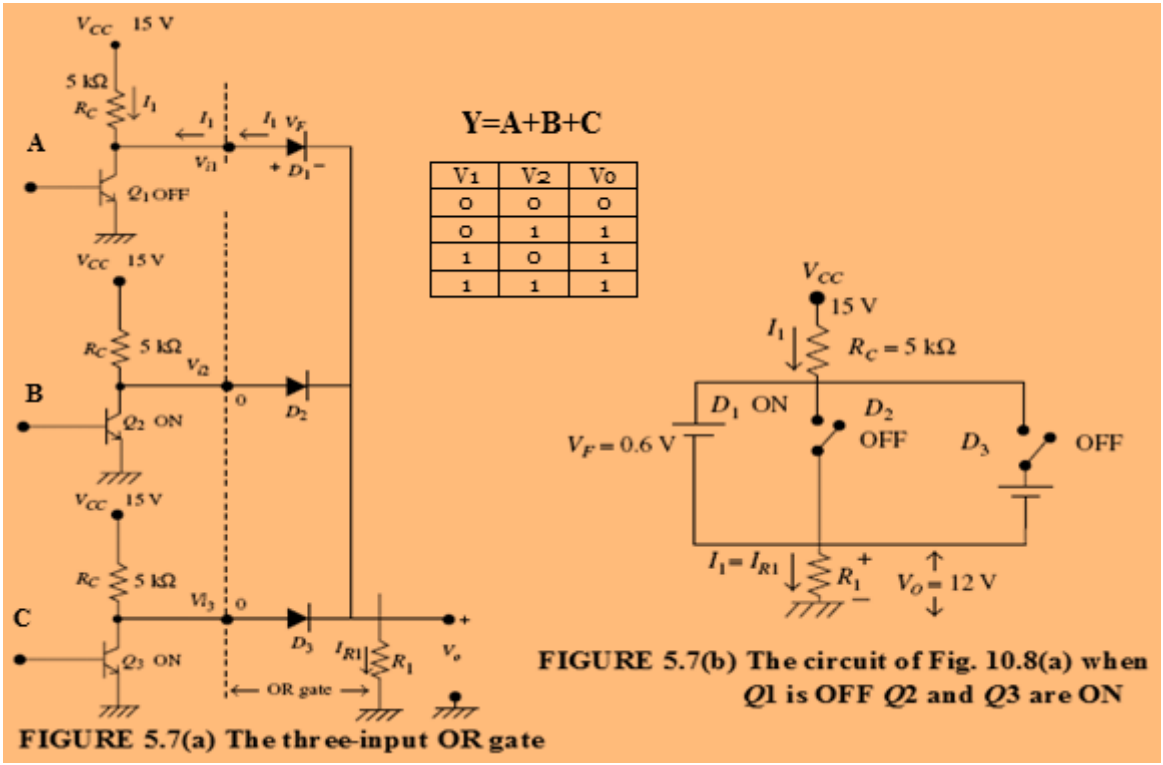


FIGURE 5.5(b) The timing diagram for a two-input OR gate



V1	V2	Vo
0	0	0
0	1	1
1	0	1
1	1	1

FIGURE 5.7(a) The three-input OR gate

FIGURE 5.7(b) The circuit of Fig. 10.8(a) when *Q*1 is OFF *Q*2 and *Q*3 are ON

Let the inputs be 1, 0 and 0 for *D*1, *D*2 and *D*3, respectively. This means *Q*1 is OFF and *Q*2 and *Q*3 are ON. Then *D*1 is ON and *D*2 and *D*3 are OFF, as shown in Figure5.7(b).

*VCC = I*1*RC + VF + Vo I*1*RC = VCC – VF – Vo*

V0 for 1 level required to be 12V. Therefore,

$$I_1 = \frac{15 - 0.6 - 12}{R_C} = \frac{2.4\,\text{V}}{5\,\text{k}\Omega} \qquad I_1 = I_{R1} = 0.48\,\text{mA}$$

Therefore

$$V_o = I_{R1} R_1 \qquad R_1 = \frac{12}{0.48\,\text{mA}} = 25\,\text{k}\Omega$$

NOR Gate: An OR gate cascaded with a NOT gate is called a NOR gate, as represented in Figure 5.7(c). Its timing diagram is shown in Figure 5.7(d). **Y=** $\overline{A+B}$.

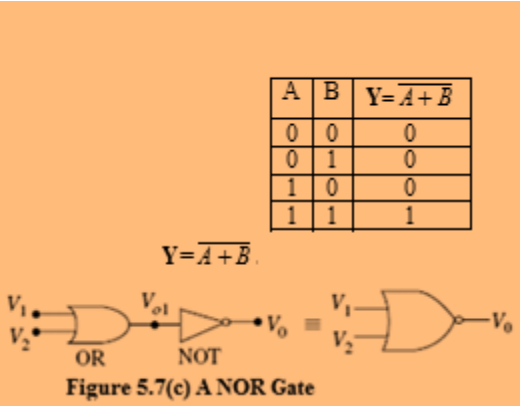


Figure 5.7(c) A NOR Gate

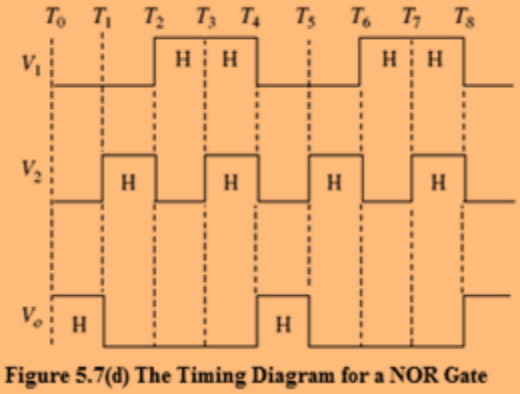


Figure 5.7(d) The Timing Diagram for a NOR Gate

The output of a NOR gate is 1 when all the inputs are 0. When any one of the inputs is 1, the output is 0. Therefore, in Figure 5.7(d), at the instant *T*0, when both the inputs *V*1 and *V*2 are 0, the output of the NOR gate is *Vo* = 1. At *T*1, *V*1 = 0 and *V*2 = 1; since one of the inputs is 1, the output *Vo* is 0. At *T*3, both the inputs *V*1 and *V*2 are equal to 1; therefore, the output *Vo* is 0. **Y=** $\overline{A+B}$.

A	B	**Y=** $\overline{A+B}$
0	0	0
0	1	0
1	0	0
1	1	1

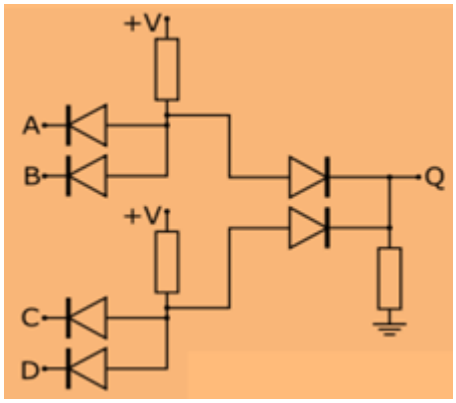
Input Logical Ones: When all the input voltages are high, they "neutralize" the biasing supply voltage +*V*. The voltage drops across the diodes are zero and these diode switches are open. The output voltage is high (output logical *1*) since no current flows through the resistor and there is no voltage drop across it. The output resistance is R1. Hence, the behavior of the diode switches is reversed - whereas in diode OR logic gates diodes act as *normally open switches*, in diode AND logic gates diodes act as *normally closed switches*.

Input Logical Zero: If the voltage of some input voltage source is low (input logical *0*), the power supply passes current through the resistor, diode and the input source. The diode is forward biased (the diode switch is closed) and the output voltage drop across the diode is low (output logical *0*). The output resistance is low and is determined by the input source. The rest of diodes connected to high input voltages (input logical *1s*) are backward biased and their input sources are disconnected from the output Node 1.

If two diode AND logic gates are cascaded, they behave as *current-sinking* logic gates: if the first gate produces high output voltage, the second gate does not consume current from the first one; if the first gate produces low output voltage, the second gate injects current into the output of the first one. A diode AND gate uses its own power supply to drive the load through the pull-up resistor.

Properties

Non-Restoring Logic:



In cascaded AND-OR diode gates, the high voltage level is decreased more than two times. Digital logic implemented by active elements is characterized by signal restoration. *True* and *false* or *1* and *0* are represented by two specific voltage levels. If the inputs to a digital logic gate are close to their respective levels, the output will be closer or exactly equal to its desired level. Active logic gates may be integrated in large numbers because each gate tends to remove noise at its input. Diode logic gates are implemented by passive elements; so, they have two restoration problems.

Forward Voltage Drop: The first restoration problem of diode logic is that there is a voltage drop VF about 0.6 V across the forward-biased diode. This voltage is added to or subtracted from the input of every gate so that it accumulates when identical diode gates are cascaded. In an OR gate, VF decreases the high voltage level (the logical *1*) while in an AND gate, it increases the low voltage level (the logical *0*). The feasible number of logic stages thus depends on the difference between the high and low voltages.

Source Resistance: Another problem of diode logic is the internal resistance of the input voltage sources. Together with the gate resistor, it constitutes a voltage divider that worsens the voltage levels. In an OR gate, the source resistance decreases the high voltage level (the logical *1*) while in an AND gate, it increases the low voltage level (the logical *0*). In the cascaded AND-OR diode gates in the picture on the right, the AND high output voltages are decreased because of the internal voltage drops across the AND pull-up resistances.

Non-Inverting Logic:

Diode logic is non-inverting in both the OR and AND configurations: a diode OR gate is *true non-inverting* ($Y = X$ in the case of one-input OR gate) while a diode AND gate is non-inverting since it is *double inverting* (Y = NOT (NOT (X)) = X in the case of one-input AND gate - see the considerations above). Diode AND gate would be inverting if the voltage drop across the resistor is taken as an output but the load would be not grounded in this case.

Applications:

Diode logic gates are used to build diode–transistor logic (DTL) gates as integrated circuits.

The outputs of conventional ICs (with complementary output stages) must never be directly connected together since they act as voltage sources. However, diodes can be used to

combine two or more digital (high/low) outputs from an IC such as a counter. Thiswired logic connection can be a useful way of producing simple logic functions without using additional logic gates.

2. Resistor–Transistor Logic Gates:

An RTL gate uses the resistances and transistors for its operation. Figure 5.8 shows a resistor–transistor logic (RTL) NOR gate. If both the inputs *V*1 and *V*2 are 0, *Q*1 and *Q*2 are OFF and *Vo* = *VCC* (1 level). If any or both the inputs are 1, *Vo* =*VCE*(sat) (0 level). Hence, this is a NOR gate. **Y=** $\overline{A+B}$**.**

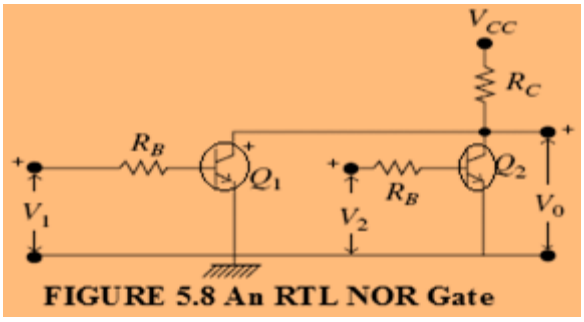


FIGURE 5.8 An RTL NOR Gate

V1	V2	Vo
0	0	1
0	1	0
1	0	0
1	1	0

TABLE 5.3 The truth table for a NOR gate

Schematic of RTL NOR gate and its operation.

RTL was the first to introduce. RTL NOR gate is as shown in Figure5.8

Working:

Case I: When A = B = 0.

Both T1 and T2 transistors are in cut off state because the voltage is insufficient to drive the transistors i.e. VBE < 0.6 V: Thus, output Y will be high, approximately equal to supply voltage Vcc. As no current flows through Rc and drop across Rc is also zero.

Thus, Y = 1, when A = B = 0.

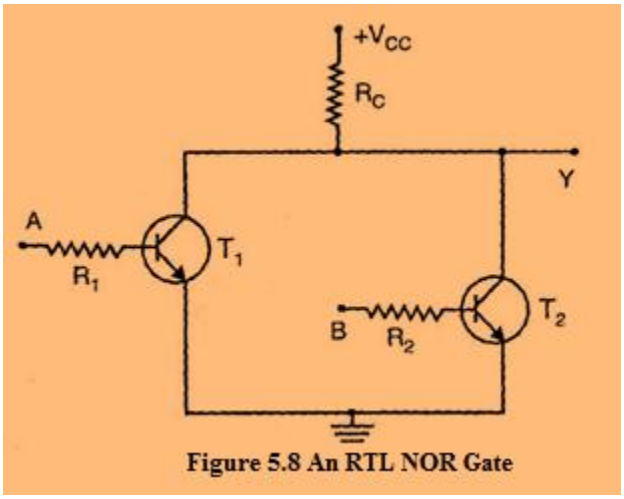


Figure 5.8 An RTL NOR Gate

Case II: When A = 0 and B = 1 or A = 1 and B = 0.

The transistor whose input is high goes into saturation where as other will goes to off cut state. This positive input to transistor increases the voltage drop across the collector resistor and decreasing the positive output voltage.

Thus, Y = 0, when A= 0 and B = 1 or A = 1 and B = 0.

Case III: When A = B = 1**.** Both the transistors T1 and T2 go into saturation and output voltage is equal to saturation voltage. Thus, Y = 0, when A = B = 1. Which is the output of a NOR gate. **Y=** $\overline{A+B}$**.**

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Table:5.3 The truth table for a NOR gate. **Y=** $\overline{A+B}$.

DCTL NAND Gate with the Help of Suitable Circuit Diagram:

DCTL NAND gate circuit diagram is as shown in Figure 5.8(b): **Y=** $\overline{A\times B}$

Working

Case I: When A = B = 0. Both transistors T1 and T2 goes to cut off state. As the voltage is not sufficient to drive the transistor into saturation. Thus, the output voltage equal to Vcc. When A = B = 0, output Y = 1

Case II: When A = 0 and B = 1 or A = 1 and, B = 0. The corresponding transistor goes to cut

off state and the output voltage equals to Vcc. Thus, When A = 0 and B = 1 or A = 1 and B = 0, Output Y = 1.

Case III: When A = B = 1. Both transistors T1 and T2 goes into saturation state and output voltage is insufficient to consider as '1' Thus when A B = 1, output Y = 0.

Y= $\overline{A\times B}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table:

Which is the output of NAND gate

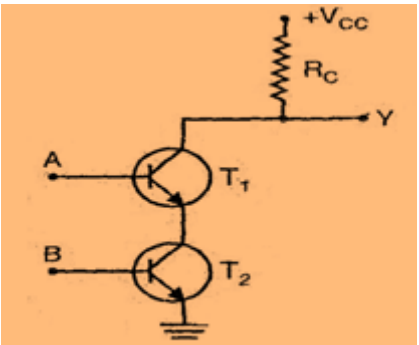


Figure 5.8(b) DCTL NAND Gate

3. Diode–Transistor Logic Gates:

In the diode–transistor logic family (DTL), diodes and transistors are used as the basic building blocks. In this family, we consider the two basic gates—NAND and NOR.

DTL NAND Gates: A diode AND gate followed by a transistor inverter is a DTL NAND gate, as shown in Figure 5.9. Here, we assume that the input at 1 is grounded. Diode *D*1 conducts. Then the voltage at A, *VA* = *VF*, the diode forward voltage. With this voltage (approximately equal to 0.7 V), diodes *D*3 and *D*4 will not conduct as they require a minimum voltage of 1.4 V to conduct. Hence, *Q* is OFF. Thus, if any one of the inputs to the NAND gate is zero, *Q* is OFF and *Vo* = *VCC* (1 level).

If, on the other hand, both the inputs are 1, then diodes *D*1 and *D*2 are reverse-biased and behave as open circuits. Diodes*D*3 and *D*4 then conduct and the voltage at the base of *Q* can drive it into saturation. Therefore, the output *Vo* = *VCE*(sat) (0 level). This gate produces a 0 output level when all the inputs are 1 and the 1 level at the output if any of the inputs is 0 (NAND gate). *D*3 and *D*4 are provided to derive noise immunity. In the NAND gate shown in Figure 5.9, when *D*3 is replaced by a Zener diode (anode and cathode reversed) with a break-down voltage of 3.8 V, this gate gives an even better noise immunity. However, this requires high supply voltages. Such a gate is called a high-threshold logic (HTL) NAND gate. HTL is also sometimes referred to as HNIL (high noise immunity logic).

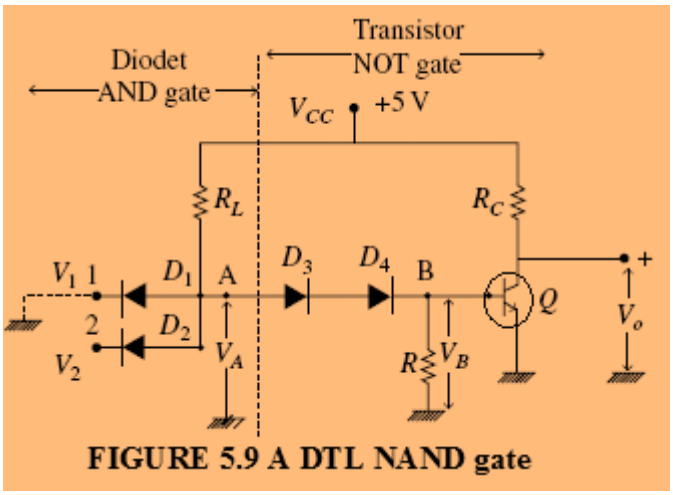


FIGURE 5.9 A DTL NAND gate

Y= $\overline{A \times B}$

V1	V2	Vo
0	0	1
0	1	1
1	0	1
1	1	0

TABLE 5.4 The truth table for a NAND gate

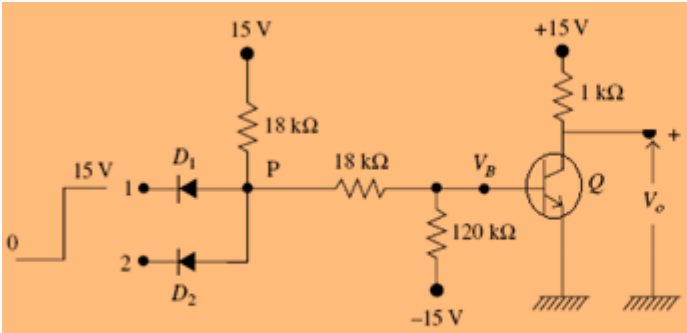


FIGURE 5.10(a) A DTL NAND gate

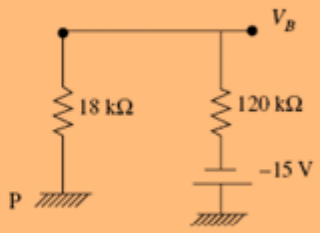


FIGURE 5.10(b) The resultant circuit of Fig. 5.10(a) when the input 1 is 0 and the other is 1

To verify that the circuit shown in Figure 5.10(a) is a NAND gate, let us assume that input1 is 0 V and input 2 is at level 1, i.e., 15 V. Then *D*1 conducts as the voltage at the anode of *D*2 is *VF* (≈ 0 V) and that at the cathode is 15 V, *D*2 is OFF and is open circuited. The voltage at P is 0 V, as shown in Figure 5.10(b).

$$V_B = \frac{-15 \times 18}{18 + 120} = -1.96 \text{ V}$$

As *VB* reverse-biases the emitter diode, *Q* is OFF and *Vo* = 15 V (1 level). If all the inputs are 15 V (1 level), both the diodes are OFF.

$$V_B = \frac{15 \times 120}{120 + 36} + (-15) \times \frac{36}{120 + 36} = 11.54 - 3.46 = 8.08 \text{ V}$$

Hence, Q is in saturation. Consequently, Vo = 0 V (0 level). The truth table for this is shown in Table 10.4. Hence, the circuit is a NAND gate.

(ii) Calculating the minimum value of hFE to keep Q in saturation

Consider the equivalent circuit of Figure 5.10(a). When Q is in saturation, VCE(sat) = 0, VBE(sat) = 0 when compared to the supply voltages of 15 V, as shown in Figure 5. 10(d).

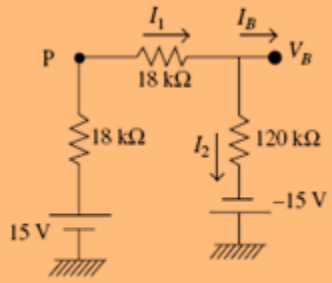


FIGURE 5.10(c) The resultant circuit of Fig. 5.10(a) when both the inputs are 1

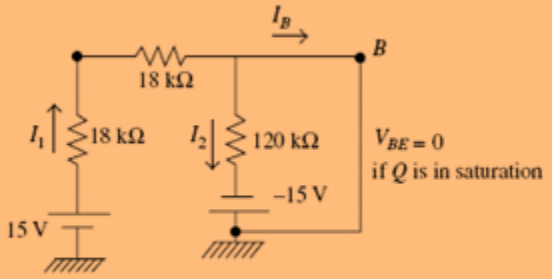


FIGURE 5.10(d) The resultant circuit of Fig. 5.10(a) when Q is in saturation

$I1 = I2 + IB$ $IB = I1 - I2$

$$I_B = \frac{15\text{ V}}{36\,k\Omega} - \frac{15\text{ V}}{120\,k\Omega} = 0.42 - 0.125 = 0.295\,\text{mA}$$

$$I_C = \frac{15\text{V}}{1\text{k}\Omega} = 15\,\text{mA}$$

And

$$h_{FE}(\text{min}) = \frac{I_C}{I_B} = \frac{15}{0.295} = 50$$

In a diode AND gate, the output voltage is high if all the input voltages are high. The output voltage is low if at least one of the input voltage is low.

DTL NOR Gates: A DTL NOR gate comprises a diode OR gate followed by a transistor inverter, as shown in Figure 5.11. When both the inputs $V1$ and $V2$ are 0, $Q1$ is OFF and Vo = VCC(1 level). If any input, say $V1$ is 1, $D1$ is ON and the voltage at the base of $Q1$ is 5 V. Consequently, $Q1$ is in saturation and Vo = VCE(sat) (0 level). $(\mathbf{Y}=\overline{A+B}\ .\ \mathbf{Y}=\overline{A})$

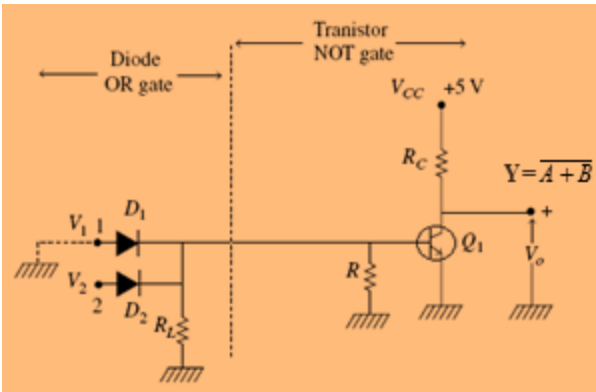


FIGURE 5.11 A DTL NOR gate

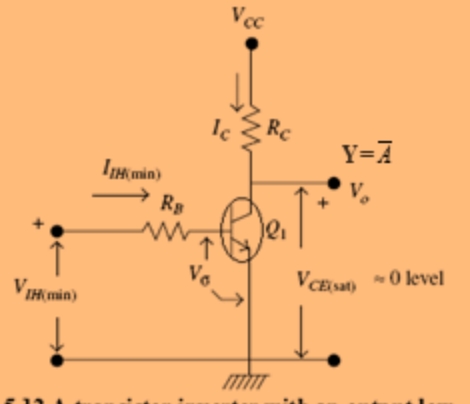


FIGURE 5.12 A transistor inverter with an output low

To realize the basic idea, the diodes are *reverse connected* and *forward biased* by an additional voltage source *+V* (a power supply) through the pull-up resistor R1. The input voltage sources are connected in opposite direction to the supplying voltage source (traveling along the loop +V - R1 - D - Vin). To invert the output voltage and to get a grounded output, the complementary voltage drop (*+V - VR1*) between the output and ground is taken as an output instead the floating voltage drop *VR1* across the resistor.

Tri-state logic: When there are three states i.e. state 0, state 1 and high impendence i.e. called Tri-state logic. High impedance is considered as state when no current pass through circuit. Although in state 0 and state 1 circuit functions and current flows through it.

4. TTL Inverter:

Tristate TTL inverter utilizer the high-speed operation of totem-pole arrangement while permitting outputs to be wired ANDed (connected together). It is called tristate TTL because it allows three possible output stages. HIGH, LOW and High-Impedance.

We know that transistor T3 is ON when output is HIGH and T4 is ON when output is LOW. In the high impedance state both transistors, transistor T3 and T4 in the totem pole arrangement are med OFF. As a result the output is open or floating, it is neither LOW nor HIGH. The circuit of Figure5.13 shows the simplified tristate inverter. It has two inputs A and E. A is the normal logic input whereas E is an ENABLE input. When ENABLE input is HIGH, the circuit works as a normal inverter.

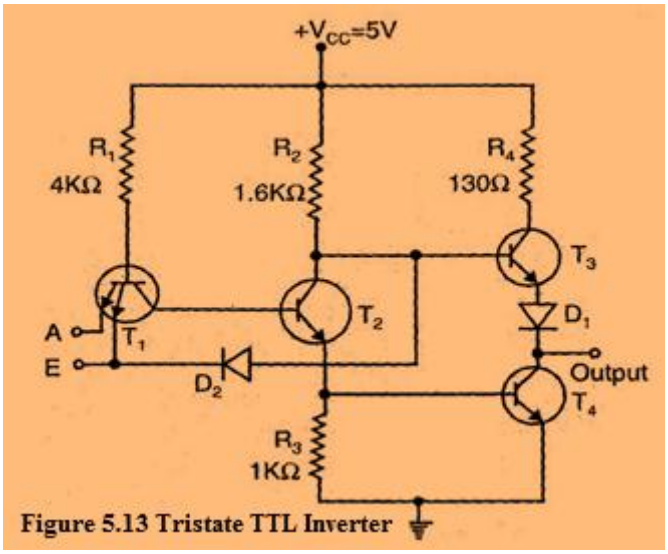


Figure 5.13 Tristate TTL Inverter

Because when E is HIGH, the state-of the transistor T1 (either ON or OFF) depends on the logic input A and the additional component diode is open circuited as cathode is at logic HIGH. When ENABLE input is LOW, regardless of the state of logic input the base emitter junction of T is forward biased and as a result it turns ON. This shunts the current through R1 away from T2 making it OFF. As T2 is OFF, there is no sufficient drive for T4 conduct and hence T4 turns OFF. The LOW at ENABLE input also forward biases diode D2, which shunt the current away from the base of T3, making it OFF. In this way, when ENABLE output is LOW, both transistors are OFF and output is at high impedance state.

Open Collector TTL NAND Gate and Its Operation:

The circuit diagram of 2-input NAND gate open-collector TTL gate is as shown in Figure5.14

Working:

Case.1: When A = 0,B = 0

When both inputs A and B are low, both functions of Q1 are forward biased and Q2 remains off. So no current flows through R4 and Q3 is also off and its collector voltage is equal to Vcc i.e. Y = 1

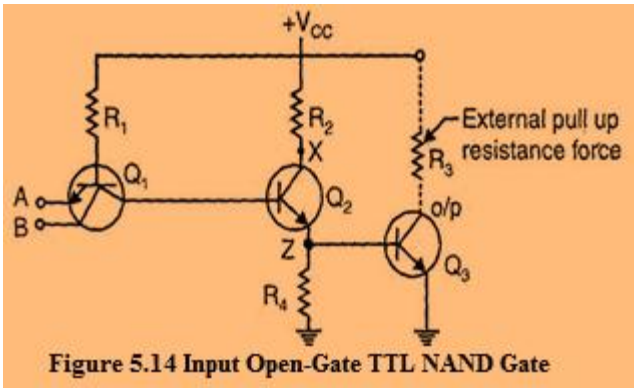


Figure 5.14 Input Open-Gate TTL NAND Gate

Case2 : When A = 0, B = 1 and

Case 3: When A = 1, B = 0.

When one input is high and. other is low, then one junction is forward biased so Q2 is off and Q3 is also off. So collector voltage is equal to Vcc i.e. Y = 1

Case 4: When A = 1, B = 1.

When both inputs are high, Q1 is turned off and Q2 turned 'ON' Q3 goes into saturation and hence Y = 0. The open-collector output has main advantage that wired AND ing is possible in it.

TTL NAND Gate:

Two inputs TTL NAND gate-is given in figure5.15. In this transistor T3 and T4 form a totem pole. Such type of configuration is called-as totem-pole output or active pull up output.

So, when A = 0 and B = 1 or (+5V). T1 conducts and T2 switch off. Since T2 is like an open switch, no current flows through it. But the current flows through the resistor R2 and into the base of transistor T3 to turn it ON.

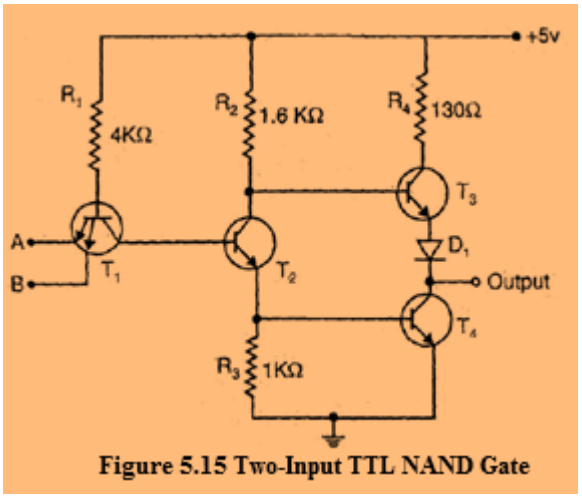


Figure 5.15 Two-Input TTL NAND Gate

T4 remains OFF because there is no path through which it can receive base current. The output current flows through resistor R4 and diode D1. Thus, we get high' output. When both inputs are high i.e. A = B = 1 or (+ 5V), T2 is ON and it drives T4 turning it ON. It is noted that the voltage at the base of T3 equals the sum of the base to emitter drop of T4 and $V_{CE(sat)}$ of T2. The diode D1 does not allow base-emitter junction of T3 to be forward-biased and hence, T3 remains OFF when T4 is ON. Thus, we get low output. It works as TTL NAND gate.

TTL Totem Pole NAND Gate:

In TTL Totem pole NAND gate, multiple emitter transistor as input is used. The no. of inputs may be from 2 to 8 emitters. The circuit diagram is as shown in Figure 5.16.

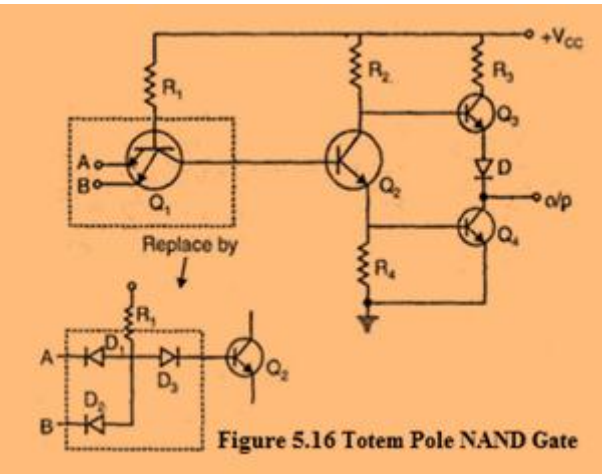


Figure 5.16 Totem Pole NAND Gate

Case 1:

When A = 0, B = 0

Now D1 and D2 both conduct, hence D3 will be off and make Q2 off. So its collector voltage rises and make Q3 'ON' and Q4 off; Hence output at Y = 1 (High)

Case 2 and Case 3:

If A = 0, B = 1 and A = 1, B=0

In both cases, the diode corresponding to low input will conduct and hence diode P3 will be OFF making Q2 OFF. In a similar way its collector voltage rises Q3 'ON' and Q4 'OFF'. Hence output voltage Y = 1 (High).

Case 4: A = 1, B = 1

Both diodes D1 and D2 will be off. D3 will be 'ON' and Q2 will 'ON' making Q4 also 'ON'. But Q3 will be 'OFF'. So output voltage Y = 0.

All the four cases shows that circuit operates as a NAND gate.

Totem pole can't be Wired ANDed due to current spike problem. The transistors used in circuits may get damaged over a period of time though not immediately. Sometimes voltage level rises high than the allowable.

Compare Standard TTL, Low Power TTL and High Speed TTL Logic Families:

Name of the Logic Family	Propagation Delay (ns)	Power Dissipation(mw)	Fan out	Max. Clock Rate(MHz)
1.Standard TTL	9	10	10	35
2.Low power TTL	33	1	20	3
3.High speed TTL	6	23	10	50

5. ECL OR Gate:

ECL OR gate: Emitter-coupled logic (ECL) is the fastest of all logic families and thus it is used in applications where very high speed is essential. High speeds have become possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven

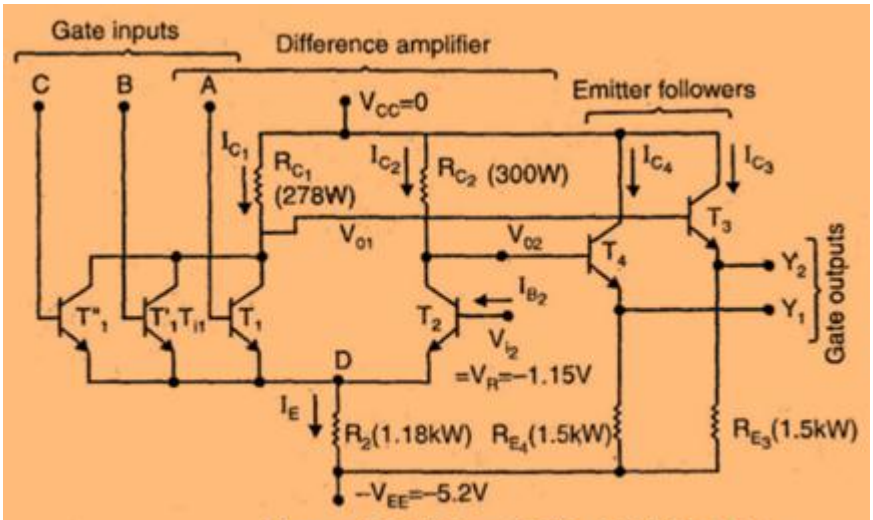


Figure 5.17 3-Input ECL OR/NOR Gate

into saturation and thereby the storage time is eliminated. Here, rather than switching the transistors from ON to OFF and vice-versa, they are switched between cut-off and active regions. Propagation delays of less than 1 ns per gate have become possible in ECL. Basically, ECL is realized using difference amplifier in which the emitters of the two transistors are connected and hence it referred to as emitter-coupled logic. A 3-input ECL gate is shown in Figure 5.17 which has three parts. The middle part is the difference amplifier which performs the logic operation.

Emitter followers are used for d.c. level shifting of the outputs, so that V (0) and V (1) are same for the inputs and the outputs. Note that two outputs Y1 and Y2 are available in this circuit which is complementary. Y1. Corresponds to OR logic and Y2 to NOR logic and hence it is named as an OR/NOR gate.

Additional transistors are used in parallel to T1 to get the required fan-in. There is a fundamental difference between all other logic families (including MOS logic) and ECL as far as the supply voltage is concerned. In ECL, the positive end of the supply is connected to ground in contrast to other logic families in which negative end of the supply is grounded. This is done to minimize the effect of noise induced in the power supply and protection of the gate from an accidental short circuit developing between the output of a gate and ground. The voltage corresponding to V (0) and V (1) are both negative due to positive end of the supply being connected to ground. The symbol of an ECL OR/NOR gate is shown in Fig.5.18.

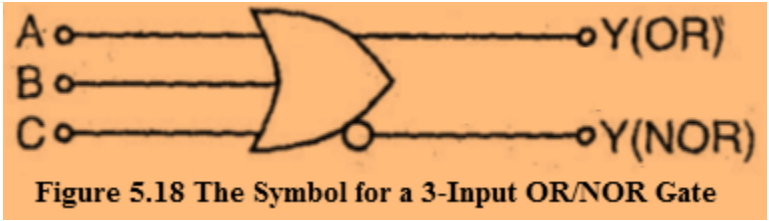


Figure 5.18 The Symbol for a 3-Input OR/NOR Gate

Two Input ECL NOR Gate: The circuit diagram of two inputs ECL NOR gate is as shown in Figure 5.19

Working:

Case I: When A = B = 0, the reference voltage of T3 is more forward biased then T1 and T2. Thus, T3 is ON and T1, T2 remains OFF. The value of R1 is such-that the output of NOR gate is high .i.e. '1'.

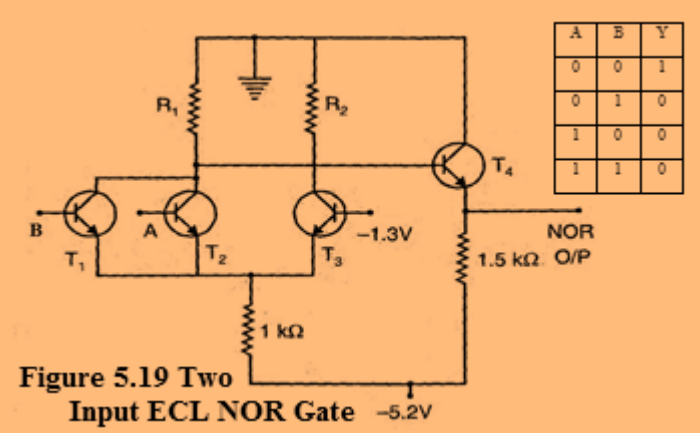


Figure 5.19 Two Input ECL NOR Gate

Case II: When A = 1 or B = 1 or A = B = 1, the corresponding transistors are ON, as they are more forward biased that T3 and thus T3 is OFF. Which makes the NOR output to below i.e. '0'. This shows that the circuit works as a NOR gate.

Comparison of the Important Characteristics of Various IC Logic Families:

	Parameter	RTL	I²L	DTL	HTL	TTL	ECL	MOS	CMOS
1.	Basic Gate	NOR	NOR	NAND	NAND	NAND	OR-NOR	NAND	NOR or NAND
2.	Fan-out	5	Depends on injector current	8	10	10 to 20	25	20	20 to 50
3.	Power dissip-ation in mW	12	6mm to 70 µM	8-12	55	10	40-55	0.2-10	0.0025
4.	Noise immunity	Nominal	Poor	Good	Excellent	Very Good	Poor	Good	Very Good
5.	Propagation delay (in sec.)	12	25-250	30	90	10	0.75	300	70.0
6.	Clock rate (MHZ)	8	–	72	4	35	>60	2	10
7.	Available functions	High	LSI only	Fairly high	Nominal	Very high	High	low	High

Monolithic Integrated Circuit Logic Families Compared:

The following logic families would either have been used to build up systems from functional blocks such as flip-flops, counters, and gates, or else would be used as "glue" logic to interconnect very-large scale integration devices such as memory and processors. Not shown are some early obscure logic families from the early 1960s such as DCTL (direct-coupled transistor logic), which did not become widely available.

Propagation delay is the time taken for a two-input NAND gate to produce a result after a change of state at its inputs. Toggle speed represents the fastest speed at which a J-K flip flop could operate. Power per gate is for an individual 2-input NAND gate; usually there would be more than one gate per IC package. Values are very typical and would vary slightly depending on application conditions, manufacturer, temperature, and particular type of logic circuit. Introduction year is when at least some of the devices of the family were available in volume for civilian uses. Some military applications pre-dated civilian use.

Family	Description	Propagation delay (ns)	Toggle speed (MHz)	Power per gate @1 MHz (mW)	Typical supply voltage V (range)	Introduction year	Remarks
RTL	Resistor–transistor logic	4	10	3.3	1963	The first CPU built from integrated circuits (the Apollo Guidance Computer) used RTL.	
DTL	Diode–transistor logic	10	5	1962	Introduced by Signetics, Fairchild 930 line became industry standard in 1964		
CMOS	AC/ACT	3	125	0.5	3.3 or 5 (2-6 or 4.5-5.5)	1985	ACT has TTL Compatible levels
CMOS	HC/HCT	9	50	0.5	5 (2-6 or 4.5-5.5)	1982	HCT has TTL compatible levels
CMOS	4000B/74C	30	5	1.2	10V (3-18)	1970	Approximately half speed and power at 5 volts
TTL	Original series	10	25	10	5 (4.75-5.25)	1964	Several manufacturers

Family	Description	Propagation delay (ns)	Toggle speed (MHz)	Power per gate @1 MHz (mW)	Typical supply voltage V (range)	Introduction year	Remarks
TTL	L	33	3	1	5 (4.75-5.25)	1964	Low power
TTL	H	6	43	22	5 (4.75-5.25)	1964	High speed
TTL	S	3	100	19	5 (4.75-5.25)	1969	Schottky high speed
TTL	LS	10	40	2	5 (4.75-5.25)	1976	Low power Schottky high speed
TTL	ALS	4	50	1.3	5 (4.5-5.5)	1976	Advanced Low power Schottky
TTL	F	3.5	100	5.4	5 (4.75-5.25)	1979	Fast
TTL	AS	2	105	8	5 (4.5-5.5)	1980	Advanced Schottky
TTL	G	1.5	1125 (1.125 GHz)	1.65 - 3.6	2004	First GHz 7400 series logic	
ECL	ECL III	1	500	60	-5.2(-5.19 - -5.21)	1968	Improved ECL
ECL	MECL I	8	31	-5.2	1962	first integrated logic circuit commercially produced	
ECL	ECL 10K	2	125	25	-5.2(-5.19 - -5.21)	1971	Motorola
ECL	ECL 100K	0.75	350	40	-4.5(-4.2 - -5.2)	1981	
ECL	ECL 100KH	1	250	25	-5.2(-4.9 - -5.5)	1981	

CMOS Logic Family:

The CMOS (Complementary Metal Oxide Semiconductor) logic family uses both N-type and P-type MOSFETs (enhancement MOSFETs, to be more precise) to realize different logic functions. The two types of MOSFET are designed to have matching characteristics. That is, they exhibit identical characteristics in switch-OFF and switch-ON conditions. The main advantage of the CMOS logic family over bipolar logic families discussed so far lies in its extremely low power dissipation, which is near-zero in static conditions. In fact, CMOS devices draw power only when they are switching. This allows integration of a much larger number of CMOS gates on a chip than would have been possible with bipolar or NMOS (to be discussed later) technology. CMOS technology today is the dominant semiconductor technology used for making microprocessors, memory devices and application-specific integrated circuits (ASICs). The CMOS logic family, like TTL, has a large number of subfamilies. The prominent members of CMOS logic were listed in an earlier part of the chapter. The basic difference between different CMOS logic subfamilies such as 4000A, 4000B, 4000UB, 74C, 74HC, 74HCT, 74AC and 74ACT is in the fabrication process used and not in the design of the circuits employed to implement the intended logic function. We will firstly look at the circuit implementation of various logic functions in CMOS and then follow this up with a brief description of different subfamilies of CMOS logic.

(ii) Tri-state logic: When there are three states i.e. state 0, state 1 and high impendence i.e. called Tri-state logic. High impedance is considered as state when no current pass through circuit. Although in state 0 and state 1 circuit functions and current flows through it.

Characteristics and Specification of CMOS:

1) Power supply (VDD) = 3 — 15 Volts

2) Power dissipation (Pd) = 10 nW, 3) Propagation delay (td) = 25 ns, 4) Noise margine (NM) = 45% of VDD 5) Fan out (FO) = >50

Circuit Implementation of Logic Functions:

In the following paragraphs, we will briefly describe the internal schematics of basic logic functions when implemented in CMOS logic. These include inverter, NAND, NOR, AND, OR, EX-OR, EX-NOR and AND-OR-INVERT functions.

(i) CMOS inverter

(i) CMOS Inverter: It is complementary MOSFET obtained by using P-channel MOSPET and n-channel MOSFET simultaneously. The P and N channel are connected in series, their drains are connected together, output is taken from common drain point. Input is applied at common gate terminal. CMOS is very fast and consumes less power.

Case 1. When input Vi = 0. The V_{GS} (Gate source) voltage of Q1 will be 0 volt, it will be off. But Q2 will be ON; Hence output will be equal to +VDD or logic 1.

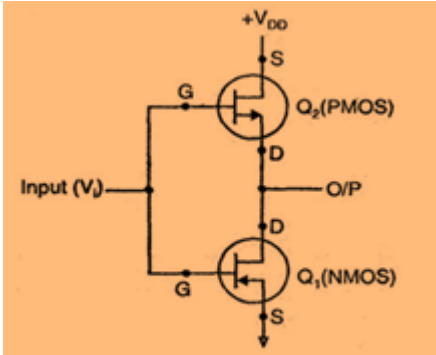


Figure 5.1 CMOS Inverter

Case 2. When input Vi = 1, The V_{GS} (Gate source) voltage of Q2 will be 0 volt, it will be OFF, But Q1 will be ON. Hence output will be connected to ground or logic 0.In this way, CMOS function as an inverter.

CMOS Inverter:

The inverter is the most fundamental building block of CMOS logic. It consists of a pair of N-channel and P-channel MOSFETs connected in cascade configuration as shown in Figure 5.20. The circuit functions as follows. When the input is in the HIGH state (logic '1'), P-channel MOSFET *Q*1 is in the cut-off state while the N-channel MOSFET *Q*2 is conducting. The conducting MOSFET provides a path from ground to output and the output is LOW (logic '0'). When the input is in the LOW state (logic '0'), *Q*1 is in conduction

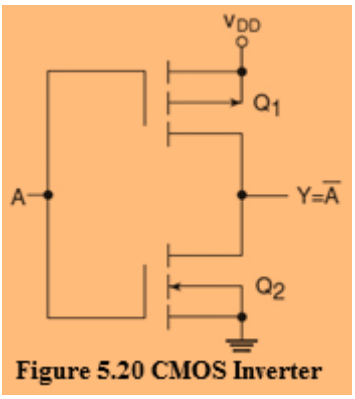


Figure 5.20 CMOS Inverter

while *Q*2 is in cut-off. The conducting P-channel device provides a path for *V*DD to appear at the output, so that the output is in HIGH or logic '1' state. A floating input could lead to conduction of both MOSFETs and a short-circuit condition. It should therefore be avoided. It is also evident from Figure 5.20 that there is no conduction path between *V*DD and ground in either of the input conditions, that is, when input is in logic '1' and '0' states. That is why there is practically zero power dissipation in static conditions. There is only dynamic power dissipation, which occurs during switching operations as the MOSFET gate capacitance is charged and discharged. The power dissipated is directly proportional to the switching frequency.

NAND Gate: Below shows the basic circuit implementation of a two-input NAND.

As shown in the Figure5.21, two P-channel MOSFETs (*Q*1 and *Q*2) are connected in parallel between *V*DD and the output terminal, and two N-channel MOSFETs (*Q*3 and *Q*4) are connected in series between ground and output terminal. The circuit operates as follows. For the output to be in a logic '0' state, it is essential that both the series-connected N-channel devices conduct and both the parallel-connected P-channel devices remain in the cut-off state. This is possible only when both the inputs are in a logic '1' state. This verifies one of the entries

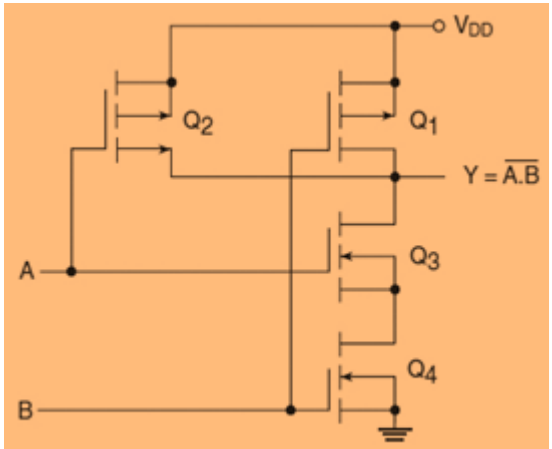


Figure 5.21 CMOS 2-Input NAND Gate

of the NAND gate truth table. When both the inputs are in a logic '0' state, both the N-channel devices are nonconducting and both the P-channel devices are conducting, which produces a logic '1' at the output. This verifies another entry of the NAND truth table. For the remaining two input combinations, either of the two N-channel devices will be nonconducting and either of the two parallel-connected P-channel devices will be conducting. We have either *Q*3 OFF and *Q*2 ON or *Q*4 OFF and *Q*1 ON. The output in both cases is a logic '1', which verifies the remaining entries of the truth table. From the circuit schematic of Figure 5. 21 we can visualize that under no possible input combination of logic states is there a direct conduction path between *V*DD and ground. This further confirms that there is near-zero power dissipation in CMOS gates under static conditions.

Figure 5.22 shows how the circuit of Figure 5.21 can be extended to build a three-input NAND gate. Operation of this circuit can be explained on similar lines. It may be mentioned here that series connection of MOSFETs adds to the propagation delay, which is greater in the case of P-channel devices than it is in the case of N-channel devices. As a result, the concept of extending the number of inputs as shown in Figure5.22 is usually limited to four inputs

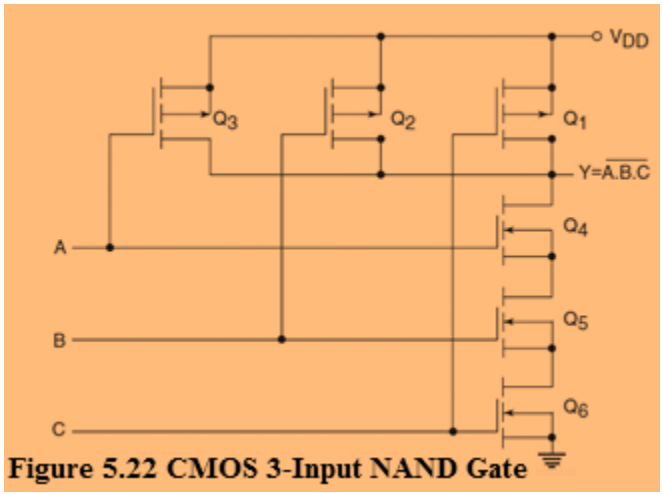


Figure 5.22 CMOS 3-Input NAND Gate

in the case of NAND and to three inputs in the case of NOR. The number is one less in the case of NOR because it uses series-connected P-channel devices. NAND and NOR gates with larger inputs are realized as a combination of simpler gates.

NOR Gate:

Figure 5.23 shows the basic circuit implementation of a two-input NOR. As shown in the figure, two P-channel MOSFETs (*Q*1 and *Q*2) are connected in series between *V*DD and the output terminal, and two N-channel MOSFETs (*Q*3 and *Q*4) are connected in parallel between ground and output terminal. The circuit operates as follows. For the output to be in a logic '1' state, it is essential that both the series-connected P-channel devices conduct and both the parallel-connected N-channel devices remain in the cut-off state. This is possible only when both the inputs are in a logic '0' state. This verifies one of the entries of the

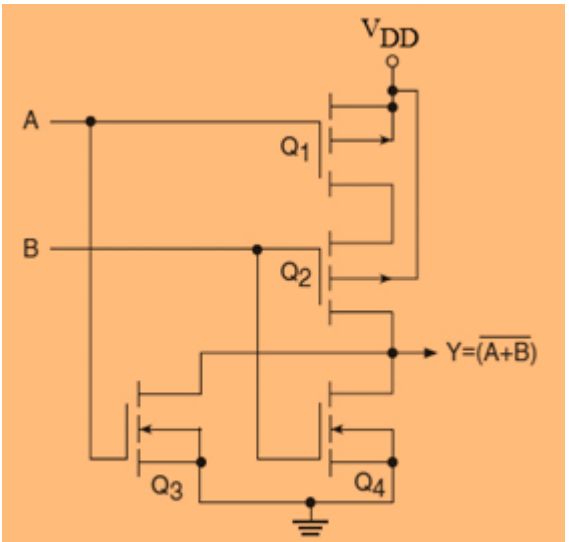


Figure 5.23 CMOS 2-Input NOR Gate

NOR gate truth table. When both the inputs are in a logic '1' state, both the N-channel devices are conducting and both the P-channel devices are non-conducting, which produces a logic '0' at the output. This verifies another entry of the NOR truth table. For the remaining two input combinations, either of the two parallel N-channel devices will be conducting and either of the two series-connected P-channel devices will be non-conducting. We have either *Q*1 OFF and *Q*3 ON or *Q*2 OFF and *Q*4 ON. The output in both cases is logic '0', which verifies the remaining entries of the truth table.

EXCLUSIVE-OR Gate: **Y=** $A \oplus B$

An EXCLUSIVE-OR gate is implemented using the logic diagram of Figure 5.24 As is evident from the figure, the output of this logic arrangement can be expressed by

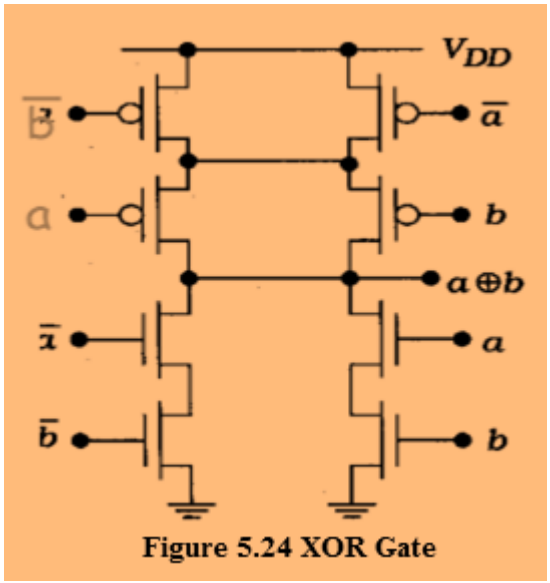


Figure 5.24 XOR Gate

Exclusive-OR (XOR)

- $a \oplus b = \overline{a} \cdot b + a \cdot \overline{b}$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

EXCLUSIVE-NOR: **Y=** $\overline{A \oplus B}$

An EXCLUSIVE-NOR gate is implemented using the logic diagram of Figure 5.25. As is evident from the figure, the output of this logic arrangement can be expressed by

Exclusive-NOR

$$\overline{a \oplus b} = a \cdot b + \overline{a} \cdot \overline{b}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

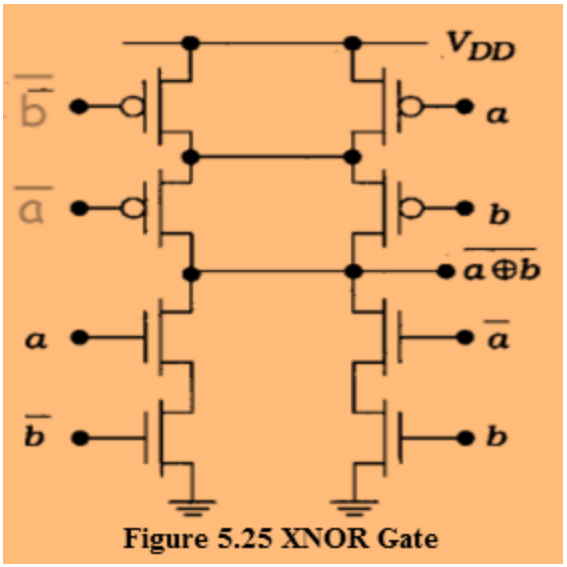


Figure 5.25 XNOR Gate

PMOS: PMOS gates are made using enhancement-mode p-channel MOS transistors. The Figure 5.26 shows the basic circuit of high-threshold p-channel gate. Note that the typical values of supply voltages are V_{DD}=-13V and V_{GG}=-27V. In some versions the drain of T_3 is tied to V_{GG} to eliminate one power supply. The negative supply is then referred to as V_{GG}. T_3 in this circuit is simply a resistive or current source load for T_1 and T_2. If the input A or B is at high voltage of a value nearly that of V_{CC} then T_1 or T_2 is off and then the output is pulled down to a low voltage near V_{DD} by T_3. When inputs A and B are both pulled to a low voltage near V_{DD} , T_1 and T_2 both conduct. This connects the output high level near V_{CC} . In positive logic this is a NOR gate. $Y = \overline{A}.\overline{B} = \overline{A+B}$.

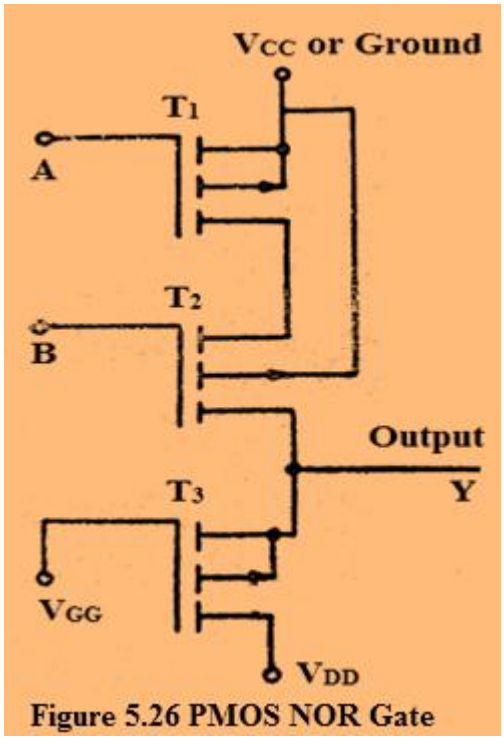


Figure 5.26 PMOS NOR Gate

NMOS: PMOS was the first MOS family because p-channel processing had less problems with contamination than N-channel processing. The higher speed and lower chip area per transistor possible with N-channel devices led manufacturers to develop NMOS devices as soon as processing technology permitted. Most of the present MOS memories and microprocessors use some variation of N-channel MOS.

Figures 5.27 and 5.28 show the circuits of basic NMOS NOR and NAND gates respectively. For the NOR gate in Figure 5.27, T_3 an N-channel enhancement FET, is simply a load resistor or a current source. In other wards T_3 is an active load. If inputs A and B are at a voltage near V_{GG}, T_1 and T_2 will be off and the output will be pulled to a voltage near V_{CC}. This corresponds to logic 1 output. If either the A input or the B input is pulled a voltage near

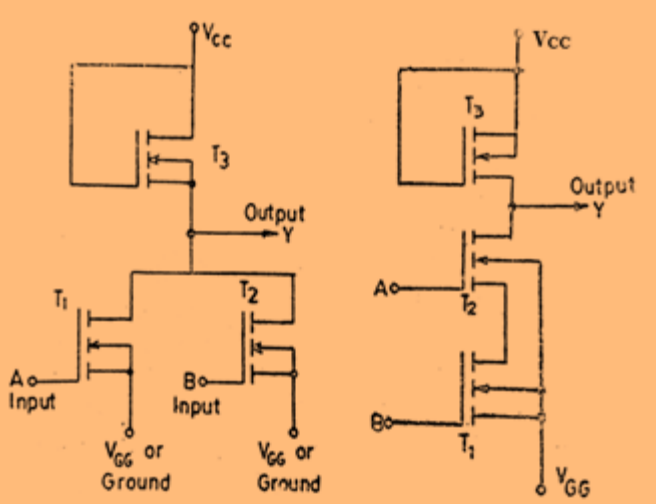


Figure 2.27 NMOS NOR Gate

Figure 2.28 NMOS NAND Gate

V_{CC} , T_1 or T_2 will turn ON and pull T_3 source voltage or the output to a low level near V_{GG}. This satisfies the expression for a positive logic NOR gate $Y = \overline{A}.\overline{B} = \overline{A+B}$.

The circuit in Figure 5.28 can be analyzed in a similar manner and it can be seen that the circuit performs the operation of an NAND gate. In the Figure 5.28, if the gates of both T_1 and T_2 be connected to V_{CC} both these transistors conduct and the output is pulled low. In all other conditions either T_1 or T_2 or both T_1 and T_2 will be OFF and hence the output is a High level as T_3 is ON.