PDCv2.0 - ICWSHLP2 - Datasheet

1 Overview

- Low power photon-to-digital converter
- Flag output for coincidence and timestamp
- Digital sum for photon count
- Analog monitor current output
- 4096 pixels with enable / disable
- Die size of $5.3 \times 5.85\ mm^2$
- 64 internal 2D CMOS SPAD
- TSMC 180 nm BCD process

2 Features

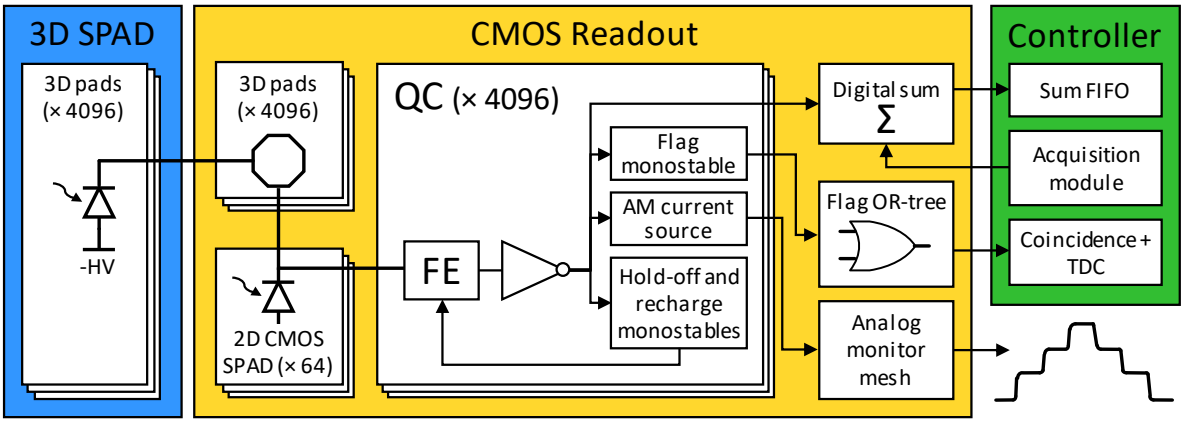
- Adjustable hold-off time from 10 ns to 10 µs
- Adjustable recharge time from 2 ns to 60 ns
- Adjustable flag duration from 2 ns to 60 ns
- Adjustable analog monitor current from 0 to 30 µA
- Programmable FIFO with up to 128 bins
- Timing resolution below 250 ps
- 5 V front-end and 1.8 V core and IOs
- Leakage standby power as low as 90 µW
- Maximum clock frequency of 100 MHz

3 Description

This PDC is a Photon to Digital Converter for low power applications. It benefits from the digital nature of a Single Photon Avalanche Diode (SPAD) to remain in the digital domain. The device contains 4096 pixels with each its own 3D interconnect pad. The PDC provides a quenching circuit for each pixel that senses the avalanche with an inverter for a low-power operation. A digitally adjustable hold-off period reduces the afterpulse probability up to 10 µs.

The PDC generates three different types of information. Two of them indicate the number of triggered pixels: a digital sum register and an analog monitor based on current sources. The third type consists of an asynchronous flag signal with a timing resolution below 250 ps. The PDC can be controlled by an external FPGA or a custom ASIC known as the Tile Controller. Using multiple PDC flags, the Controller can implement a coincidence algorithm to filter the dark count, or it can trigger an acquisition for each flag. The acquisition starts when enough photons from different PDCs are received on the same tile in a configurable time window. The photons detected from each pixel are then digitally summed in single acquisition. The sum can also be produced with a continuous sampling period down to 10 ns for pulse shape discrimination applications. The result is placed in the up to 128-bin FIFO that will later be serialized and sent to the Controller on request. To reduce power consumption, a digital clock is only required to complete an acquisition or to transmit data to the Controller, otherwise, it can be turned off.

Simplified Schematic



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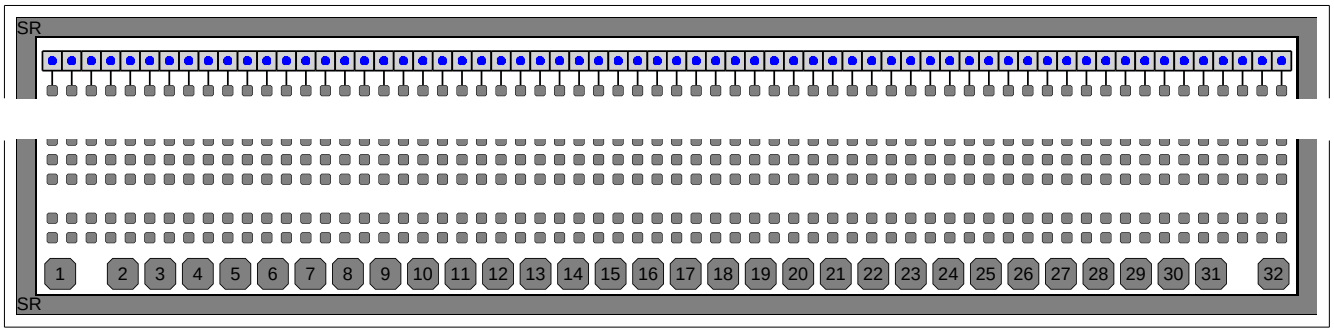
5 Pin Configuration and Functions



Pin Functions

PIN NAME	NO.	TYPE[1]	RAIL	DESCRIPTION
HV	1	P		Negative high-voltage to bias the SPADs.
VSS	2	P		VSS pin.
VDD_FE	3	P	5V0	Power supply pin for analog front-end.
CFG_RTN_EN	4	I	1V8	Input to enable/disable the return (RTN) signals to implement a configuration daisy chain of multiple PDCs. Internal pull-up.
VSS	5	P		VSS pin.
CFG_DATA	6	I	1V8	Serial input of the PDC to receive configurations and commands.
VDD_CORE	7	P	1V8	Power supply pin for digital core.
CFG_CLK	8	I	1V8	Configuration clock of the PDC to receive configurations and commands.
VSS	9	P		VSS pin.
CFG_CLK_RTN	10	O	1V8	Configuration clock return of the PDC to implement a configuration daisy chain of multiple PDCs.
VDD_IO	11	P	1V8	Power supply pin for digital output buffers.
CFG_DATA_RTN	12	O	1V8	Serial output of the PDC to implement a configuration daisy chain of multiple PDCs.
VSS	13	P		VSS pin.
VSS	14	P		VSS pin.
VDD_AM	15	P	5V0	Power supply pin for analog monitor. This rail can be powered off to reduce power consumption. If used, always connect both pins.
AM	16	AO	5V0	Analog monitor output. Current sum proportional to the number of detected photons.
AM	17	AO	5V0	Analog monitor output. Current sum proportional to the number of detected photons.
VDD_AM	18	P	5V0	Power supply pin for analog monitor. This rail can be powered off to reduce power consumption. If used, always connect both pins.
VSS	19	P		VSS pin.
VSS	20	P		VSS pin.

Pin Functions (continued)

PIN NAME	NO.	TYPE[1]	RAIL	DESCRIPTION
FLAG	21	O	1V8	FLAG digital output. Its primary function is to indicate the presence of one or more detected photons. Its purpose can also be reconfigured to any supported output signal.
VDD_IO	22	P	1V8	Power supply pin for digital output buffers.
DATA	23	O	1V8	DATA digital output. Its primary function is to transmit the result of the digital sum. Its purpose can also be reconfigured to any supported output signal.
VSS	24	P		VSS pin.
CLK	25	I	1V8	PDC principal clock. Used as the clock in acquisition mode. Used as a chip select in configuration mode. Used a trigger input in trigger mode.
VDD_CORE	26	P	1V8	Power supply pin for digital core.
POR_DIS	27	I	1V8	Power-On Reset disable. Internal pull-down.
VSS	28	P		VSS pin.
RSTN	29	I	1V8	Active-low reset input. Internal pull-up.
VDD_FE	30	P	5V0	Power supply pin for analog front-end.
VSS	31	P		VSS pin.
HV	32	P		Negative high-voltage to bias the SPADs.
SEAL RING	SR	P		Mechanical seal ring for 3D bonding with the SPAD. Connected to HV. Do not use for wire bonding.
VSS (Substrate)	SUB	P		Substrate. VSS pin.

[1] KEY: I = Input, O = Output, AI = Analog Input, AO = Analog Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
VDD_CORE to VSS	-0.3	1.98	V
VDD_IO to VSS	-0.3	1.98	V
VDD_FE to VSS	-0.3	5.50	V
VDD_AM to VSS	-0.3	5.50	V
Digital input voltage to VSS	-0.3	VDD_CORE + 0.3	V
CMOS SPAD high voltage (HV) to VSS	-50[1]	0	V
Supply pads maximum input current		97.6	mA
VSS pads maximum return current		97.6	mA
Digital ouputs maximum current		50	mA
Analog monitor output maximum current		50	mA
Maximum operating junction temperature		125	°C

[1] Specified at room temperature. Refer to SPAD datasheet.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Target human body model (HBM)[1]	±2000	V
		Target machine model (MM)[1]	±200	

[1] These ratings come from design, not measured nor qualified.

6.3 Recommended Operation Conditions

		MIN	NOM	MAX	UNIT
VDD_CORE	Core supply voltage range	1.70	1.80	1.90	V
VDD_IO	Output buffers supply voltage range	1.70	1.80	1.90	V
VDD_FE	Quench front-end supply voltage range	4.75	5.00	5.25	V
VDD_AM	Analog monitor supply voltage range	4.75	5.00	5.25	V
T_A	Ambient temperature	-200	25	100	°C

6.4 Electrical Characteristics

PARAMETERS		TEST CONDITION	MIN	TYP	MAX	UNIT
DIGITAL INPUT PINS: CFG_RTN_EN, CFG_DATA, CFG_CLK, CLK, POR_DIS, RSTN						
V_{IH}	High input threshold		0.92			V
V_{IL}	Low input threshold				0.68	V
RPULL_DOWN - INTERNAL PULL-DOWN RESISTOR FOR DIGITAL INPUTS						
R_{POR_DIS}	Internal pull-down resistor			2.5		MΩ
RPULL_UP - INTERNAL PULL-UP RESISTOR FOR DIGITAL INPUTS						
$R_{CFG\_RTN\_EN}$	Internal pull-up resistor			2.5		MΩ
R_{RSTN}	Internal pull-up resistor			2.5		MΩ
DIGITAL OUTPUT PINS: CFG_CLK_RTN, CFG_DATA_RTN, FLAG, DATA						
R_{CFG_CLK}	Output impedance			50		Ω
R_{CFG_DATA}	Output impedance			50		Ω
R_{FLAG}	Output impedance			50		Ω
R_{DATA}	Output impedance			50		Ω

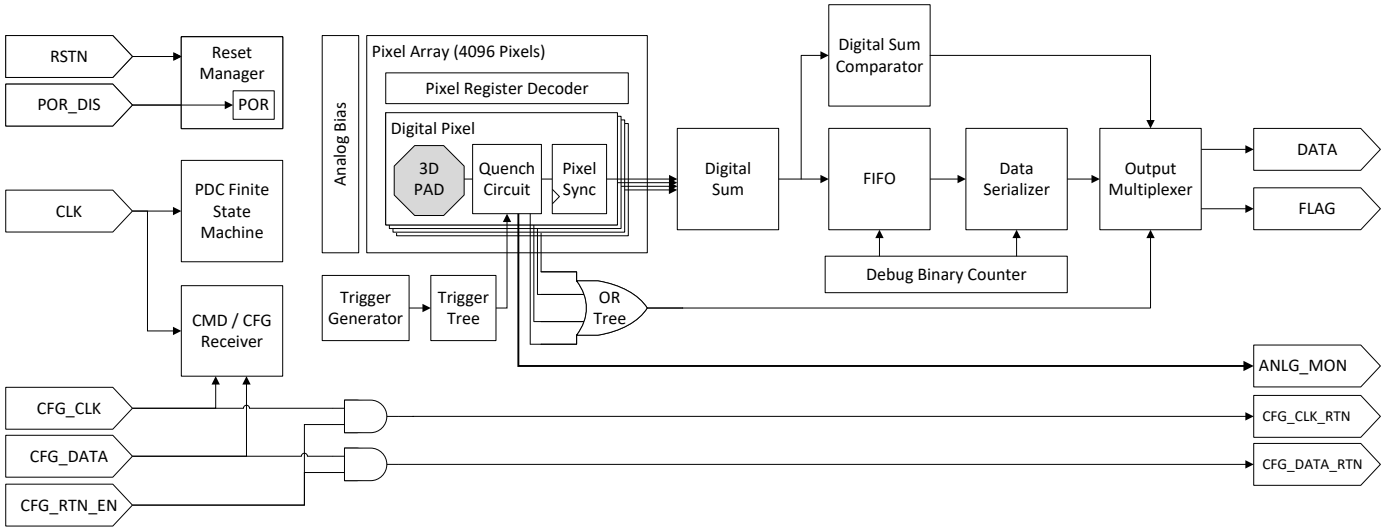
6.5 Timing Requirements

		MIN	TYP	MAX	UNIT
T_{CLK}	CLK input period	10			ns
T_{CFG_CLK}	CFG_CLK input period	10			ns
$T_{EXT\_TRG\ (CLK)}$	External trigger pulse duration	5			ns
T_{RSTN}	RSTN pulse duration	20			ns

7 Detailed Description

7.1 Overview

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 SPAD

The PDCv2.0 contains a row of 64 2D CMOS SPADs to be used when the readout is not bonded with 3D SPADs. The SPADs are quenched at the cathode and thus require a negative high voltage bias of approximately -50 V. The active area of each SPAD is a rounded-corner square of 34 µm (1026 µm^2). This results in a single SPAD fill factor of 17 %. For more information regarding the SPAD performances and operation, refer to the appropriate SPAD datasheet.

7.3.2 Quenching Circuit

The PDC contains 4096 copies of the quenching circuits (QC) which is designed to read each SPAD from the cathode. As shown in Figure 4, the FRONT-END contains the 5V transistors to interface with the SPAD. Apart from the ANALOG_MONITOR, the rest of the logic uses 1.8 V transistors to reduce the power consumption. The RECHARGE LATCH ensures the hold-off/recharge cycle is not interrupted if the SPAD quenches itself for uniformity in the operation. The programmable HOLD-OFF MONOSTABLE sets the duration of the time before the recharge and the programmable RECHARGE MONOSTABLE sets the time while the SPAD is recharged. The recharge control signal is shifted back to 5 V to control the FRONT-END transistors. Two different triggers can be used to test the QC. A front-end trigger (FE_TRG) directly activates the transistors of the FRONT-END while the digital trigger (DGTL_TRG) only activates the 1.8 V logic. It also triggers the FLAG MONOSTABLE which sets the duration of the output pulse of the flag. The output QC_OUT goes to the pixel synchronization module for the digital sum.

Figure 4: Top block diagram of the quenching circuit of the PDC.

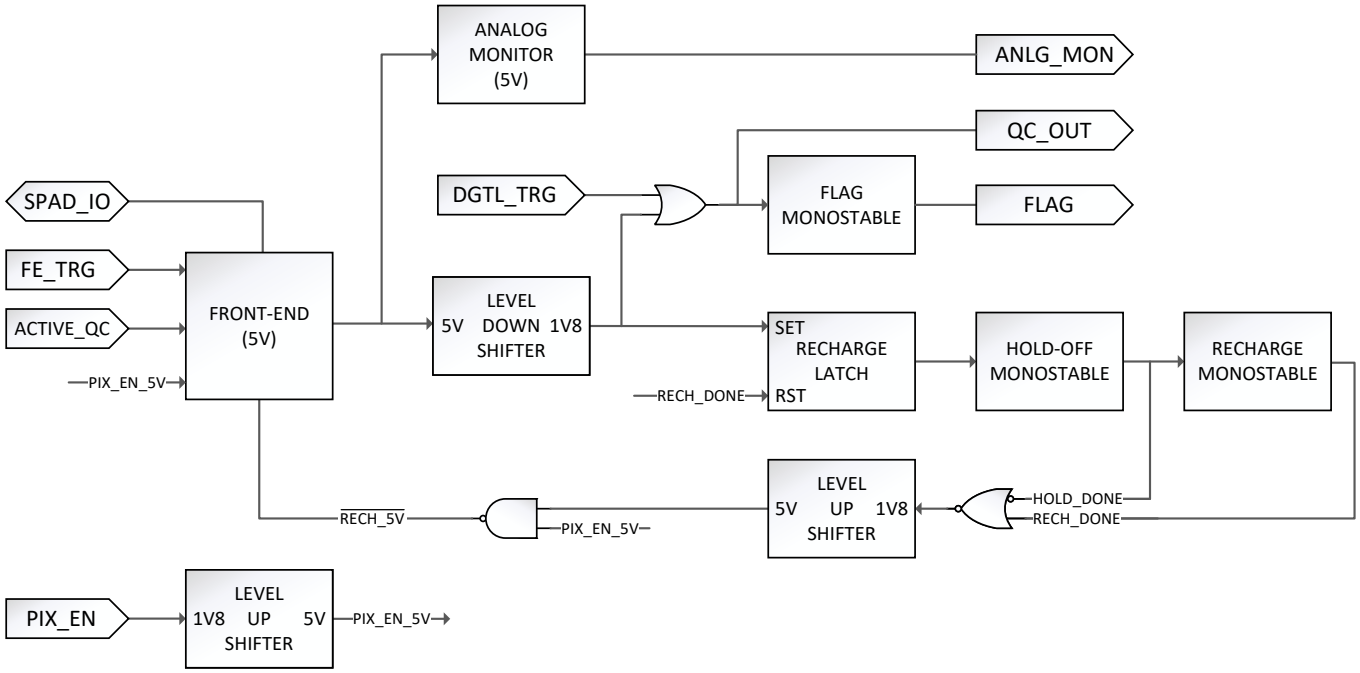


Figure 5 shows the front-end transistors to interface with the SPAD. M1 is the recharge transistor, M3 is the hold-off transistor to quench the SPAD through its open state impedance. M2 is a cascode transistor to double the possible SPAD overvoltage without allowing negative voltage on the READING_NODE. The unbalanced inverter I2 senses the avalanche and start the quenching sequence. The AND gate (G1) is used to gate the output signal when a pixel is disabled and during the recharge. Some more transistors can pull READING_NODE to VSS (M4, M5, M6, M7 and M8). M7 prevents any of those to enable during a recharge which would cause a short between VDD_FE (5 V) and VSS. M4 and M5 form an active quench which can be enabled/disabled by the PIXL register. M6 is the front-end trigger to test the QC without any SPAD. M8 forces the READING_NODE to VSS when a pixel is disabled.

Figure 5: Block diagram of the front-end of the quenching circuit of the PDC.

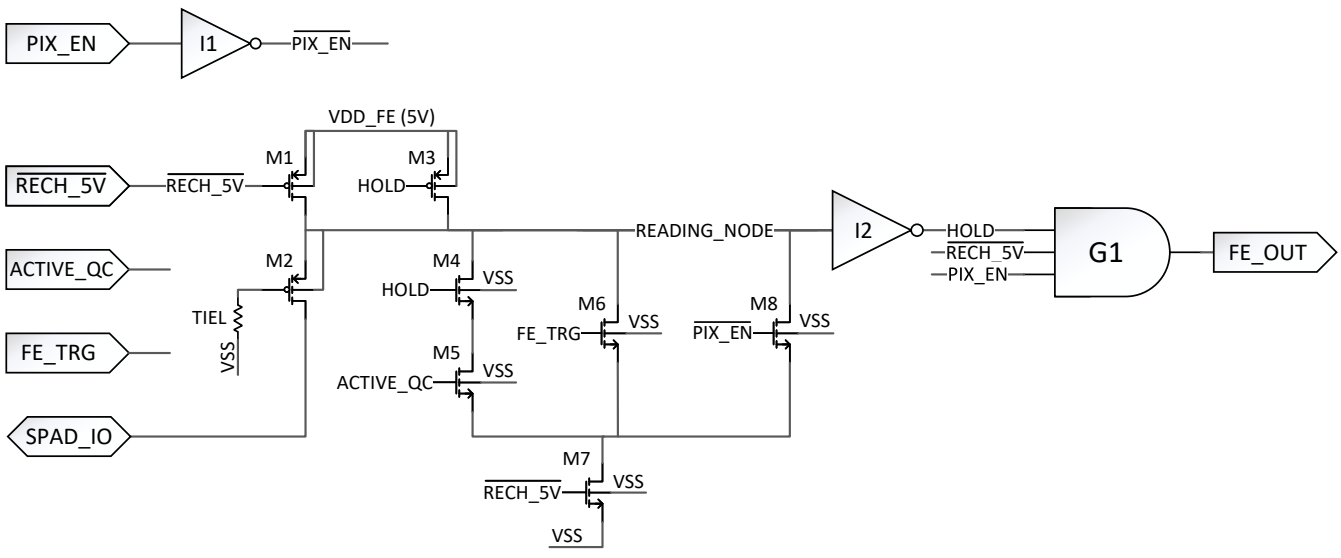
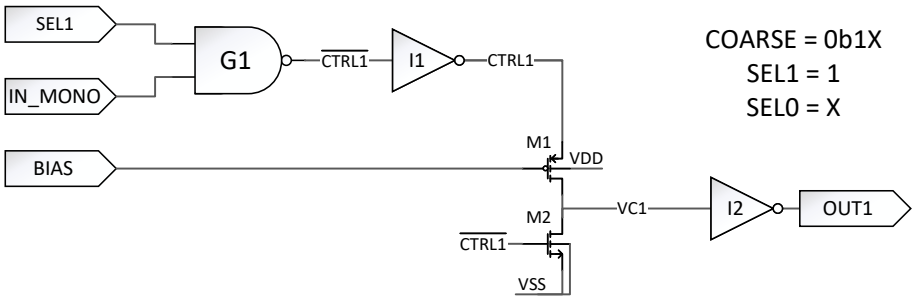


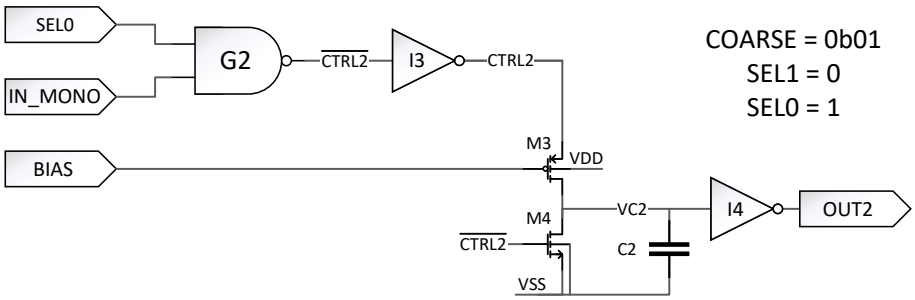
Figure 6 illustrates the three branches used to generate the different hold-off time ranges (TIME Register). Each range is based on a current source charging a capacitor. For the shortest range (Figure 6a), the gates on inverter I2 are used as a capacitor. The reference current is produced by M1 which is used as a current mirror. G1 enables the current source only when the shorter hold-off range is required and after the monostable is started (IN_MONO). M2 discharges the capacitance at the end of the monostable period to be ready for the next cycle. Figure 6b illustrates the middle range on which an extra capacitor is added to increase the hold-off time. To be selected this branch must enabled by the configuration registers. Figure 6c illustrates the longest range on which a larger capacitor is added to increase the hold-off time. This branch is always enabled. The three branches are combined together with the NAND gate G3 of Figure 6d which always selects the shortest enabled branch.

Figure 6: Block diagram of the hold-off monostable of the quenching circuit of the PDC

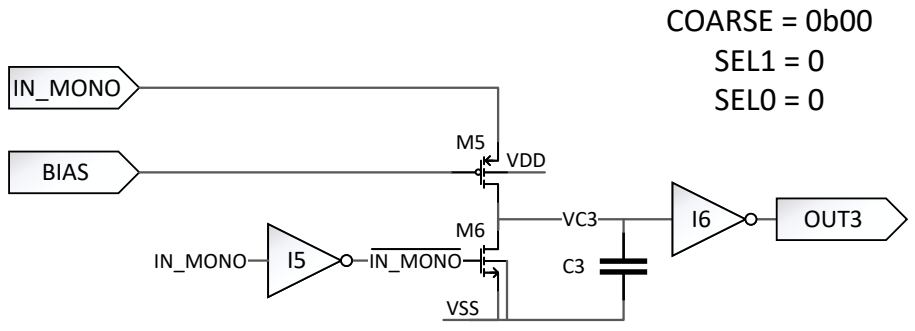
(a) SEL1X - Hold-off short range



(b) SEL01 - Hold-off middle range



(c) SEL00 - Hold-off longest range



(d) Hold-off output

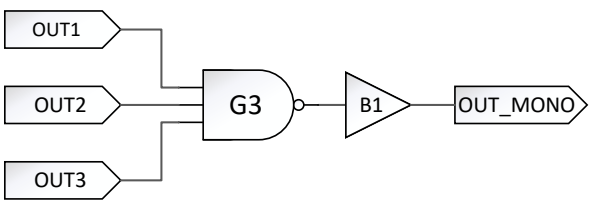


Figure 7 illustrates the recharge monostable. The monostable is adjustable to ensure the SPAD is fully recharged after the hold-off period even with the extra capacitance of the SPAD and its 3D bonding. As for the hold-off monostable, the duration is adjusted with the current source M1 charging the capacitance of the gates of inverter I3. The current source is activated when IN_MONO triggers and disabled at the end of the cycle. M2 then discharges the capacitance at the end of the cycle. G1 ensures that no recharge can occur when a pixel is disabled. This is also used for a proper boot up sequence since all pixels are disabled at boot up.

Figure 7: Block diagram of recharge monostable of the PDC quenching circuit.

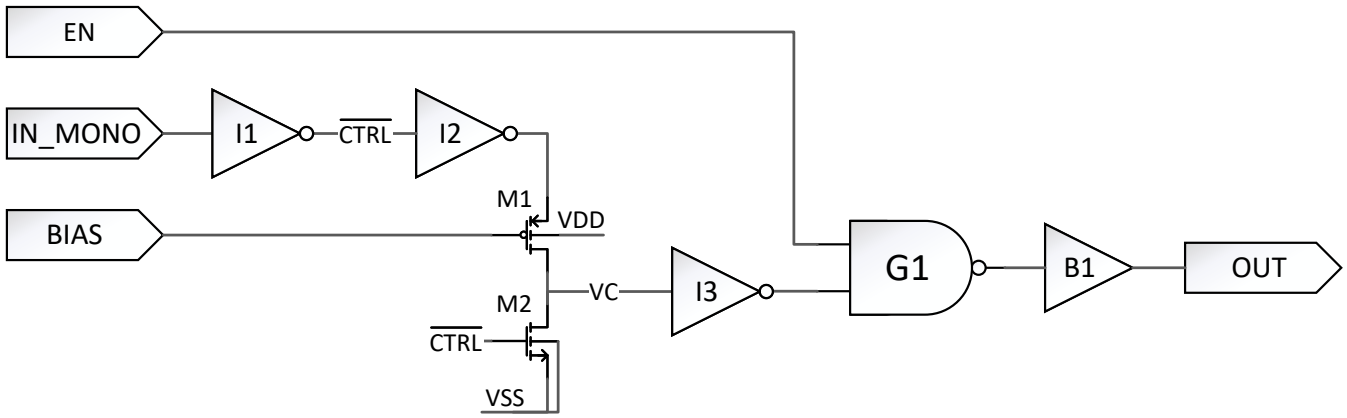


Figure 8 illustrates the flag monostable. The monostable to keep the pulse as short as possible to prevent saturation, but long enough to be detected. The flag monostable duration can only be shorter than the hold-off monostable. For example, if the hold-off is set to 10 ns, and the flag duration is set to 20 ns, the flag duration will be set to 10 ns because the hold-off pulse is shorter. This duration is adjusted with the current source M1 charging the capacitance of the gates of buffer B1. When the flag output is enabled (FLAG_EN) the current source is activated when IN_MONO triggers and disabled at the end of the cycle. M2 then discharges the capacitance at the end of the cycle. G2 generates a shorter pulse than the hold-off period (IN_MONO).

Figure 8: Block diagram of flag monostable of the PDC quenching circuit.

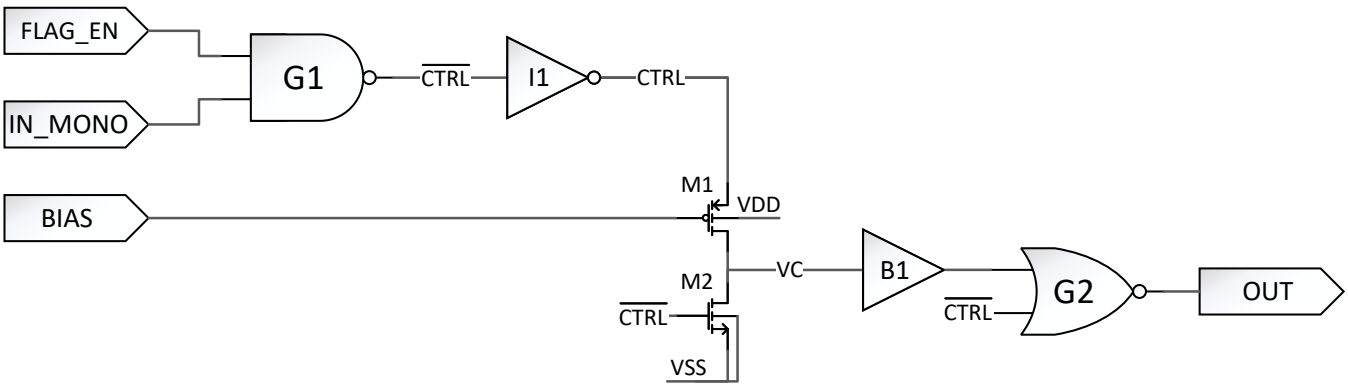
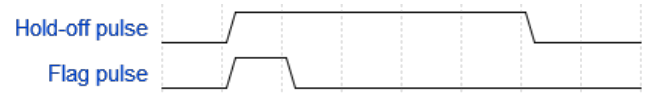
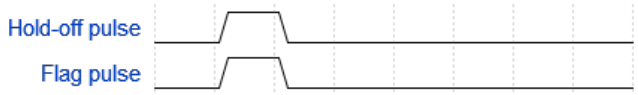


Figure 9: Chronogram of the hold-off and flag durations.

(a) Hold-off and flag duration respectively set to 50 ns and 10 ns. Both pulses duration match the setting.



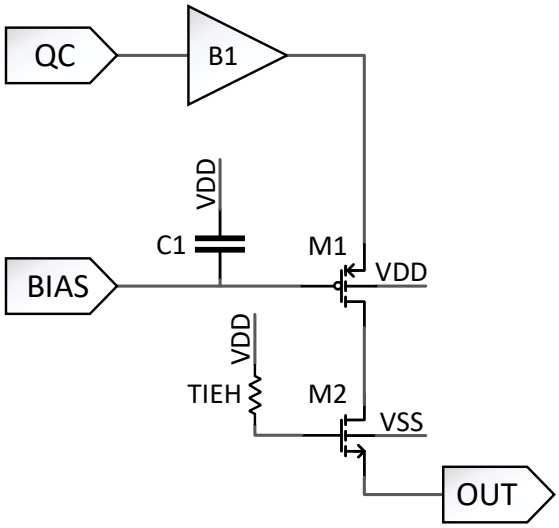
(b) Hold-off and flag duration respectively set to 10 ns and 20 ns. Flag pulse duration can't be longer than the hold-off.



7.3.3 Analog Monitor

Figure 10 illustrates the analog monitor circuit present in each pixel of the PDC. The output of the quenching circuit (QC) which is active during the complete hold-off period is buffed by B1 to drive the PMOS current mirror source M1. The output current is referenced from the analog monitor supply (VDD_AM = 5V). The bias (BIAS) is generated by the analog bias module to set the current amplitude of the analog monitor via the ANLG Register. C1 stabilizes the bias voltage and decouples it from the capacitive spikes when B1 output toggles. M2 NMOS prevents the current from returning into the pixel when the output voltage is higher than BIAS voltage.

Figure 10: Analog monitor current output.



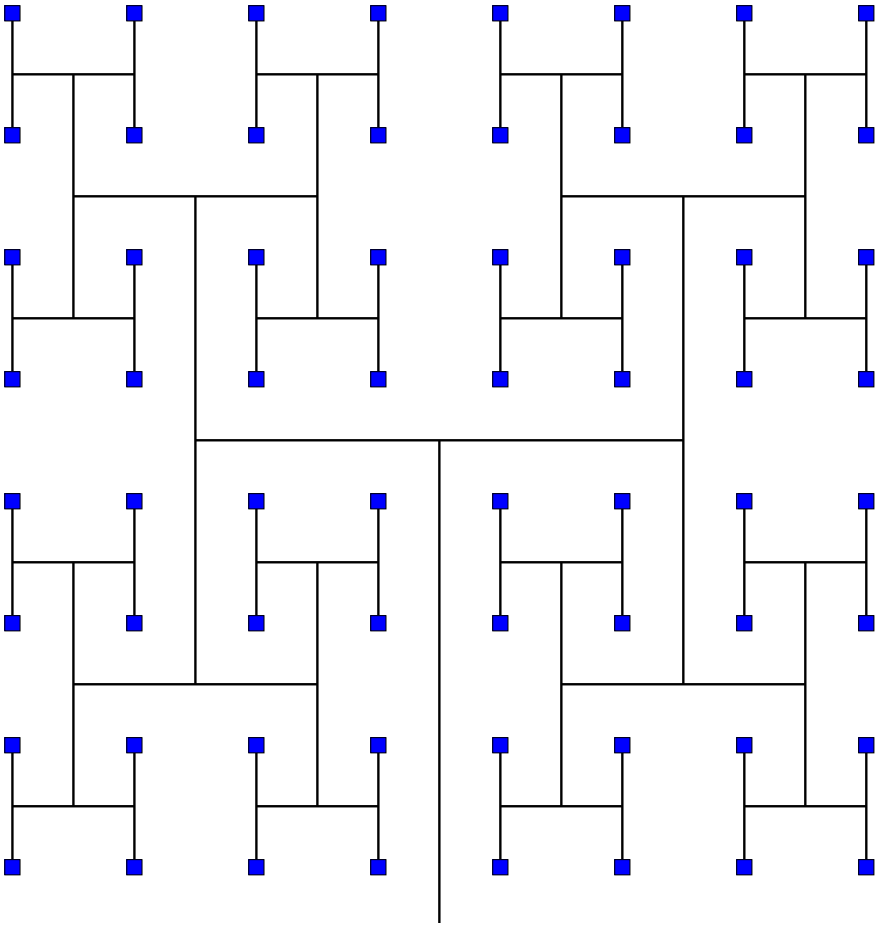
7.3.4 Analog Bias

To bias the analog monitor current amplitude and the different monostable durations, an analog bias module is implemented into the PDC. 4 different DAQs (analog monitor, hold-off time, recharge time and flag duration) adjusted by the configuration registers set the bias points. These bias are propagated to all the pixels of the PDC.

7.3.5 Flag OR-Tree

The FLAG output of the PDC can either be used to implement a coincidence algorithm between 1 or more PDCs or to get a timestamp with an external Time-to-Digital Converter. Since the PDC doesn't provide the index of the pixel that triggers, the difference in delay between each pixel and the FLAG output must be minimized. Otherwise, this skew will increase the system jitter of the FLAG output. To this end a H-Tree structure is implemented into the PDC to combine the pixels. Based on Figure 11, the blue boxes represent the pixels and each intersection include a logic OR gate. The position of each OR gate of the tree is optimized so each segment of wire is respectively matched in length.

Figure 11: H-Tree Structure of the Flag Tree. The route length and delay is matched for each pixel to minimize the skew between the pixels. The tree presented here only contains 64 pixels to simplify the diagram.



7.3.6 Pixel Synchronization

7.3.6.1 Overview

To execute the digital sum on request, a circuit needs to retrieve and store the status of each pixel to feed the digital sum which is combinatorial logic. This status bit for each pixel must remain unchanged as long as the sum is not completed to obtain the proper result. Since each pixel generates a fully asynchronous signal that can trigger at any time, a synchronizer circuit must correctly transfert the pixel status to the synchronous acquisition domain for the digital sum.

Crossing a clock domain (from asynchronous to synchronous) can cause hazardous behaviours (metastability) if special cares are not taken. Because of timing constraints of digital logic (mainly setup and hold constraints), it is impossible to completely remove metastability. However, the mean time between failure (MTBF) can be increased to become negligible compared to the required signal periods.

7.3.6.2 Pixel Synchronizer Modes of Operation

The pixel synchronizer is designed to operate in two different modes of operation, level or edge sensitive. These two modes change the representation of the pixel status bit to use with the sum. This dual mode of operation accommodates the analysis of the received photons on the detector depending on the application.

Important: Both modes are not available at the same time. Only one mode can be selected to feed the digital sum. The user must select the required mode before the acquisition.

The first mode of operation is **level sensitive**. On each acquisition clock cycle, the output of the synchronizer remains high during the totality of the quenching circuit hold-off period. This mode is the digital equivalent of the analog monitor waveform. The result indicates, at the moment of the acquisition, how many pixels are in hold-off. It does not indicate in which acquisition bin the pixels fired. When looking at a single pixel, the complete hold-off cycle can be seen. When looking at the sum of multiple pixels, the pileup tends to blurry the hold-off cycles.

The second mode of operation is **edge sensitive**. On each acquisition clock cycle, the output of the synchronizer goes high when a rising transition of the quenching circuit is detected (from idle to hold-off transition) and remains high for a single clock cycle. The duration of the synchronizer output pulse is then independent to the duration of the hold-off period. If a transition or more are detected at each acquisition clock cycle, the output of the synchronizer can remain high for more than one clock cycle. The purpose of this mode is to count each pixel only once in the time bin it triggered. It indicates, at the moment of the acquisition, how many pixels triggered since the last acquisition. When looking at a single pixel, if considering an acquisition period (e.g. 10 ns) shorter than the hold-off period (e.g. 100 ns), the synchronizer output will never be high for more than one clock cycle since it is impossible to have more than one hold-off cycle during an acquisition clock period. Each output pulse of the synchronizer would then be spaced by a period relative to the hold-off period.

Figures 12, 13 and 14 illustrate different use cases for both level and edge sensitive modes of operation.

Figure 12: Pixel synchronizer modes of operation with continuous clock - Level and Edge sensitive. In level sensitive mode, the output of the pixel synchronizer (LEVEL) follows the output of the quenching circuit (QC) with a latency caused by the acquisition clock. In edge sensitive mode, the output (EDGE) is high for a single clock cycle when the rising edge is detected.

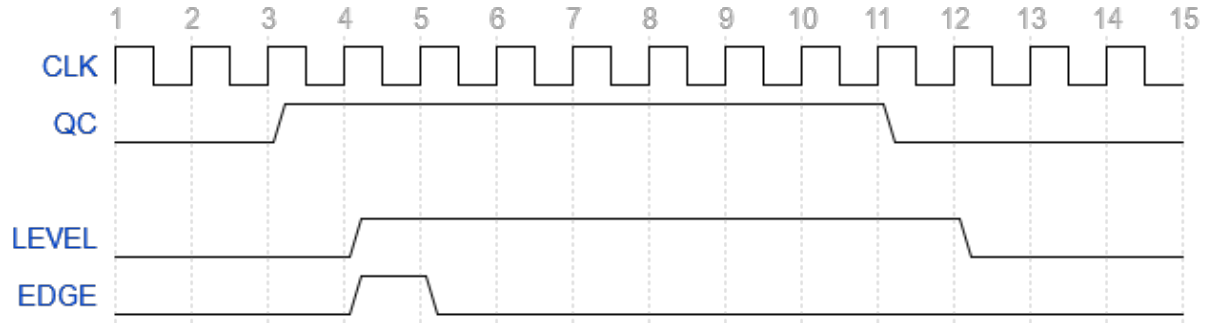


Figure 13: Pixel synchronizer modes of operation with clock gating. A gated clock has an effect similar to using a lower frequency clock. The gated clock can be sent from the Tile Controller or generated internally using the PDC finite state machine acquisition (ACQA Register and ACQB Register).

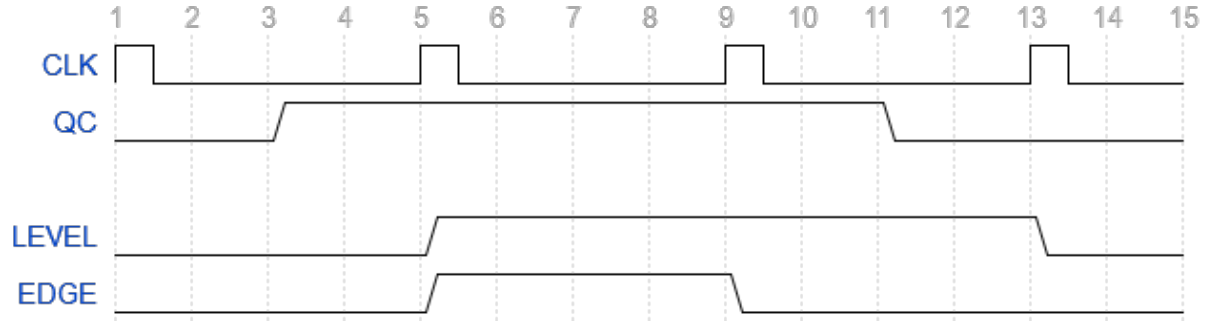


Figure 14: Pixel synchronizer modes of operation with clock gating showing a missed event using level synchronization. If the period of the acquisition clock is larger than the hold-off period, A hit could be missed in level synchronization mode.

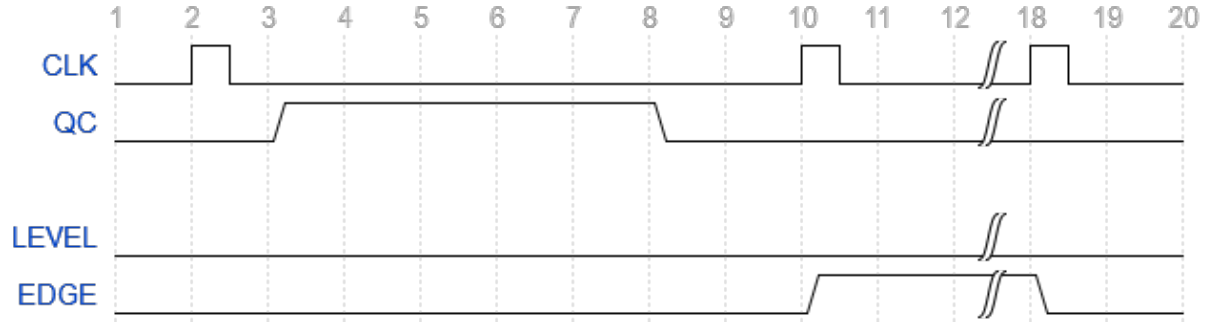
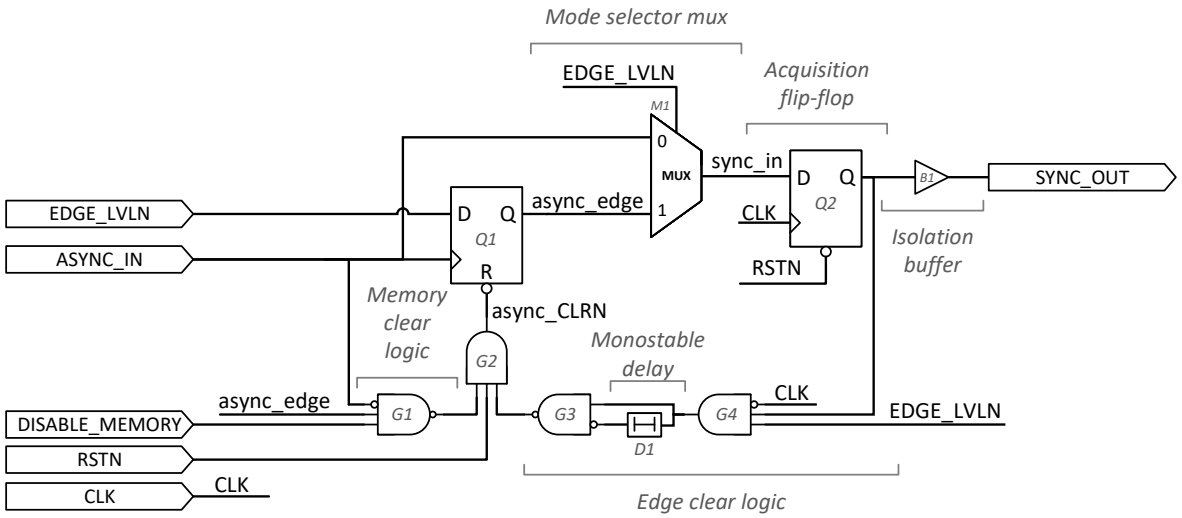


Figure 15: Implementation of the pixel synchronizer circuit. EDGE_LEVELN selects between level and edge sensing. ASYNC_IN is the output of the quenching circuit to synchronize. When DISABLE_MEMORY configuration is active, Q1 memory is reset via G1 at the end of the hold-off period. RSTN is the system reset of the PDC. CLK is the acquisition/synchronization clock. Q1 is used for the edge synchronization only and is bypassed with MUX in level synchronization. Q2 is the synchronization flip-flop. G2, G3, G4 and D1 are used to reset Q1 in edge synchronization with minimum dead time. B1 isolates the synchronizer circuit from the sum logic. The different modes of operation are set up using PIXL Register

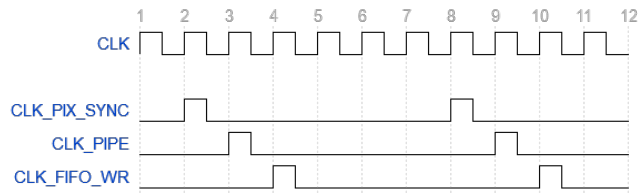


7.3.7 Digital Sum

The digital sum of the PDC looks at the synchronizer output of each pixel and sum how many of them triggered in the acquisition period. Compared to a digital counter that would be triggered by the flag output, the digital sum is able to count multiple pixels that trigger at the same time resulting in a full dynamic range from 0 to 4096 (number of pixels). The logic gates required to implement the digital sum is spread around the analog quenching circuits in the array. To allow the digital sum to be sampled as fast as each 10 ns, a pipeline is required to split the digital sum in two. This means a digital sum can be sampled each 10 ns, but the total time required from the synchronizer to the output of the sum is 20 ns. This allow multiple digital sum acquisitions sampled with a countinuous clock of 10 ns. This architecture is presented on Figure 17.

Figure 16: Chronogram of the acquisition with the different internal clock signals.

(a) Chronogram of an intermittent acquisition. Acquisition clock CLK_PIX_SYNC has a period of six clock cycles. The pipeline clock CLK_PIPE is enabled on the cycle following CLK_PIX_SYNC. The clock to write into the FIFO is active one clock cycle after CLK_PIPE. The result of the sum is hence ready two clock cycles after the CLK_PIX_SYNC cycle. Even if the acquisition period is six clock cycles, the input clock (CLK) period must be no shorter than 10 ns.



(b) Chronogram of a continuous acquisition. Acquisition clock CLK_PIX_SYNC is enabled for seven clock cycles. The pipeline clock CLK_PIPE is also enabled for seven clock cycles but with a delay of one cycle. The clock to write into the FIFO is also delay from one cycle compared to the pipeline clock. The sum can hence be sampled with a 10 ns clock, but the result is stored into the FIFO with a latency of two cycles.

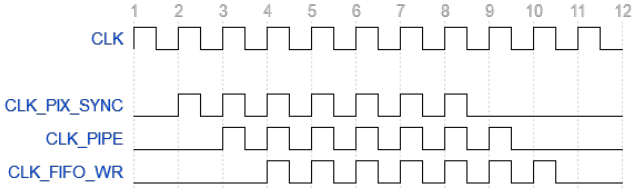
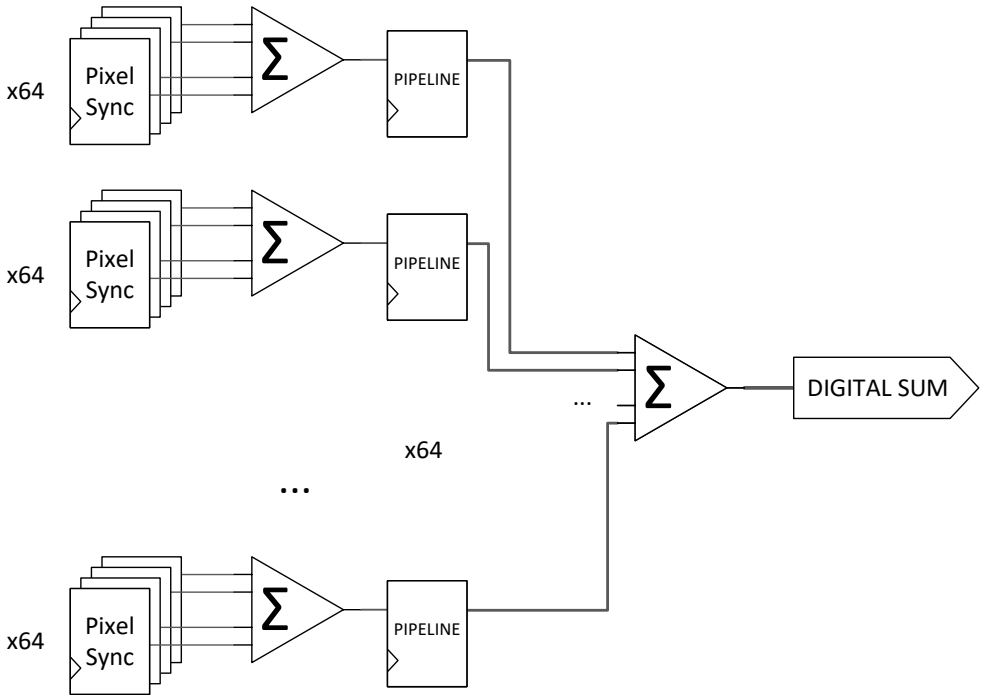


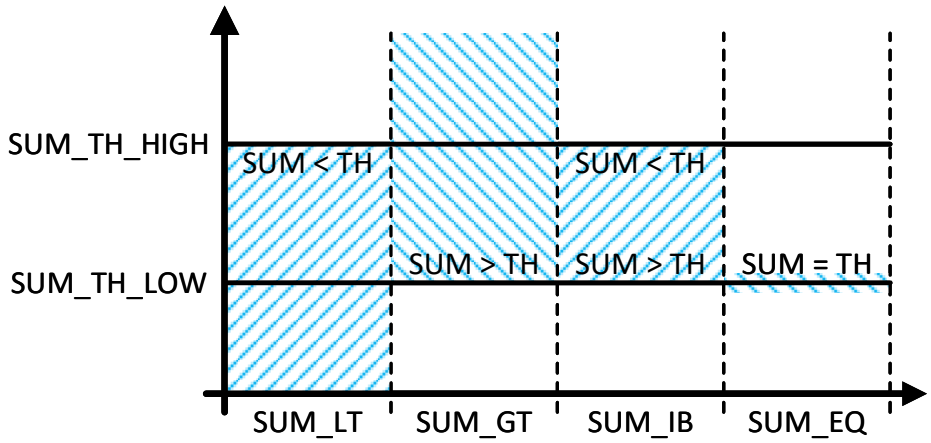
Figure 17: Digital sum and pipeline architecture. 64 pixel synchronizers are first summed together and the intermediate result of 7 bits is stored into a pipeline at each clock cycle. This implementation of intermediate sum and pipeline is replicated 64 times to sum all of the 4096 pixels of the PDC. Then, the final step of the sum takes all the intermediate results stored into each pipeline to generate the digital sum result on 13 bits.



7.3.8 Digital Sum Comparator

For some applications, it might be required to get an idea of the result of the digital sum without having to transmit it. By using the flag output, one can only know if one or more pixels triggered at the same time, but not how many. The digital sum is then required to get the exact number of pixels. To get the result, the sum must be sampled and the result must be transmitted. To save on transmission time, the two reconfigurable outputs (DATA, FLAG) can be reprogrammed (OUTD Register and OUTF Register) to use the digital sum comparator. By setting the thresholds and enabling the feature (STHH Register and STHL Register), up to 4 functions are available : SUM_LT, SUM_GT, SUM_IB and SUM_EQ. The relations are explained on Figure 18.

Figure 18: Digital sum comparator - Comparator output relations to thresholds. SUM_LT rises when sum result is less than SUM_TH_HIGH. SUM_GT rises when sum result is greater than SUM_TH_LOW. SUM_IB rises when sum result is in between SUM_TH_LOW and SUM_TH_HIGH. SUM_EQ rises when sum result is equal to SUM_TH_LOW.



7.3.9 Debug Binary Counter

To test data transmission without the need to bias the SPADs, an internal debug counter can be enabled to generate data. The data can then be used as an input source to the PDC FIFO or directly to the data transmitter. When enabled, the counter is increased at each CLK input cycle while the PDC is in acquisition mode. When disabled, the counter is clock gated and does not consume power at every clock transition. The depth of the counter is 13 bits to match the result of the digital sum.

7.3.10 FIFO

Since the data going out of the PDC is serialized using the input clock frequency (see Data Serializer at 7.3.11), most of the time, the acquisition occurs faster than the data transmission. Hence, the PDC dispose of an internal FIFO memory (First In First Out) to store up to 128 digital sum results. To each sum result, one extra bit is required to indicate if the sum is acquired directly from each CLK input cycle (external) or if it is triggered using the PDC internal finite state machine to acquire a digital sum each N clock cycles. Each word of the FIFO is then 14 bits. The FIFO Register sets up how the FIFO operates. First, the FIFO must be enabled to operate. Then the input source must be selected. The default setting stores the results of the digital sum into the FIFO, but two other debug options are available to store into the FIFO : the debug counter and the debug register.

During the external acquisition, the FIFO is normally in overwrite mode. The FIFO contains an adjustable buffer which will then start to overwrite the oldest data when this adjustable buffer is full. If this behaviour is not required, it can be disabled so the FIFO remains full without any overwrite. The overwriting behaviour can be useful for continuous acquisitions where an history of the digital sum before a given trigger. The adjustable depth of the buffer from 1 to 128 is also set by the FIFO Register.

7.3.11 Data Serializer

To reduce the number of required outputs in a system with a large number of PDCs, the results of the digital sum are sent on a serial link. As defined in 7.8, the data transmission requires 18 bits to transmit the result of a digital sum. This includes a start and a stop bit for flow control, 2 CRC bits to detect errors in transmission, 1 bit to indicate if the acquisition was external or internal, 1 overflow bit and 12 bits of data. A packet formed of 18 bits conserves the full dynamic range of the PDC of 4096 pixels per sum. In some applications, this full dynamic range might not be required. For example, even if all the 4096 pixels are enabled, the events to observe may not trigger more than 100 pixels in a single bin. In that case, the user could reduce the number of bits to 12 to transmit the result of the digital sum. This results in less power consumed and less time required to transmit all the data. In case the result of the sum is larger than what can be represented with the configured number of bits, the overflow bit is set. The user can then change the setting of the number of bits or can accept this saturation in the triggered pixel count.

7.3.12 Output Multiplexer

The number of outputs of the PDC is optimized to ease the integration in large scale system. For this reason, apart from the configuration bus, only two outputs are available. Since more than two signals can be required to operate the system, each output has multiple functions that can be selected. The advantage over dedicated debug outputs is that the two outputs already need to be routed in a system. These outputs main function are respectively FLAG and DATA. The different functions are listed in Table 43. A given output can be configure to always keep the same function, or can change dynamically depending on the task executed by the PDC. For example, during the acquisition, the DATA output could be used as a digital sum comparator output. Then during the data transmission, the DATA pin returns to its default DATA function. Finally during the configuration mode of the PDC, DATA and FLAG outputs can be configured as handshake signal to validate the configurations are executed properly. The associated registers are OUTD Register for DATA output, OUTF Register for FLAG output and OUTC Register for both DATA and FLAG during configuration mode.

7.3.13 Trigger Generator and Trigger Tree

To test the PDC without having to bias the SPAD, an external signal can be routed to each quenching circuit to trigger it. As shown in the quenching circuit descriptions (7.3.2), the trigger can be configured to impact the reading node before the discriminating element (FE_TRG) or to impact only the digital circuits (DGTL_TRG) using the PIXL Register. The trigger signal itself can be generated in two different ways, a signal or a command.

If the trigger signal is required without any acquisition on the PDC, for example to measure the flag tree timing, the PDC can be placed in trigger mode with a command. In trigger mode, the CLK input of the PDC no long serves as a clock input, but directly feeds the trigger tree to all the enabled pixels. Any sequence of trigger can then be applied to the PDC.

To trigger the PDC to test the acquisition, since the CLK input is required, the trigger command can be used. The PDC must be in acquisition mode to operate normally. Using the CFG_CLK and CFG_DATA link, a trigger can be sent using a command. The duration of this internally generated trigger pulse can be programmed from 1 to 128 CFG_CLK cycles using the TRGC Register. If the period TRG_TON is larger than 1, the user must ensure to send enough CFG_CLK cycles to prevent the PDC to remain on a triggered state. With the FE_TRG, this would force the quenching circuit to trigger continuously.

Recommendation: Even if the PDC can support all its pixels triggering at the exact same time, it is not recommended. This results in the maximum peak currents associated with the quenching circuit.

7.3.14 Configuration and Commands Receiver

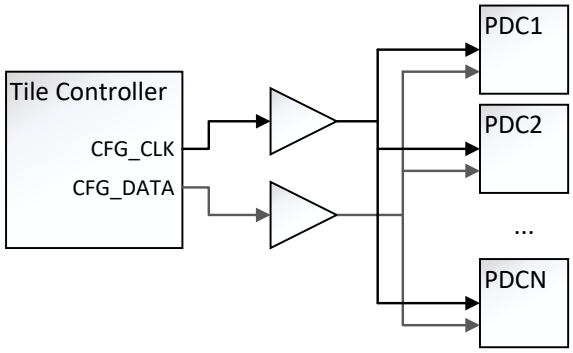
The PDC provide a dedicated interface for configurations and commands (CFG_CLK, CFG_DATA, CFG_CLK_RTN, CFG_DATA_RTN and CFG_RTN_EN). An external device (Tile Controller or FPGA) must send a configuration clock (CFG_CLK) and the appropriate synchronized data (CFG_DATA) in order to use this communication link. A command (Commands) requires 8 bits to transmit and a configuration (Configuration) is 32 bits. A command can be receive at any time by the PDC. To send a configuration, the PDC must first be put in configuration mode with the configuration mode command (Command identification). While in configuration mode, the CLK input of the PDC becomes a chip select to indicate if the configuration applies to a given PDC (if systems with multiple PDCs). Once the configuration phase is complete, the PDC must be returned to acquisition mode for normal operation.

7.3.15 Configuration and Commands Daisy Chain

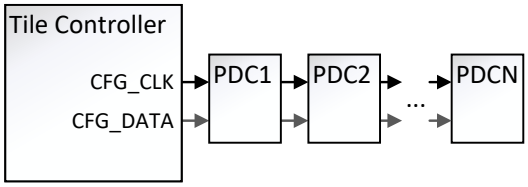
Multiple PDCs can be configured or receive commands from the same configuration interface. This helps reducing the number of inputs/outputs required at the Tile Controller. Since the CLK input of the PDC becomes a chip select during configuration mode, the same configuration data can be sent to multiple PDCs, but be addressed to a single PDC.
From a single CFG_CLK and CFG_DATA from the Tile Controller, one could use a fanout buffer towards each PDC (Figure 19a), but this leads to more component on the tile. Another approach is to use the PDC embedded configuration and command daisy chain (CFG_CLK_RTN, CFG_DATA_RTN, CFG_RTN_EN). The configuration interface from the tile controller is routed to a first PDC, then buffed by the first PDC to a second PDC and so on. To use the daisy chain, CFG_RTN_EN must be tied high to enable the return pins (CFG_CLK_RTN and CFG_DATA_RTN). The output of the daisy chain is a buffed version of its input. This means no clock period delay adds up at each PDC, only propagation delay of the wires and the buffers.

Figure 19: Configuration and Commands Interface Routing.

(a) Fanout Buffer.



(b) Daisy Chain.

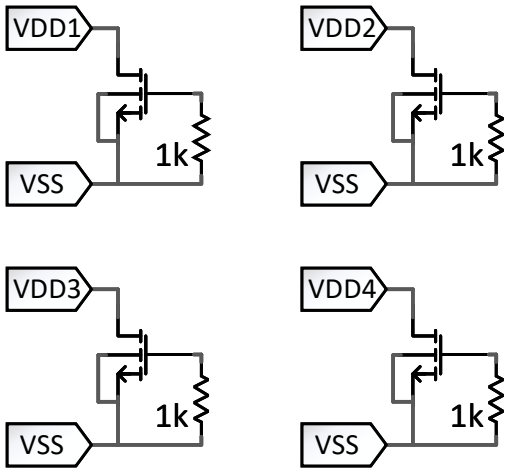


7.3.16 PDC ESD Protections

Each pad of the PDC is protected with ESD structures respecting TSMC 180nm BCD rules. Each VSS pad has a transistor connected as a clamp diode toward each of the VDD supplies (VDD_CORE, VDD_IO, VDD_FE and VDD_AM) as shown in Figure 20a. Each VDD pad as a clamp to VSS (Figure 20b). The Analog Monitor output is protected via two transistors connected as diodes, one in direct from Analog Monitor to VDD_AM and the other in direct from VSS to Analog Monitor (Figure 21a). The digital outputs are protected using a chain of digital buffers of increasing size where the last one is large enough to offer a proper protection (Figure 21b). For the digital inputs, the basic ESD protection scheme is illustrated at Figure 22a. MP1 and MP2 transistors are the primary protections. MS1 and MS2 form the secondary protection which are smaller in size. Primary and secondary protections are separated with a 300 Ohm resistor. VDD_CORE is used for the digital inputs as VDD ESD rail. For some inputs, a pull-up (Figure 22b) or a pull-down (Figure 22c) is included to set a default value without requiring an external wirebond. The impedance of the pull transistor (MT1) is defined in section 6.4.

Figure 20: Supply Pad ESD Protection.

(a) VSS Pad ESD Protection.



(b) VDD Pad ESD Protection.

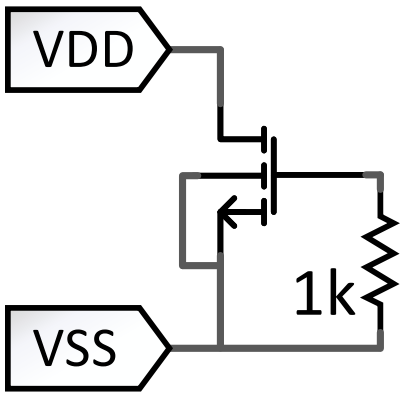
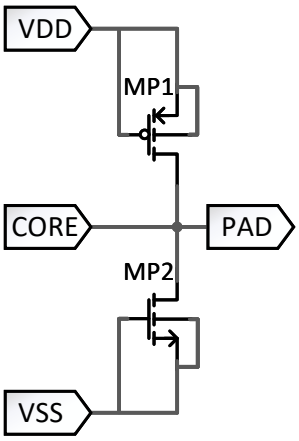


Figure 21: Output ESD Protection.

(a) Analog Output.



(b) Digital Output.

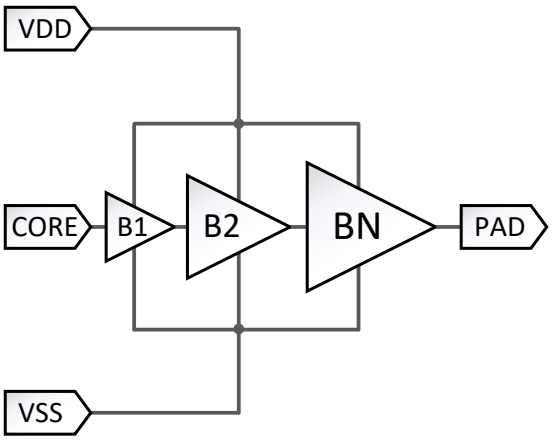
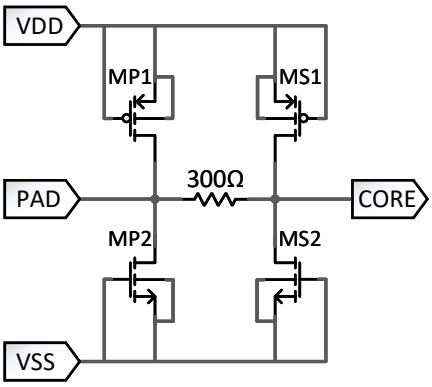
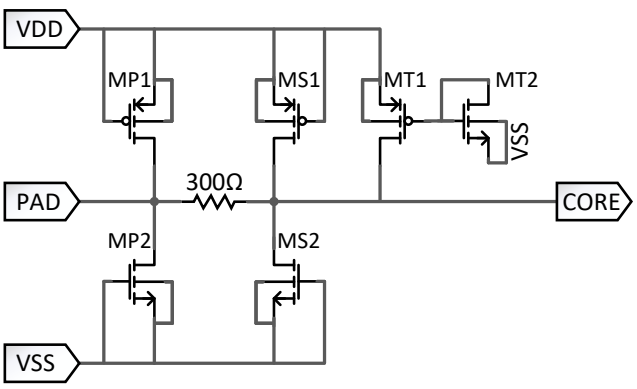


Figure 22: Input Pad ESD Protection.

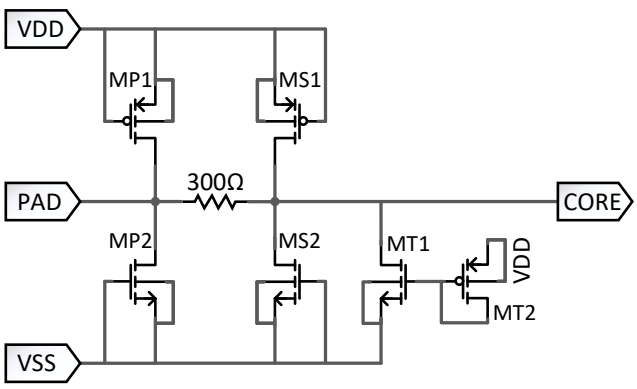
(a) Input.



(b) Input with Pull-Up.



(c) Input with Pull-Down.



7.3.17 Power-up and Power-down Sequence Control

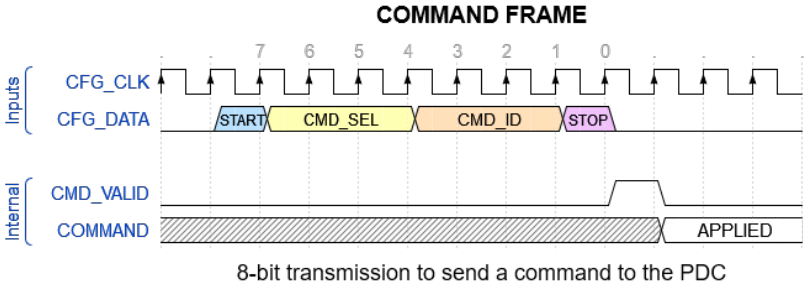
The recommended power-up sequence is VDD_CORE, VDD_IO, VDD_FE, VDD_AM and HV to ensure the proper operation of the PDC. The required power-off sequence is the reverse of the power-up sequence: HV, VDD_AM, VDD_FE, VDD_IO and VDD_CORE.

In addition, when no supply is present on the PDC, all PDC inputs (CFG_RTN_EN, CFG_DATA, CFG_CLK, CLK, POR_DIS and RSTN) should be set to 0 V. Due to the ESD protections, an input set to 1.8 V will pass through the protection diode directly to VDD_CORE and supply the PDC. **It can result in damage of the PDC or the device connected to it (FPGA or Controller).**

7.4 Device Functional Modes

7.5 Commands

Figure 23: Chronogram of the required signals to send a command to the PDC with the 8-bit sequence



Based on the Table 7, a valid command frame must meet following conditions:

- START 1 bit to start the command with a value of 1 [7].
- CMD_SEL 3 bits to select between a command or a configuration [6:4].
- CMD_ID 3 bits to identify the command to apply [3:1].
- STOP 1 bit to stop data transmission with a value of 0 [0].

Table 7: Description of the frame to send a command to the PDC

FAST COMMAND PROTOCOL							
START_BIT	CMD_SEL			CMD_ID			STOP_BIT
	2	1	0	2	1	0	
MSB	6	5	4	3	2	1	LSB

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
START_BIT (1)	Transmission always begins with START BIT	1
CMD_SEL (3)	Select between configuration (32 bits) frame or fast command (8 bits)	
	Value **Name** **Size** **Description**	
	0 MODE 8 Modes of operation of the PDC	0 0 0
	1 GCMD 8 General command of the PDC	0 0 1
	2 DACQ 8 Acquisition of the PDC	0 1 0
	3 ODTX 8 Data transmission of the PDC	0 1 1
	4 PIXR 32 Pixel enable registers of the PDC	1 0 0
	5 PIXC 32 Pixel command registers of the PDC	1 0 1
	6 CREG 32 Configuration registers of the PDC	1 1 0
	7 UNSD 0 Unused command select	1 1 1
CMD_ID (3)	Identification of the command to execute The description of the addresses is available in Table 9.	
STOP_BIT (1)	Transmission always end with STOP BIT	0

7.6 Configuration

The PDC (ICWSHLP2 v2.0) uses a serial communication synchronous to the configuration clock (CFG_CLK) to be programmed. Since both command and configurations can be sent via CFG_DATA, the PDC must first be placed in configuration mode by sending the appropriate command. In configuration mode, the CLK input of the PDC acts as a chip select (CS). Only PDCs with active CS will be configured. The configuration CS must be sent for at least 2 clock cycles before begin to transmit any configuration frame. Then, while CFG_CLK is being sent to the PDC, the transmission of the configuration frame starts with the start bit. The configuration data input (CFG_DATA) data format consists of a 32-bit word with the most significant bit (MSB) sent first. If the PDC is daisy chained and enabled (CFG_RTN_EN), CFG_CLK and CFG_DATA will be transmitted by the return outputs (CFG_CLK_RTN and CFG_DATA_RTN). The chronogram of Figure 24 shows these signals with the order of the bits to transmit.

Based on the Table 10, a valid configuration frame must meet following conditions:

- START 1 bit to start the command with a value of 1 [31].
- CMD_SEL 3 bits to select between a command or a configuration [30:28].
- ADDRESS 8 bits to define the address of the register to program [27:20].
- REGISTER 16 bits to set the new content of the configuration register [19:4].
- CRC 3 bits to match the content of the frame (excluding start and stop bits) [3:1].
- STOP 1 bit to stop data transmission with a value of 0 [0].

Table 9: Command identification (CMD_ID)

COMMAND IDENTIFICATION					
CMD_SEL	**COMMAND NAME**	**CODE (CMD_ID)**	**DESCRIPTION**	**CLOCK DOMAIN**	**ASSOCIATED REGISTER**
PDC Operation Mode (MODE) - CMD_SEL = 0b000					
MODE	ACQ	b001	CLK input is used to control the data acquisition and transmission. No configuration possible. Only fast commands are available.	CLK	PIXL, TIME, ANLG, STHH, STHL, ACQA, ACQB, DBGC, FIFO, DTXC, OUTD, OUTF
MODE	TRG	b010	CLK input is used to trigger the pixels. Data acquisition and transmission functions are disabled. No configuration possible. Only fast commands are available.	Asynchronous	TRGC
MODE	CFG	b011	CLK input is used as a chip select for the configuration. Data acquisition and transmission functions are disabled. To exit configuration mode, return to ACQ or TRG modes.	CFG_CLK	ALL
PDC General Commands (GCMD) - CMD_SEL = 0b001					
GCMD	RSTN_SYS	b001	Reset of the PDC systems only. Configuration registers are unchanged. Reset affects finite internal state machines (FSM), pixel synchronizers, adder, FIFO and transmitter.	CLK	NONE
GCMD	RSTN_CFG	b010	Reset of the configuration registers only. Finite State Machines (FSM), Pixel synchronizers, adder, FIFO and transmitter are unchanged	CFG_CLK	ALL
GCMD	RSTN_FULL	b011	Full reset of the PDC systems and configuration registers.	CLK/CFG_CLK	ALL
GCMD	TRG	b100	Executes a software trigger. Trigger duration is set by the trigger register. CFG_CLK must remain active to generate a trigger with a duration longer than 1 cycle.	CFG_CLK	TRGC
PDC Data Acquisition Commands (DACQ) - CMD_SEL = 0b010					
DACQ	ACQ	b001	Each CLK cycle triggers an acquisition. This is referred as an external acquisition. No data transmission occurs.	CLK	NONE
DACQ	AATXF	b010	Start intermittent acquisition with Bank A settings. A sum is acquired at each N CLK cycles for M samples. Transmission of DATA from the FIFO will occur during the acquisition.	CLK	ACQA
DACQ	ABTXF	b100	Start intermittent acquisition with Bank B settings. A sum is acquired at each N CLK cycles for M samples. Transmission of DATA from the FIFO will occur during the acquisition.	CLK	ACQB
PDC Data Transmission Commands (ODTX) - CMD_SEL = 0b011					
ODTX	FIFO	b000	Transmit the content of the FIFO until it is empty.	CLK	FIFO, DTXC, OUTD, OUTF
ODTX	DSUM	b001	Transmit a single digital sum without using the FIFO.	CLK	DTXC, OUTD, OUTF
ODTX	DBGC	b010	Transmit a single sample of the debug counter.	CLK	DBGC, DTXC, OUTD, OUTF
ODTX	DBGR	b011	Transmit a single sample of the debug register.	CLK	DBGC, DTXC, OUTD, OUTF
ODTX	ASID	b111	Transmit a single sample of the ASIC ID.	CLK	DTXC, OUTD, OUTF

Figure 24: Chronogram of the required signals to program the PDC with the 32-bit sequence

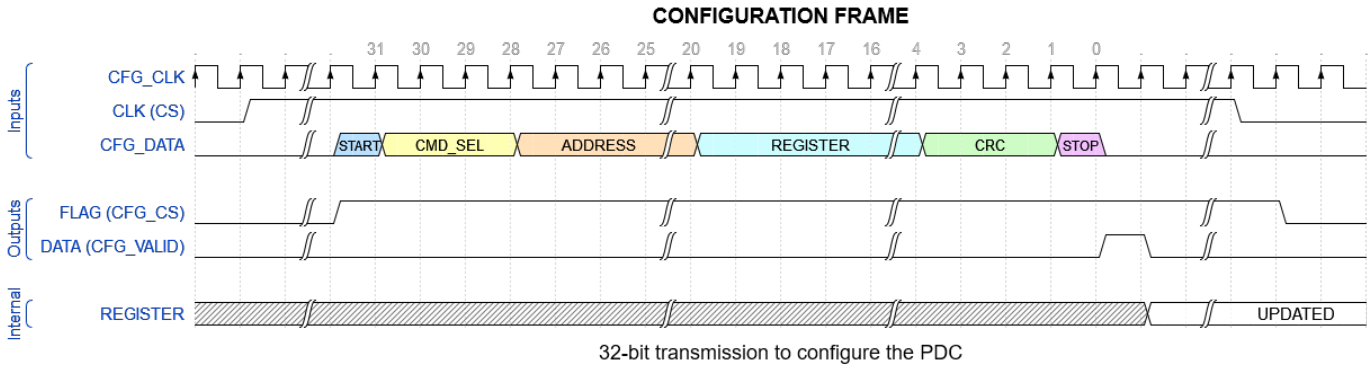


Table 10: Description of the frame to configure the PDC

CONFIGURATION REGISTER TRANSMISSION PROTOCOL																																
START_BIT	CMD_SEL			ADDRESS								REGISTER																CRC			STOP_BIT
	2	1	0	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	2	1	0	
MSB	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
START_BIT (1)	Transmission always begins with START BIT	1
CMD_SEL (3)	Select between configuration (32 bits) frame or fast command (8 bits) **Value** **Name** **Size** **Description** 0 MODE 8 Modes of operation of the PDC 1 GCMD 8 General command of the PDC 2 DACQ 8 Acquisition of the PDC 3 ODTX 8 Data transmission of the PDC 4 PIXR 32 Pixel enable registers of the PDC 5 PIXC 32 Pixel command registers of the PDC 6 CREG 32 Configuration registers of the PDC 7 UNSD 0 Unused command select	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1
ADDRESS (8)	Address of the register to configure with the REGISTER bits The description of the addresses is available in Table 12.	
REGISTER (16)	Content of the register to configure The description of the register is available in Subsection 7.7 Register Map.	
CRC (3)	Checksum to validate the reception of the configuration START and STOP bits are not considered in the calculation of the CRC Polynomial used is 3b011 with implicit first bit (4b1011)	0 1 1
STOP_BIT (1)	Transmission always end with STOP BIT	0

7.7 Register Map

Most of the register addresses of the PDC are used to enable or disable each pixel. Since there are 4096 pixels and each configuration register is 16 bits, this leads to 256 registers required. These registers are selected using the CMD_SEL bits 0b100 in the configuration frame with addresses from 0 to 255. The pixel command registers (CMD_SEL bits 0b101) are not physical registers, but are used to execute operations on pixel enable. Finally, The device configuration registers are selected using CMD_SEL bits 0b110. They set the operating mode of the PDC. These different addresses are shown in Table 12.

7.7.1 PIXR Registers

Table 12: Register Addresses

ADDRESSES OF THE CONFIGURATION REGISTER					
ADDRESS			REGISTER NAME	NOTE1	NOTE2
dec	hex	bin			
PIXEL ENABLE REGISTERS (PIXR) - CMD_SEL = 0b100					
0	0x00	b0000 0000	REG_PIX_ENABLE_0	Pixels 0 to 15	Register row 0, column 0
1	0x01	b0000 0001	REG_PIX_ENABLE_1	Pixels 16 to 31	Register row 0, column 1
2	0x02	b0000 0010	REG_PIX_ENABLE_2	Pixels 32 to 47	Register row 0, column 2
3	0x03	b0000 0011	REG_PIX_ENABLE_3	Pixels 48 to 63	Register row 0, column 3
...	...	...	...	...	
252	0xFC	b1111 1100	REG_PIX_ENABLE_252	Pixels 4032 to 4047	Register row 15, column 12
253	0xFD	b1111 1101	REG_PIX_ENABLE_253	Pixels 4048 to 4063	Register row 15, column 13
254	0xFE	b1111 1110	REG_PIX_ENABLE_254	Pixels 4064 to 4079	Register row 15, column 14
255	0xFF	b1111 1111	REG_PIX_ENABLE_255	Pixels 4080 to 4095	Register row 15, column 15
PIXEL COMMAND REGISTERS (PIXC) - CMD_SEL = 1b101					
64	0x40	b0100 0000	REG_PIXC_16	Pixels 0 to 255	Array is split into 16 sections.
DEVICE CONFIGURATION REGISTERS (CREG) - CMD_SEL = 1b110					
0	0x00	b0000 0000	RSVD	Reserved address	No register associated with address 0
1	0x01	b0000 0001	PIXL	Pixels control register	Sets the operation of the pixels
2	0x02	b0000 0010	TIME	Monostable time register	Sets the duration of the monostables
3	0x03	b0000 0011	ANLG	Analog control register	Sets the amplitude of the analog monitor
4	0x04	b0000 0100	STHH	Sum high threshold register	Sets the higher threshold for sum comparisons
5	0x05	b0000 0101	STHL	Sum low threshold register	Sets the lower threshold for sum comparisons
6	0x06	b0000 0110	ACQA	Acquisition control register A	Sets the bank A acquisition of the PDC
7	0x07	b0000 0111	ACQB	Acquisition control register B	Sets the bank B acquisition of the PDC
8	0x08	b0000 1000	DBGC	Debug control register	Sets the debug features of the PDC
9	0x09	b0000 1001	FIFO	FIFO control register	Sets the parameters of the PDC FIFO
10	0x0A	b0000 1010	DTXC	Data transmit control register	Sets the parameters of the data transmission
11	0x0B	b0000 1011	OUTD	DATA output control register	Sets the signal on DATA output pin
12	0x0C	b0000 1100	OUTF	FLAG output control register	Sets the signal on FLAG output pin
13	0x0D	b0000 1101	OUTC	CFG output control register	Sets the signal on DATA and FLAG output pins
14	0x0E	b0000 1110	TRGC	Trigger control register	Sets the parameters of the PDC internal trigger

Refer to Figure 25 for the physical position of each pixel enable register in the PDC.

Table 13: PIXR Registers Definition

PIXR Registers - 0 to 255 (0x00 to 0xFF)															
PIX_EN	PIX_EN	PIX_EN	PIX_EN	PIX_EN	PIX_EN	PIX_EN	PIX_EN	PIX_EN	PIX_EN	PIX_EN	PIX_EN	PIX_EN	PIX_EN	PIX_EN	PIX_EN
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEFAULT VALUE															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HEX	DEC
0x0000	0

Figure 25: Position of the pixel enable registers in the array. The pixel enable register addresses are represented in black and the bits of the pixel enable command are in blue. The register address 0 is at the lower left of the PDC near the wirebonding IO Pads. The register address 255 is at the upper right near the 2D CMOS SPADs. Each bit of the pixel enable command regroups 16 addresses for a total of 256 pixels.

2D CMOS SPADs

240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

12 13 14 15 8 9 10 11 4 5 6 7 0 1 2 3

Wire bonding pads

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
PIX_EN (1)	1 bit to enable a pixel of the PDC.	
	All pixels are disabled by default and must be enabled to operate the PDC.	0
	When PIX_EN=0, the associated pixel is disabled.	0
	When PIX_EN=1, the associated pixel is enabled.	1
	The 16 pixels within a register are placed in a 4×4 fashion as shown below. When looking at the PDC from above with the pad ring at the bottom, pixels 0 to 3 are closest to the pad ring. The position of each address is shown in Figure 25.	
	upper left: 12 13 14 15 (upper right); 8 9 10 11; 4 5 6 7; lower left: 0 1 2 3 (lower right). Towards the pad ring	

7.7.2 PIXC Register

Table 15: PIXC Command Definition

PIXC Command Register															
GRP_EN	GRP_EN	GRP_EN	GRP_EN	GRP_EN	GRP_EN	GRP_EN	GRP_EN	GRP_EN	GRP_EN	GRP_EN	GRP_EN	GRP_EN	GRP_EN	GRP_EN	GRP_EN
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
GRP_EN (1)	1 bit to enable a group of pixel of the PDC.	
	All pixels are disabled by default and must be enabled to operate the PDC.	0
	When GRP_EN=0, the 256 associated pixels are disabled.	0
	When GRP_EN=1, the 256 associated pixels are enabled.	1
	The 4096 pixels of the PDC are splitter into 16 bits in a 4×4 fashion as shown below. When looking at the PDC from above with the pad ring at the bottom, groups 0 to 3 are closest to the pad ring. The position of each address is shown in Figure 25.	
	upper left: 12 13 14 15 (upper right); 8 9 10 11; 4 5 6 7; lower left: 0 1 2 3 (lower right). Towards the pad ring	

7.7.3 PIXL Register

Table 17: PIXL Register Definition

PIXL Register - 1 (0x01)															
DGTL								FE/QC							
SYNC				FLAG				TRG				QC			
UNUSED		DIS_MEM	EDGE_LVLN	UNUSED			FLAG_EN	UNUSED			TRG_DGTL_FEN	UNUSED		ACTIVE_QC_EN	UNUSED
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEFAULT VALUE															
0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0

HEX	DEC
0x1100	4352

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
DIS_MEM (1)	Bit to disable the memory of each pixel synchronizer. Enabled by default (DIS_MEM = 0), each pixel has a 1 bit memory that sets when the pixel triggers. The memory is reset when the pixel is read by the digital sum during an acquisition. When the memory is disabled (DIS_MEM = 1), the memory is reset at the end of the hold-off period of the pixel. This is useful when the hold-off is long enough to ensure that an acquisition will occur to read the pixel before the end of the hold-off period. In the case of a pixel triggered by a dark count, if the pixel is not read by an acquisition before the end of the hold-off period, then the memory resets itself at the end of the hold-off period.	
EDGE_LVLN (1)	Bit to select the type of acquisition of the pixel synchronizer. Each pixel of the PDC has its own synchronizer with the purpose of transfering the asynchronous output of the pixel to the synchronous domain of the acquisition clock. The two available types of acquisition are level synchronization (EDGE_LVLN = 0) and edge synchronization (EDGE_LVLN = 1). Only one type of acquisition can be executed at a time. The level synchronization is level sensitive and the output of the synchronizer remains high during the hold-off period. The edge synchronization is edge sensitive and the output of the synchronizer remains high for a single clock cycle. This type of acquisition is used to count when the pixel triggered.	
FLAG_EN (1)	Bit to enable or disable the flag from each pixel. To reduce digital activity when using the PDC in analog mode only, the flag output of the pixels can be disabled.	
TRG_DGTL_FEN (1)	Bit to select the trigger tree operation between digital only or front-end. When the PDC is in trigger mode (TRG_MODE) or with the trigger command, two triggering options are available. The first (TRG_DGTL_FEN = 1) is a digital trigger which does no interact with the front-end of the pixels. It will not trigger the analog monitor output, but only the input of the digital sum and the flag. The second option (TRG_DGTL_FEN = 0) triggers the front-end. The signal passes through the discriminating element (an inverter) and trigger the complete quenching circuit state machine.	
ACTIVE_QC_EN (1)	Bit to enable or disable the active quenching of the SPADs. In its default configuration (ACTIVE_QC_EN = 0), the quenching circuit is passive, which means there is no feedback on the reading node (the discriminating element input). Each SPAD is quenched via the high impedance of the quenching transistor. When the active quench functionality is enabled (ACTIVE_QC_EN = 1), a feedback from the output of the discriminating element forces the reading node to quench the SPAD faster and hold the reading node in the quenched state.	

7.7.4 TIME Register

Table 19: TIME Register Definition

TIME Register - 2 (0x02)															
FLAG_TIME					RECH_TIME					HOLD_TIME					
										COARSE		FINE			
4	3	2	1	0	4	3	2	1	0	1	0	3	2	1	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEFAULT VALUE															
1	**1**	**0**	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**0**

HEX	DEC
0xDEDE	**57054**

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
FLAG_TIME (5)	5 bits to adjust the pulse duration of the flag A shorter pulse duration will reduce the number of missed hits on the FLAG A longer pulse will ensure the FLAG will propagate through long wires to the tile controller The adjustment of these bits gives a *linear* time adjustment The shortest pulse duration is achieved by filling the registers with ones Any value in between is acceptable The longest pulse duration is achieved by filing the register with zeros Figure 28 shows the mapping between the register value and the duration	1 1 1 1 1 ... 0 0 0 0 0
RECH_TIME (5)	5 bits to adjust the duration of the recharge A shorter recharge will reduce blind time at the end of the hold-off period A longer recharge will ensure the SPAD is fully recharged and ready The adjustment of these bits gives a *linear* time adjustment The shortest recharge duration is achieved by filling the registers with ones Any value in between is acceptable The longest recharge time is achieved by filing the register with zeros Figure 27 shows the mapping between the register value and the duration	1 1 1 1 1 ... 0 0 0 0 0
HOLD_TIME COARSE (2)	2 bits to coarsely adjust the duration of the hold-off A shorter hold-off time will reduce blind time of the SPAD A longer hold-off time will reduce the afterpulse on the SPAD Default hold-off time is long enough to decrease RMS recharge current The adjustment of these bits gives a *non-linear* time adjustment The shortest time range is achieved by any of these two combinations : The intermediate time range is achived by 01 The longest time range is achived by filing the register with zeros Figure 26 shows the mapping between the register value and the duration	1 1 1 0 0 1 0 0
HOLD_TIME FINE (4)	4 bits to finely adjust the duration of the hold-off A shorter hold-off time will reduce blind time of the SPAD A longer hold-off time will reduce the afterpulse on the SPAD Default hold-off time is long enough to decrease RMS recharge current The adjustment of these bits gives a _*linear* time adjustment The shortest pulse length is achieved by filling the registers with ones Any value in between is acceptable The longest time range is achieved by filing the register with zeros Figure 26 shows the mapping between the register value and the duration	1 1 1 1 ... 0 0 0 0

Figure 26: Hold-off monostable duration as a function of the register code

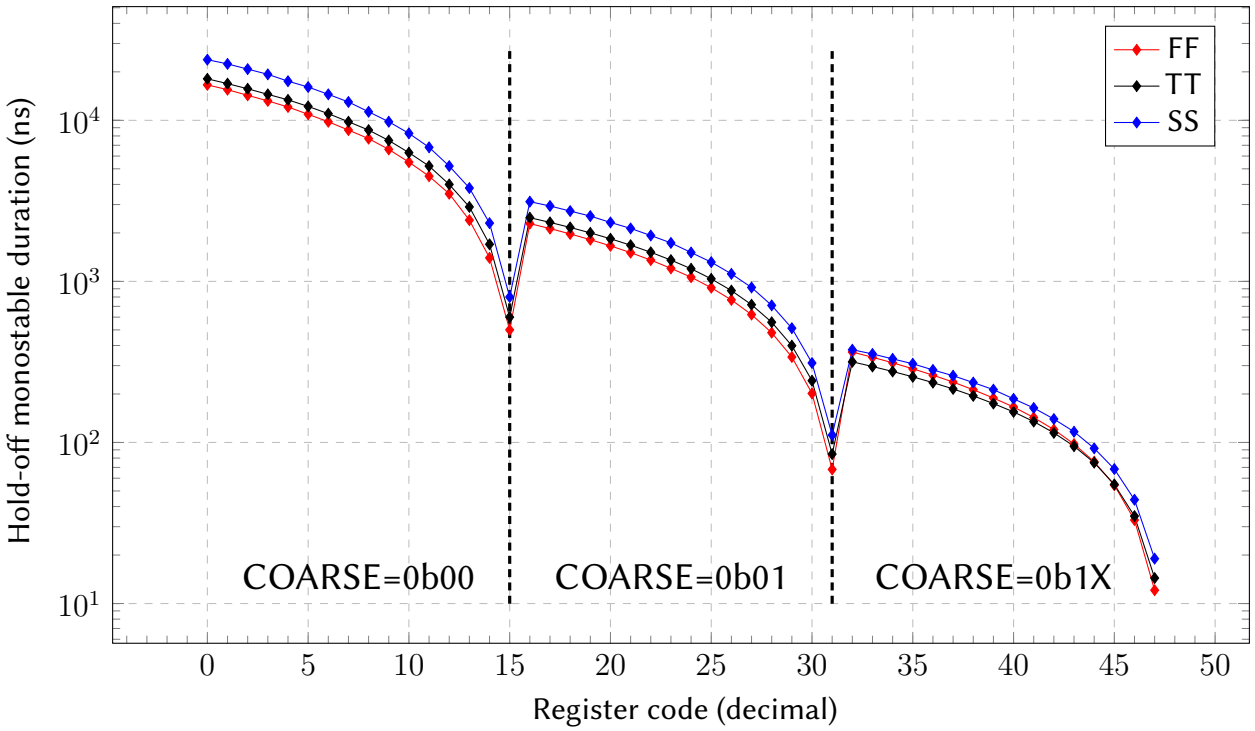


Figure 27: Recharge monostable duration as a function of the register code

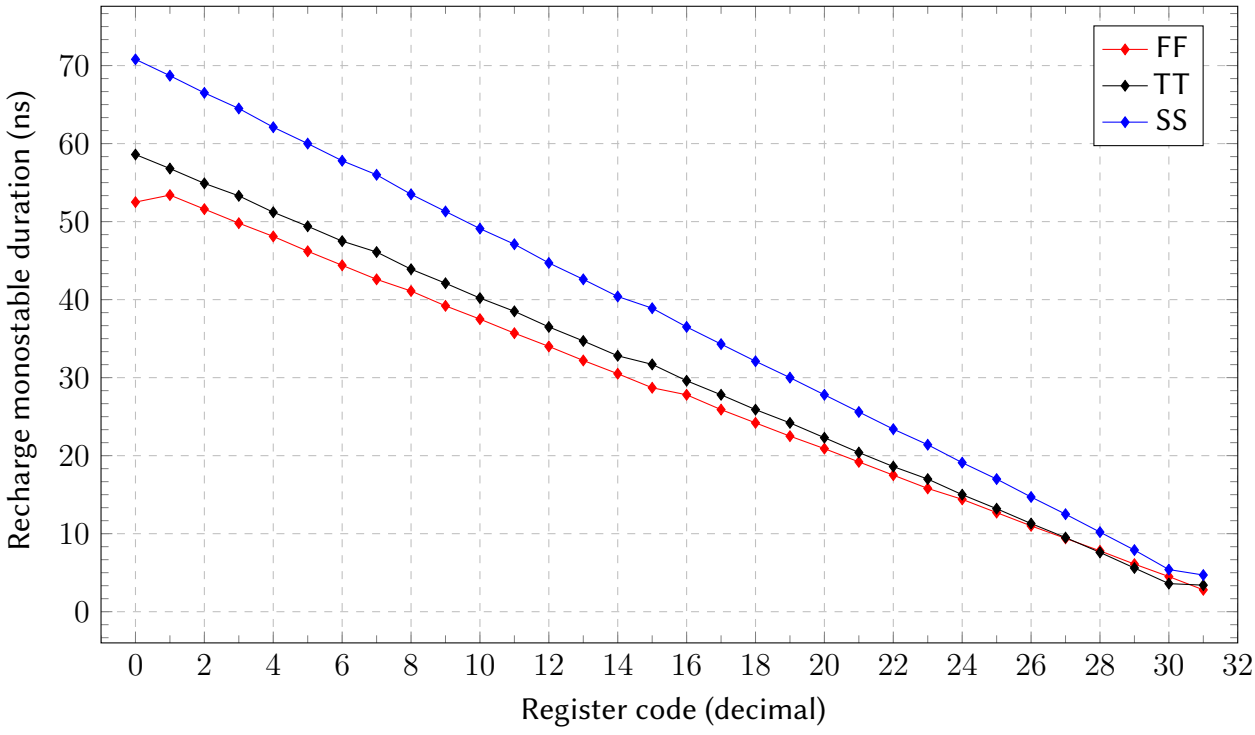
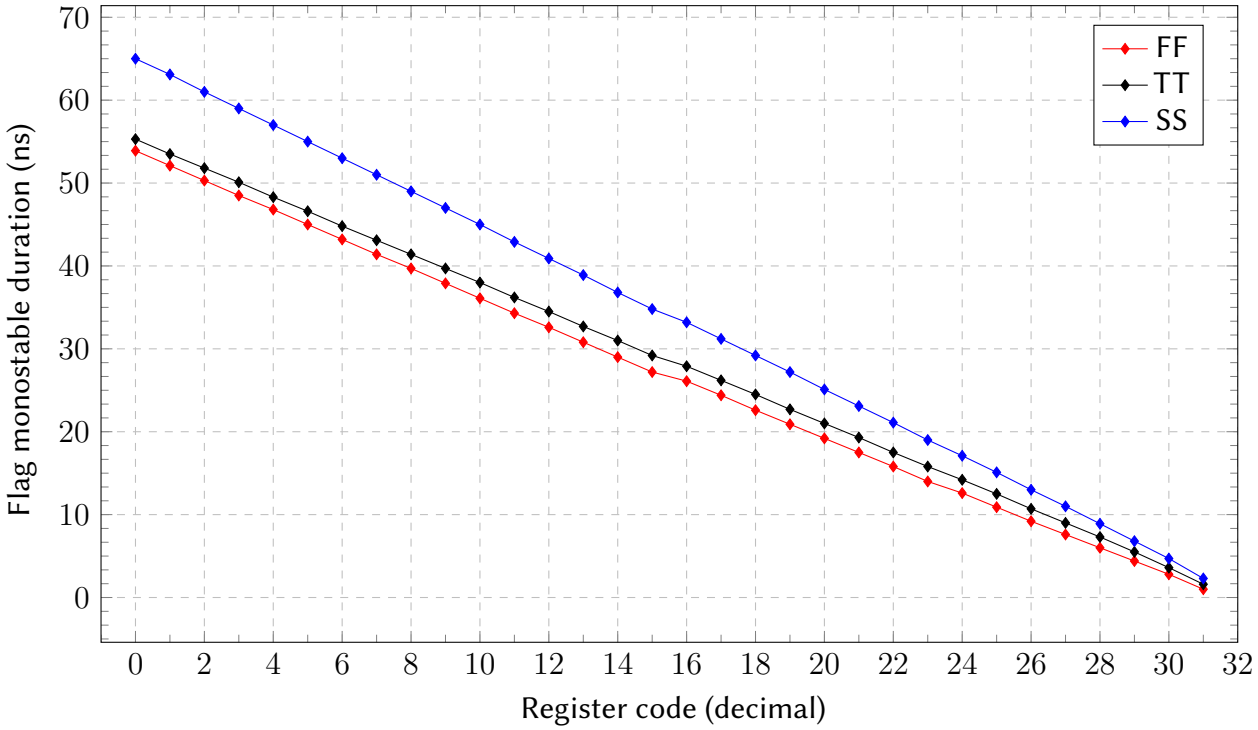


Figure 28: Flag monostable duration as a function of the register code



7.7.5 ANLG Register

Table 21: ANLG Register Definition

ANLG Register - 3 (0x03)															
UNUSED											ANLG_MON				
10	9	8	7	6	5	4	3	2	1	0	4	3	2	1	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEFAULT VALUE															
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

HEX	DEC
0x0000	**0**

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
ANLG_MON (5)	5 bits to adjust the amplitude of the analog monitor. A smaller amplitude will reduce the power consumption and help the analog monitor readout to detect more pixel with the same dynamic range. A higher amplitude will help with the single pixel resolution and increase the SNR of the analog monitor. The adjustment of these bits gives a *linear* amplitude adjustment. The analog monitor is disabled by filing the register with zeros (default value). The maximum analog monitor amplitude is achieved by filling the registers with ones. Any value in between is valid.	0 0 0 0 0 1 1 1 1 1 ...

7.7.6 STHH Register

Table 23: STHH Register Definition

STHH Register - 4 (0x04)															
UNUSED			SUM_TH_HIGH												
2	1	0	12	11	10	9	8	7	6	5	4	3	2	1	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEFAULT VALUE															
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

HEX	DEC
0x0000	0

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
SUM_TH_HIGH (13)	13 bits to adjust the higher threshold of the digital sum comparator. The digital sum comparator can be used to now if the number of triggered pixel is in a given range before transmitting the result to the tile controller. The comparator must be enabled (STHL Register) to operate, otherwise all comparator outputs remain low. The outputs of the comparator must be routed to either FLAG or DATA output to be used. The value of this register will impact the comparator outputs SUM_LT and SUM_IB. If the result of the digital sum is less than SUM_TH_HIGH, output (SUM_LT) will rise for one complete clock cycle. If the result of the digital sum is in between SUM_TH_HIGH and SUM_TH_LOW (STHL Register), output (SUM_IB) will rise for one complete clock cycle.	

7.7.7 STHL Register

Table 25: STHL Register Definition

STHL Register - 5 (0x05)															
EN_SUM_TH	UNUSED		SUM_TH_LOW												
0	1	0	12	11	10	9	8	7	6	5	4	3	2	1	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEFAULT VALUE															
0	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

HEX	DEC
0x1FFF	8191

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
EN_SUM_TH (1)	1 bit to enable the thresholds of the digital sum comparator. When this bit is unset (EN_SUM_TH=0), the digital sum does not reach the sum comparator module to reduce power consumption.	
SUM_TH_LOW (13)	13 bits to adjust the lower threshold of the digital sum comparator. The digital sum comparator can be used to know if the number of triggered pixel is in a given range before transmitting the result to the tile controller. The comparator must be enabled (EN_SUM_TH) to operate, otherwise all comparator outputs remain low. The outputs of the comparator must be routed to either FLAG or DATA output of the PDC to be used. The value of this register will impact the comparator outputs SUM_IB, SUM_GT and SUM_EQ. If the result of the digital sum is in between SUM_TH_HIGH (STHH Register) and SUM_TH_LOW, output (SUM_IB) will rise for one complete clock cycle. If the result of the digital sum is greater than SUM_TH_LOW, output (SUM_GT) will rise for one complete clock cycle. If the result of the digital sum is equal to SUM_TH_LOW, output (SUM_EQ) will rise for one complete clock cycle.	

7.7.8 ACQA Register

Table 27: ACQA Register Definition

ACQA Register - 6 (0x06)															
PRD_A								N_ACQ_A							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEFAULT VALUE															
0	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**0**

HEX	DEC
0x1432	**5170**

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
PRD_A (8)	8 bits to adjust the spacing between each PDC internal acquisition for acquisition Bank A. The PDC has two types of acquisition, external and internal. External acquisition is when a sample is taken each time the acquisition clock (CLK) rises. Any pattern can be used for the external acquisition clock : continuous, intermittent, etc. This is driven by the tile controller. Internal acquisition uses the PDC internal finite state machine to set when to take a digital sum sample. When sending a continuous clock on the PDC CLK input, the period of the samples is set by PRD_A. It sets the spacing between each sample. When all bits are set to 0 (value = 0), the PDC will take a sample at each clock cycle. The acquisition period is then the same as CLK period. When all bits are set to 1 (value = 255), the PDC will take a sample, wait for 255 clock cycle before the next sample. The acquisition period is then the CLK period divided by 256.	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
N_ACQ_A (8)	8 bits to set the number of samples to acquire in internal acquisition for Bank A. When using the internal acquisition driven by the PDC internal finite state machine, N_ACQ_A sets the number of samples for Bank A. When all bits are set to 0 (value = 0), no sample is taken. When all bits are set to 1 (value = 255), up to 255 samples can be taken. But since the PDC has only a FIFO large enough for 128 samples, the first samples might be overwritten, or the last samples lost.	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1

7.7.9 ACQB Register

Table 29: ACQB Register Definition

ACQB Register - 7 (0x07)															
PRD_A								N_ACQ_A							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEFAULT VALUE															
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**

HEX	DEC
0x020A	522

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
PRD_B (8)	8 bits to adjust the spacing between each PDC internal acquisition for acquisition Bank B. The PDC has two types of acquisition, external and internal. External acquisition is when a sample is taken each time the acquisition clock (CLK) rises. Any pattern can be used for the external acquisition clock : continuous, intermittent, etc. This is driven by the tile controller. Internal acquisition uses the PDC internal finite state machine to set when to take a digital sum sample. When sending a continuous clock on the PDC CLK input, the period of the samples is set by PRD_B. It sets the spacing between each sample. When all bits are set to 0 (value = 0), the PDC will take a sample at each clock cycle. The acquisition period is then the same as CLK period. When all bits are set to 1 (value = 255), the PDC will take a sample, wait for 255 clock cycle before the next sample. The acquisition period is then the CLK period divided by 256.	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
N_ACQ_B (8)	8 bits to set the number of samples to acquire in internal acquisition for Bank B. When using the internal acquisition driven by the PDC internal finite state machine, N_ACQ_B sets the number of samples for Bank B. When all bits are set to 0 (value = 0), no sample is taken. When all bits are set to 1 (value = 255), up to 255 samples can be taken. But since the PDC has only a FIFO large enough for 128 samples, the first samples might be overwritten, or the last samples lost.	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1

7.7.10 DBGC Register

Table 31: DBGC Register Definition

DBGC Register - 8 (0x08)															
DBG_CNT_EN	UNUSED		DBG_VAL												
0	1	0	12	11	10	9	8	7	6	5	4	3	2	1	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEFAULT VALUE															
0	**0**	**0**	**1**	**0**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**1**

HEX	DEC
0x11CD	4557

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
DBG_CNT_EN (1)	1 bit to enable the internal debug counter of the PDC. When this bit is unset (DBG_CNT_EN=0), the clock towards the debug counter module is disabled to reduce power consumption.	
DBG_VAL (13)	13 bits to store a debug value to be used by the PDC. The first use is as a FIFO input source. The content of DBG_VAL is stored into the PDC FIFO. The second use is for data transmission. The content of DBG_VAL is transmitted by the PDC. These two usages are for debug purposes and not required in normal operation of the PDC.	

7.7.11 FIFO Register

Table 33: FIFO Register Definition

FIFO Register - 9 (0x09)															
UNUSED		OVERWR_DIS	FIFO_EN	UNUSED		SEL_FIFO_IN		UNUSED	FIFO_DEPTH						
1	0	0	0	1	0	1	0	0	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEFAULT VALUE															
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

HEX	DEC
0x007F	127

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
OVERWR_DIS (1)	1 bit to disable the PDC FIFO overwrite of the external acquisition of the PDC. In typical operation, when the PDC is executing the external acquisition (each clock cycle is an acquisition), the FIFO overwrites the first samples when the number of samples is larger than the FIFO size. To stop the FIFO from overwriting, this configuration bit can be used. To overwrite previous data when FIFO is full (e.g. to reject DCR), set this bit to 0 To stop saving data into the FIFO when it is full, set this bit to 1	 0 1
FIFO_EN (1)	1 bit to enable the FIFO of the PDC. When this bit is unset (FIFO_EN=0), the clock towards the FIFO is disabled to reduce power consumption. No data can be written or read using the FIFO. To use the FIFO during the acquisition, the FIFO must be enabled (FIFO_EN=1)	 0 1
SEL_FIFO_IN (2)	2 bits to select the input data source for the FIFO. There are three options : the digital sum (DSUM), the debug counter (DBGC) and the debug register (DBGR). DSUM is the default option to use with the digital sum. DBGC, when the debug counter is enabled (DBGC Register - 0x08) the value of the counter is increased at each clock cycle and then stored into the FIFO. DBGR will copy the content of DBG_VAL (DBGC Register - 0x08) into the FIFO. UNSD will fill the FIFO with zeros.	 0 0 0 1 1 0 1 1
FIFO_DEPTH (7)	7 bits to select the depth of the FIFO. This register sets the depth of the FIFO when using the external acquisition of the PDC. During the overwriting mode, it sets the number of samples before starting to overwrite the older samples. When overwriting is disabled, it sets when the FIFO stops saving data. The depth of the FIFO is the value stored in this register plus one. When set to 0 (all zeroes), the depth of the FIFO is 1 When set to 1, the depth of the FIFO is 2 ... When set to 127 (all ones), the depth of the FIFO is 128	 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1

7.7.12 DTXC Register

Table 35: DTXC Register Definition

DTXC Register - 10 (0x0A)															
SPACING				UNUSED				DATA_LEN_CMD				DATA_LEN_FIFO			
3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEFAULT VALUE															
0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0

HEX	DEC
0x00CC	204

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
SPACING (4)	4 bits to add an extra spacing between each data sample. In normal operation, no extra spacing is required (SPACING=0). This gives the best performances in terms of data transfer rate. When SPACING > 0, the DATA line remains to 0 until the next start bit. A SPACING of 0 will add no idle bit between the stop bit and the start bit of the next data transmission. A SPACING of 1 will add one idle bit between the stop bit and the start bit of the next data transmission. The maximum SPACING is 15 clock cycles between the stop bit and the start bit of the next data transmission.	0 0 0 0 0 0 0 1 1 1 1 1
DATA_LEN_CMD (4)	4 bits to set the number of bits in the data transmission started by a command (CMD_SEL=ODTX). The data that can be transmitted from a command are : • The digital sum output (DATA_DSUM) without using the FIFO. • The debug counter output (DATA_DBGC) without using the FIFO. • The debug register content (DATA_DBGR) without using the FIFO. • The ASIC ID (DATA_ASID) which is an hard-coded pattern to debug the data transmission. When DATA_LEN_CMD=0, no data bits are sent. The data transmission only contains the following bits: start, external acquisition, overflow, CRC and stop. If the data to transmit is 0, the overflow bit will be 0, otherwise the overflow bit will be set to 1. When DATA_LEN_CMD=N where 0 < N < 12, N data bits are sent. If the data to transmit is larger than what can be represented bit 2^N-1, the overflow bit will be 1, otherwise the overflow bit will be set to 0. When DATA_LEN_CMD=12, 12 data bits are sent. If the data to transmit is larger than what can be represented bit 2^{12}-1, the overflow bit will be 1, otherwise the overflow bit will be set to 0.	0 0 0 0 1 1 0 0
DATA_LEN_FIFO (4)	4 bits to set the number of bits in the data transmission of the content of the FIFO. This setting applies to the transmission of the content of the FIFO (DATA_FIFO) When DATA_LEN_FIFO=0, no data bits are sent. The data transmission only contains the following bits: start, external acquisition, overflow, CRC and stop. If the data to transmit is 0, the overflow bit will be 0, otherwise the overflow bit will be set to 1. When DATA_LEN_FIFO=N where 0 < N < 12, N data bits are sent. If the data to transmit is larger than what can be represented bit 2^N-1, the overflow bit will be 1, otherwise the overflow bit will be set to 0. When DATA_LEN_FIFO=12, 12 data bits are sent. If the data to transmit is larger than what can be represented bit 2^{12}-1, the overflow bit will be 1, otherwise the overflow bit will be set to 0.	0 0 0 0 1 1 0 0

7.7.13 OUTD Register

Table 37: OUTD Register Definition

OUTD Register - 11 (0x0B)															
MODE_ELSE	MODE_ACQTX	MODE_TX	MODE_ACQ	UNUSED	DATA_SEL1					UNUSED	DATA_SEL0				
0	0	0	0	0	4	3	2	1	0	0	4	3	2	1	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEFAULT VALUE															
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

HEX	DEC
0x0082	130

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
MODE_ELSE (1)	1 bit to select between DATA_SEL1 or DATA_SEL0 for DATA pin function when no mode is active (MODE_ACQTX, MODE_TX and MODE_ACQ). When MODE_ELSE=0, DATA_SEL0 is selected when no mode is active. When MODE_ELSE=1, DATA_SEL1 is selected when no mode is active.	 0 1
MODE_ACQTX (1)	1 bit to select between DATA_SEL1 or DATA_SEL0 for DATA pin function when acquisition and data transmission occurs at the same time. When MODE_ACQTX=0, DATA_SEL0 is selected during simultaneous data acquisition and transmission. When MODE_ACQTX=1, DATA_SEL1 is selected during simultaneous data acquisition and transmission.	 0 1
MODE_TX (1)	1 bit to select between DATA_SEL1 or DATA_SEL0 for DATA pin function when only data transmission occurs. When MODE_TX=0, DATA_SEL0 is selected during data transmission. When MODE_TX=1, DATA_SEL1 is selected during data transmission.	 0 1
MODE_ACQ (1)	1 bit to select between DATA_SEL1 or DATA_SEL0 for DATA pin function when only data acquisition occurs. When MODE_ACQ=0, DATA_SEL0 is selected during data acquisition. When MODE_ACQ=1, DATA_SEL1 is selected during data acquisition.	 0 1
DATA_SEL1 (5)	5 bits to select which signal to use for DATA_SEL1. Refer to Table 43 for the list of available signals and their register value. Default value is DATA (DEC = 2, HEX = 0x02)	 0 0 0 0 0
DATA_SEL0 (5)	5 bits to select which signal to use for DATA_SEL0. Refer to Table 43 for the list of available signals and their register value. Default value is DATA (DEC = 2, HEX = 0x02)	 0 0 0 0 0

7.7.14 OUTF Register

Table 39: OUTF Register Definition

OUTF Register - 12 (0x0C)															
MODE_ELSE	MODE_ACQTX	MODE_TX	MODE_ACQ	UNUSED	FLAG_SEL1					UNUSED	FLAG_SEL0				
0	0	0	0	0	4	3	2	1	0	0	4	3	2	1	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEFAULT VALUE															
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

HEX	DEC
0x0000	0

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
MODE_ELSE (1)	1 bit to select between FLAG_SEL1 or FLAG_SEL0 for FLAG pin function when no mode is active (MODE_ACQTX, MODE_TX and MODE_ACQ). When MODE_ELSE=0, FLAG_SEL0 is selected when no mode is active. When MODE_ELSE=1, FLAG_SEL1 is selected when no mode is active.	 0 1
MODE_ACQTX (1)	1 bit to select between FLAG_SEL1 or FLAG_SEL0 for FLAG pin function when acquisition and data transmission occurs at the same time. When MODE_ACQTX=0, FLAG_SEL0 is selected during simultaneous data acquisition and transmission. When MODE_ACQTX=1, FLAG_SEL1 is selected during simultaneous data acquisition and transmission.	 0 1
MODE_TX (1)	1 bit to select between FLAG_SEL1 or FLAG_SEL0 for FLAG pin function when only data transmission occurs. When MODE_TX=0, FLAG_SEL0 is selected during data transmission. When MODE_TX=1, FLAG_SEL1 is selected during data transmission.	 0 1
MODE_ACQ (1)	1 bit to select between FLAG_SEL1 or FLAG_SEL0 for FLAG pin function when only data acquisition occurs. When MODE_ACQ=0, FLAG_SEL0 is selected during data acquisition. When MODE_ACQ=1, FLAG_SEL1 is selected during data acquisition.	 0 1
FLAG_SEL1 (5)	5 bits to select which signal to use for FLAG_SEL1. Refer to Table 43 for the list of available signals and their register value. Default value is FLAG (DEC = 0, HEX = 0x00)	 0 0 0 0 0
FLAG_SEL0 (5)	5 bits to select which signal to use for FLAG_SEL0. Refer to Table 43 for the list of available signals and their register value. Default value is FLAG (DEC = 0, HEX = 0x00)	 0 0 0 0 0

7.7.15 OUTC Register

Table 41: OUTC Register Definition

OUTC Register - 13 (0x0D)															
UNUSED					FLAG_SELC					UNUSED	DATA_SELC				
4	3	2	1	0	4	3	2	1	0	0	4	3	2	1	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEFAULT VALUE															
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**0**

HEX	DEC
0x03DA	986

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
FLAG_SELC (5)	5 bits to select which signal to use for FLAG pin while PDC is in configuration mode. Refer to Table 43 for the list of available signals and their register value. Default value is CLK_CS (DEC = 15, HEX = 0x0F)	0 1 1 1 1
DATA_SELC (5)	5 bits to select which signal to use for DATA pin while PDC is in configuration mode. Refer to Table 43 for the list of available signals and their register value. Default value is CFG_VALID (DEC = 26, HEX = 0x1A)	1 1 0 1 0

Table 43: Output multiplexer signal select values

VALUE			FUNCTION NAME	TYPE	DESCRIPTION
dec	hex	bin			
0	0x00	b0 0000	FLAG	BASIC	Flag OR-tree output
1	0x01	b0 0001	CLK_TX	BASIC	Data transmission clock return
2	0x02	b0 0010	DATA	BASIC	Data transmission output
3	0x03	b0 0011	TRG_SRC	BASIC	Trigger signal returned for timing
4	0x04	b0 0100	VSS	UNSD	Unused , tied to VSS
5	0x05	b0 0101	PIX_FLAG	PIXEL	Pixel 0 flag output
6	0x06	b0 0110	PIX_QC	PIXEL	Pixel 0 quenching circuit output toward digital sum
7	0x07	b0 0111	PIX_SYNC	PIXEL	Pixel 0 synchronized quenching circuit output toward digital
8	0x08	b0 1000	SUM_LT	COMP	Digital sum comparator, less than STHH register
9	0x08	b0 1001	SUM_IB	COMP	Digital sum comparator, between STHL and STHH registers
10	0x0A	b0 1010	SUM_GT	COMP	Digital sum comparator, greater than STHL register
11	0x0B	b0 1011	SUM_EQ	COMP	Digital sum comparator, equal to STHL register
12	0x0C	b0 1100	MODE_ACQ	MODE	Acquisition mode of the PDC is activated
13	0x0D	b0 1101	MODE_TRG	MODE	Trigger mode of the PDC is activated
14	0x0E	b0 1110	MODE_CFG	MODE	Configuration mode of the PDC is activated
15	0x0F	b0 1111	CLK_CS	MODE	PDC chip select return
16	0x10	b1 0000	CLK_SYNC	CLK_FN	Internally generated acquisition synchronizer clock return
17	0x11	b1 0001	CLK_PIPE	CLK_FN	Internally generated digital sum pipeline clock return
18	0x12	b1 0010	FIFO_WR_EN	CLK_FN	FIFO write enable signal to generate FIFO write clock
19	0x13	b1 0011	FIFO_RD_EN	CLK_FN	FIFO read enable signal to generate FIFO read clock
20	0x14	b1 0100	TX_DATA_VALID	MISC	Data transmission valid strobe signal
21	0x15	b1 0101	FIFO_EMPTY	MISC	FIFO is empty
22	0x16	b1 0110	FIFO_OVERWR	MISC	FIFO is overwriting previous data
23	0x17	b1 0111	FIFO_FULL	MISC	FIFO is full
24	0x18	b1 1000	CFG_CLK	CFG	Configuration clock return
25	0x19	b1 1001	CFG_DATA	CFG	Configuration data return
26	0x1A	b1 1010	CFG_VALID	CFG	Configuration valid strobe
27	0x1B	b1 1011	CMD_VALID	CFG	Command valid strobe
28	0x1C	b1 1100	VDD_CORE	UNSD	Unused, tied to VDD_CORE
29	0x1D	b1 1101	VDD_CORE	UNSD	Unused, tied to VDD_CORE
30	0x1E	b1 1110	VDD_CORE	UNSD	Unused, tied to VDD_CORE
31	0x1F	b1 1111	VSS	UNSD	Unused, tied to VSS

7.7.16 TRGC Register

Table 44: TRGC Register Definition

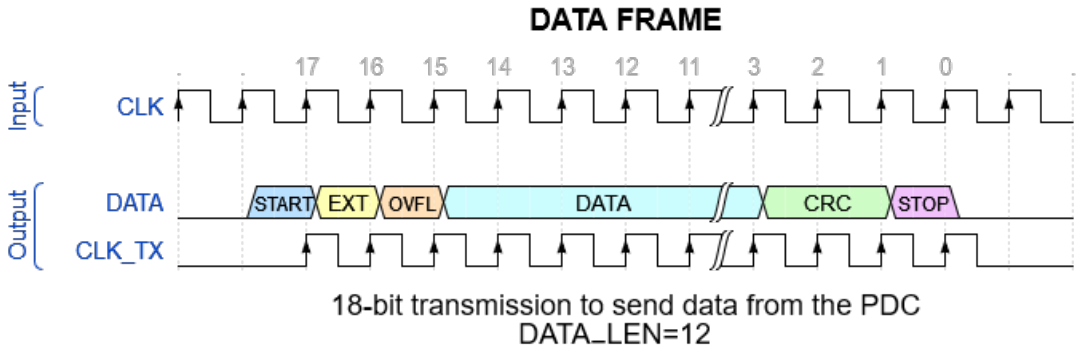
TRGC Register - 14 (0x0E)															
TRG_CMD_EN	UNUSED							TRG_TON							
0	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEFAULT VALUE															
0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

HEX	DEC
0x0000	0

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
TRG_CMD_EN (1)	1 bit to enable the trigger command. When this bit is unset (TRG_CMD_EN=0), a general command to trigger the PDC will have no effect. When this bit is set (TRG_CMD_EN=1), a general command to trigger the PDC will force a trigger of the enabled pixels.	 0 1
TRG_TON (8)	8 bits to set the period of the internal trigger which starts after the trigger command. The duration of the actual trigger pulse is the value of the register plus one. The clock cycles are counted on the CFG_CLK pin of the PDC. If the period TRG_TON is larger than 1, the user must ensure to send enough CFG_CLK cycles to prevent the PDC to remain on a triggered state. When TRG_TON is set to 0, the period of the internal trigger pulse is 1 CFG_CLK cycle. When TRG_TON is set to 127, the period of the internal trigger pulse is 128 CFG_CLK cycles.	 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1

7.8 Data Transmission

Figure 29: Chronogram of the signals to transmit DATA from the PDC with a 18-bit frame (DATA_LEN=12)



Based on the Table 46, the PDC data frame is formed with:

- START 1 bit to start data transmission with a value of 1 [17].
- EXT_ACQ 1 bit to indicate the sample has been acquired from the external acquisition (1) or from the PDC internal state machine (0) [16].
- OVERFLOW 1 bit to indicate the information to transmit does not fit into the number of specified bits (DATA_LEN) [15].
- DATA 12 to 0 bits to contain the data to transmit [14:3].
- CRC 3 bits to match the content of the frame (excluding start and stop bits) [3:1].
- STOP 1 bit to stop data transmission with a value of 0 [0].

Table 46: Description of the frame to send data from the PDC

DATA TRANSMISSION PROTOCOL																
START_BIT	EXT_ACQ	OVERFLOW	DATA												CRC		STOP_BIT
			11	10	9	8	7	6	5	4	3	2	1	0	1	0	
MSB	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB

BIT NAME	DESCRIPTION	VALUE (MSB to LSB)
START_BIT (1)	Transmission always begins with START BIT.	1
EXT_ACQ (1)	Indicate if the sample is acquired with the PDC CLK input (external) or with the PDC internal acquisition state machine. When the PDC is in external acquisition mode (EXT_ACQ=1), each clock cycle sent to the PDC on its CLK input triggers an acquisition, hence get a sample of the digital sum. When the PDC is in internal acquisition mode (EXT_ACQ=0), for a continuous clock sent to the PDC, the acquisitions is only triggered by the internal acquisition finite state machine. Based on the content of the acquisition configuration registers (ACQA and ACQB), the number of samples and the sampling period set when to get a sample of the digital sum.	 1 0
OVERFLOW (1)	Indicate if the configured number of DATA bits is enough to contain all the required information. When the information is fully contained in DATA, OVERFLOW=0. When the information is not fully contained in DATA, OVERFLOW=1.	 0 1
DATA (12-0)	Indicate if the configured number of DATA bits is enough to contain all the required information. The PDC has 4096 pixels on $5 \times 5\ mm^2$. 13 bits are required to contain all pixels state ($2^13 = 8192$). Here the sum is represented with a maximum of 12 bits and an OVERFLOW bit. The number of bits to transmit the content of DATA can be reduced dynamically with the configuration registers (DTXC Register). By reducing the number of bits, the MSBs will be omitted. If the number of expected photons is known and less than 4096 per bin, the number of bits can be reduced without loosing any information. When the DATA length is set to 0, only the OVERFLOW bit is used to indicate if DATA is 0 or not (Figure 30).	
CRC (2)	Checksum to validate the transmission of the data. START and STOP bits are not considered in the calculation of the CRC. Polynomial used is 2b01 with implicit first bit (3b101).	 0 1
STOP_BIT (1)	Transmission always end with STOP BIT.	0

Figure 30: Chronogram of the signals to transmit DATA from the PDC with a 6-bit frame (DATA_LEN=0)