	Page No.	
To conte a Venlog por venly it truth lable.	agram for all Logic gates and	
Fim: To write a virileg program for all Logic gata and virily to truth table.		
APPARATUS REWURED:		
5.No Component 1 haptop with Moder sim software	Speci-fication Oty 107411 1	
Verslog code:	INDIA	
AND Gate: module and 12 (a,b,c); Phoput a; Phoput b; Putput c; assign (= a &b end module	or Gate module on 12 (a,b,d); input a; input b; output d; awign d = a b; end module	
NARD Gata: module nand & (a,b,e): input a; input b; output e; assign e= ~ (98b). endmodule.	module xoria(a,b,h); Enput a; Enput b; output h; ousign h=aNb; endmodule	

	Page No.
Knor Gate:	NOTE GATE.
module xnor(2(a,b,i); Input a; input b; output i; assign i= ~(anb); endmodule	module nox(2(9, b, f): Input a; Input b; output f: assign f = ~ (alb): endmodule.
notule not 12 (9,9); input a; output g; assign g = ~a; endmodule chennal	INDIA
	res respired.

and full adder wing Model sim software:
AIM: To design and implement the furth table of the Italf adde and full adde wing model sim represent
APPARATUS REQUIRED:
8:No Component Specification Oty 1. Laptop with 107411 MODELIAM SOFTWARE
Verilog Locle
1. Half adder:
module hadd (a,b,s,c); input a; input b;
output 8;
ausign 8= 9Nb;
output s; output c; assign 8 = anb; assign c = asb; end module
2. Ful adder:
input a;

and Full subtractor wing Modelsim software.			
Aim: To design and implement the truth table of talf subtractor and full subtractor wing model sim			
APPRATUS REQUIRED:			
8. No Component Specification Oty 7. deeptop with 107471			
MODEL SIM Software			
Verilog Code:			
1. Half Subtractor - 2005			
module houb Carb, d'hor)			
Input 6;			
output bor;			
avign d= (a^b); avign box = (~a & ~b); end module			
CNU VIZICULE			

Page No.

	a. Full subtractor:
-	
-	module sub(a,b,c,d,b,out)
	input a;
	in out hi
	input c:
	originity q.
	methout bout.
	input c; output d; output bout; asign d= (9^b) ^c; assign bout - (~a &b) (b &c) (c2-ra); end module.
	assign bout: (20 8h) (6 b&c) (622a):
	end module.
	A) -IMAT - (A
	1 2 V O. L
	CHENNAI
£	SECULT:
Ċ	TUSULY
	The vinlog code was enecuted wing MODELSIM
1	officere and toutpill was renfied.
_6	ge Conque
	1000000

Design and implement the touth table of 401 Multiplene and 1404 De- Multiplene wing			
Multiplener and 1 to 4 De- Multiplener Wing			
Modelsim software.			
0.44			
To player and implement the shift table of 4 to 1			
To design and implement the furth table of 4+01 trustiplene and 1+04 De-Multiplene wing modelsm			
software.			
APPARATUS PIEQUIRED:			
s-No Component Specification Oty			
1. deeptop with 107477 1			
Much Bm			
Ciscottuciee INDIA			
Venlog Locle:			
1. 4 to 1 Phultiplener			
module mun 4 to 1 (4, 10, 11, 12, 13, sel);			
output y;			
input 10,12,12;			
input 10,12,12; Input [1:0] 8el;			
ng y;			
always @ (Sc) or 10 00 11 00 12 00 13)			
core (sel)			
ng y: always @ (sc) or 10 00 11 00 12 00 13) core (sel) 2 boo: y = 10;			
2' bo1: 4= 11;			
2 / b10: 4=12;			
2 1 617: 4 = 13;			
endage			

	Tage No.	
_	endmodule	
	2. 1 to 4 de-Multiplener:	
	module demun (S, D, y);	_
_	Input [1:0] 8;	
_	Input D;	
-	Input D: Output [3:0] y; 29y;	
- -	always @ (s o x)	
	αιναμς @ (s o x) Caye (f D,8 ζ) 3'b700: y = 4'b0001;	
╬	3'btoo: y= 4'booo1;	
╟	3'b101: y = 4'b0010; 3'b110: y = 4'b0100;	
\parallel	3 b710: y = 4 b0100;	
-	3' b721: y: 4' b0000;	
\vdash	default: cynjai4 600 00; INDIA	
_	enclase	
	endmodule	
	2005	
	Thowiedge Conquere All	
_	RESULT:	
	The Verilog Code was executed using Model Six	מ
	The Verilog Code was enecuted wing Model Sis	
a lista de la constanta de la	· · · · · · · · · · · · · · · · · · ·	
	,	_

Design and Implement the buth table of 2 to 4
Design and implement the touth table of 2 to 4 Design and 4 to 2 Envolu wing Modesim reflexue
AM: descen and analoment the table of
To design and emplement the touth table of 4 to 1 Multiplenee and 1 to 4 obe-Muliplenee using Model sim software
uing Model sim software
APPARATUS REQUIRED:
S.No Component specification Qty
1. daptop with 117471 1
Defuse
Venleg cocle
1. 2 to 4 Devoter:
module decoderay argen (en, a, b, y). // declare input and output posts
input en a a b;
output [3:0] y;
augn enb= ren;
augh hb = \rightarrows;
// assign output value by referring to Cogic
dicy 2a m

Page	No.
1 age	140.

assign glo] = 2 (enb 2 na 2 nb); axign y[1]= 1 (enb q na & b);
axign y[2]= ~ (enb 4 a & nb);
avign y[3]= 1 (enb 4 a & b);

end module.

2. 4 to 2 Encocler.

module prosty encode datation (Ao, A1 40, 41,42,43) Input 40, 41, 42, 43;

awign A) = 43+42

ouign A0 = 43 + ((242) & 41);

end module HENNAI

The visiting code was enecuted using moderson