PAPER ID-311337

Roll No: | | | | | | | | | | | | | |

B TECH
(SEM-III) THEORY EXAMINATION 2020-21
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours ***Total Marks: 100***

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 10 = 20**

Q no.	Question	Marks	CO
a.	Define the term Computer architecture and Computer organization.	2	1
b.	What is mean by bus arbitration? List different types of bus arbitration.	2	1
c.	Discuss biasing with reference to floating point representation.	2	2
d.	What is restoring method in division algorithm?	2	2
e.	Define micro operation and micro code.	2	3
f.	Write short note on RISC.	2	3
g.	Define hit ratio.	2	4
h.	What do you mean by page fault?	2	4
i.	Explain the term cycle stealing.	2	5
j.	What do you mean by vector interrupt? Explain.	2	5

SECTION B

2. Attempt any *three* of the following: **3 x 10 = 30**

Q no.	Question	Marks	CO
a.	i. Draw a diagram of bus system using MUX which has four registers of size 4 bits each. ii. Evaluate the arithmetic statement. X = A + B * [C * D + E * (F + G)] using a stack organized computer with zero address operation instructions.	10	1
b.	Explain in detail the principle of carry look ahead adder and design 4-bit CLA adder.	10	2
c.	Draw the flowchart for instruction cycle with neat diagram and explain.	10	3
d.	Discuss 2 D RAM and 2.5D RAM with suitable diagram.	10	4
e.	Draw and explain the block diagram of typical DMA controller.	10	5

SECTION C

3. Attempt any *one* part of the following:

Q no.	Question	Marks	CO
a.	An instruction is stored at location 400 with its address field at location 401.The address field has the value 500.A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (i) direct (ii) immediate (iii) relative (iv) register indirect (v) index with R1 as index register	10	1
b.	What do you mean by processor organization? Explain various types of processor organization.	10	1

4. Attempt any *one* part of the following:

Q no.	Question	Marks	CO
a.	Show the systemic multiplication process of (20) X (-19) using Booth's algorithm	10	2
b.	Explain IEEE standard for floating point representation. Represent the number $(-1460.125)_{10}$ in single precision and double precision format.	10	2

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5. Attempt any *one* part of the following:

Q no.	Question	Marks	CO
a.	What is a micro program sequencer? With block diagram, explain the working of micro program sequencer.	10	3
b.	Differentiate between hardwired and micro programmed control unit. Explain each component of hardwired control unit organization.	10	3

6. Attempt any *one* part of the following:

Q no.	Question	Marks	CO
a.	Calculate the page fault for a given string with the help of LRU & FIFO page replacement algorithm, Size of frames = 4 and string 1 2 3 4 2 1 5 6 2 1 2 3 7 6 3 2 1 2 3 6	10	4
b.	A computer uses RAM chips of 1024*1 capacity. i) How many chips are needed & how should their address lines be connected to provide a memory capacity of 1024*8? ii) How many chips are needed to provide a memory capacity of 16 KB?	10	4

7. Attempt any *one* part of the following:

Q no.	Question	Marks	CO
a.	What do you mean by asynchronous data transfer? Explain strobe control and hand shaking mechanism.	10	5
b.	Discuss the different modes of data transfer.	10	5