Rohan Mehta – VLSI Verification Engineer

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Professional Summary

Detail-oriented VLSI Verification Engineer with 4 years of experience in SystemVerilog, UVM methodology, and SoC-level functional verification. Proven track record in improving simulation efficiency and coverage closure.

Skills

- SystemVerilog, UVM, Verilog, VCS, QuestaSim
- AXI, AHB, SPI, UART protocol verification
- Functional Coverage, Assertions, Random Constraint Testing
- Scripting: Python, Perl, Shell

Experience

Intel Corporation – *Verification Engineer* (Jan 2021 – Present)

- Developed UVM testbench for DDR4 Controller verification.
- Automated regression suite, reducing runtime by 25%.
- Achieved 98% functional coverage for key blocks.

Cadence Design Systems – *Associate Engineer* (Jul 2019 – Dec 2020)

- Designed reusable verification IP for AXI4 interface.
- Debugged and resolved simulation failures in complex SoC flows.

Education

B.Tech in Electronics and Communication Engineering, NIT Trichy (2019)