Priya Sharma – ASIC Design Engineer

Email: priya.sharma.vlsi@gmail.com
Phone: +91-8823456789
Location: Hyderabad, India

Professional Summary

ASIC Design Engineer with 5+ years of experience in RTL design, synthesis, and static timing analysis for 7nm and 5nm nodes. Passionate about low-power SoC architecture and verification.

Skills

- RTL Design (Verilog, SystemVerilog), Synthesis (Design Compiler)
- STA, Linting, CDC checks, Low-power UPF
- EDA Tools: Synopsys DC, Primetime, Innovus

Experience

Qualcomm India Pvt Ltd – *ASIC Design Engineer* (2019 – Present)

- Designed and implemented high-speed datapath blocks for modem SoC.
- Worked on ECO closure and timing optimization for critical paths.

Wipro Technologies – *VLSI Engineer* (2017 – 2019)

- Delivered RTL blocks for multimedia subsystem with 100% code coverage.

Education

M.Tech in VLSI Design, IIT Delhi (2017)