Date: 09.04.2019

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Group ID: 21
Session ID: 2

CMPE 240 Experiment 5 Preliminary Work

1. State Register Inputs:

   Register 0:

   D = d0 = (n0+X).(X+n1).(X.n1) = X.n1

   Clock

   Register 1:

   D = d1 = (X.n1)+X’ = n1+X’

   Clock

2. State Register Outputs:

   Register 0:

   Q = n0

   Q’ = n0’

   Register 1:

   Q = n1

   Q’ = n1’

3. Combinational Block Inputs:

   X

   n0

   n1

4. Combinational Block Outputs:

   y0 = (n1.n0)+((X.n1)+X’)’ = (n1.n0)+(n1’.X)

   y1 = X’+n0’+n1’

   d0 = (n0+X).(X+n1).(X.n1) = X.n1

   d1 = (X.n1)+X’ = n1+X’

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5. Obtain the truth table.

Combinational Block Inputs			Combinational Block Outputs			
n1	n0	X	d1	d0	y1	y0
0	0	0	1	0	1	0
0	0	1	0	0	1	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
1	0	0	1	0	1	0
1	0	1	1	1	1	0
1	1	0	1	0	1	1
1	1	1	1	1	0	1

6. Is this a Moore or Mealy Machine?

   This is a Mealy Machine.

7. Draw the finite state machine.