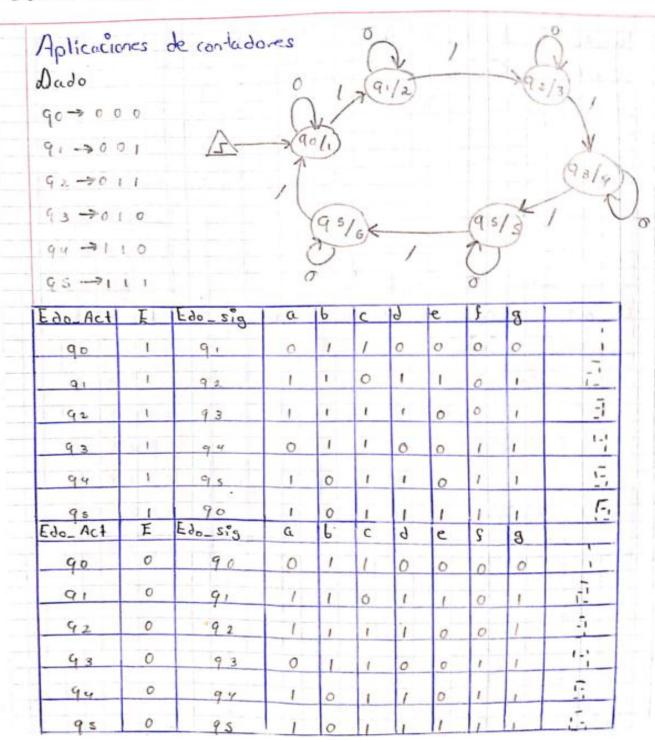




## PRÁCTICA 7 "APLICACIÓN DE CONTADORES"

Análisis de los circuitos con FF's

# Santos Mendez Ulises Jesus



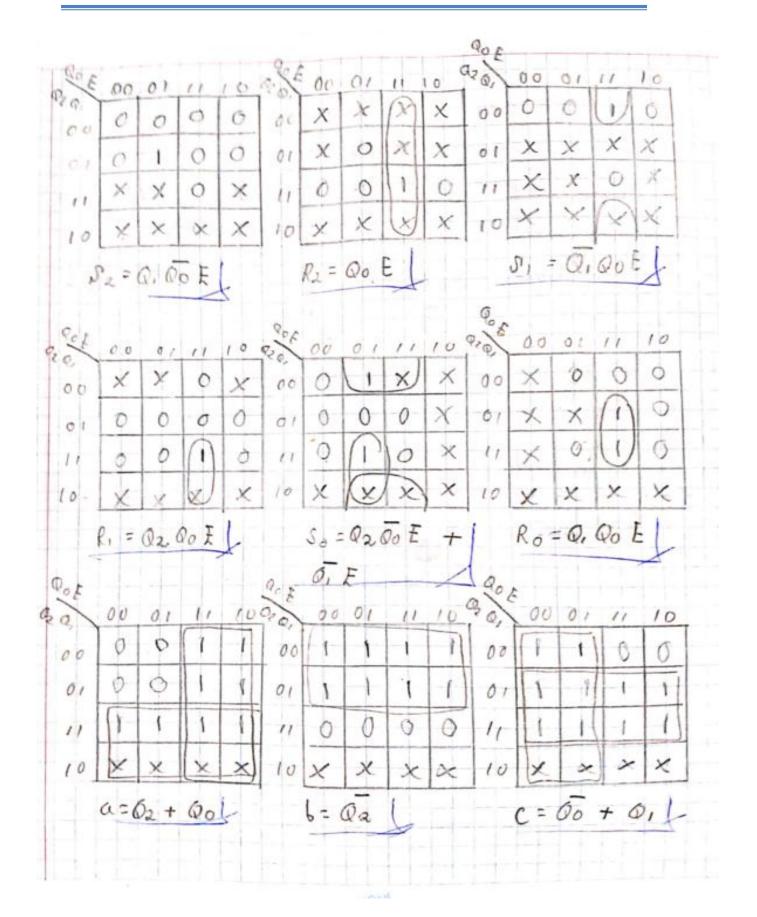




eda Act	E	Edo_Sig	a	P	C	9	C	f	3	Sa Ra Sa Ra Sa Ro
0 0 0	t	001	0	1	1	0	0	0	0	0 1 2 0 2 1 0
001		011	1	1	0	1	1	0	1	0 × 1 0 × 0
0 1 1	1	010	1	1	ī	1	0	0	1	0 x x 0 0 1
010	1	110	0	1	1	0	0	1	1	10x00x
110	t	111	t	0	,	ı	6	1	1	X 0 X 0 1 0
111	1	000	1	0	Ī	1	1	ī.	1	010101
Edo_Act	-	Edo-Sig		ι	C	9	e	ł	3	S2 R2 S1 R S0 R0
000	0	000	0	1	1	0	0	0	0	oxoxox
0 0 1	0	0 0.1	1	1-	0	- 1	1	0	1	0 × 0 × × 0
011	0	0 1 1	1		1	1	0	0	1	0 X X 0 X 0
010	0	010	0	1	1	6	0	1	1	0 × X 0 0 X
110	0	110	1	0	t	1	0,	1	1	X 0 X 0 0 X
111	0	111	1	0	1	1	1	i	1	xoxoxo

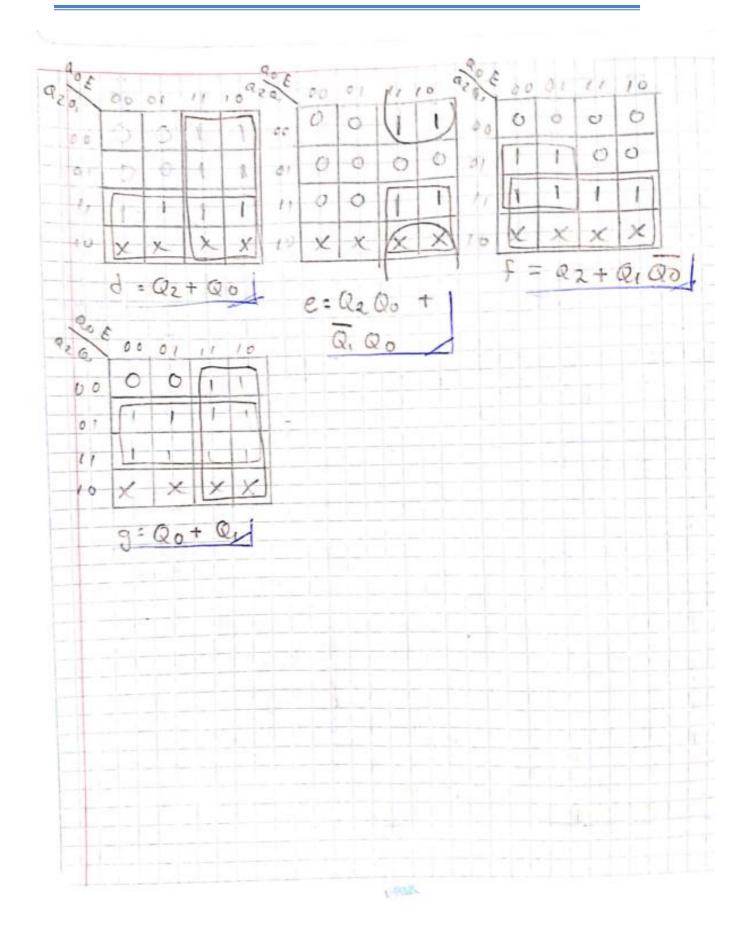






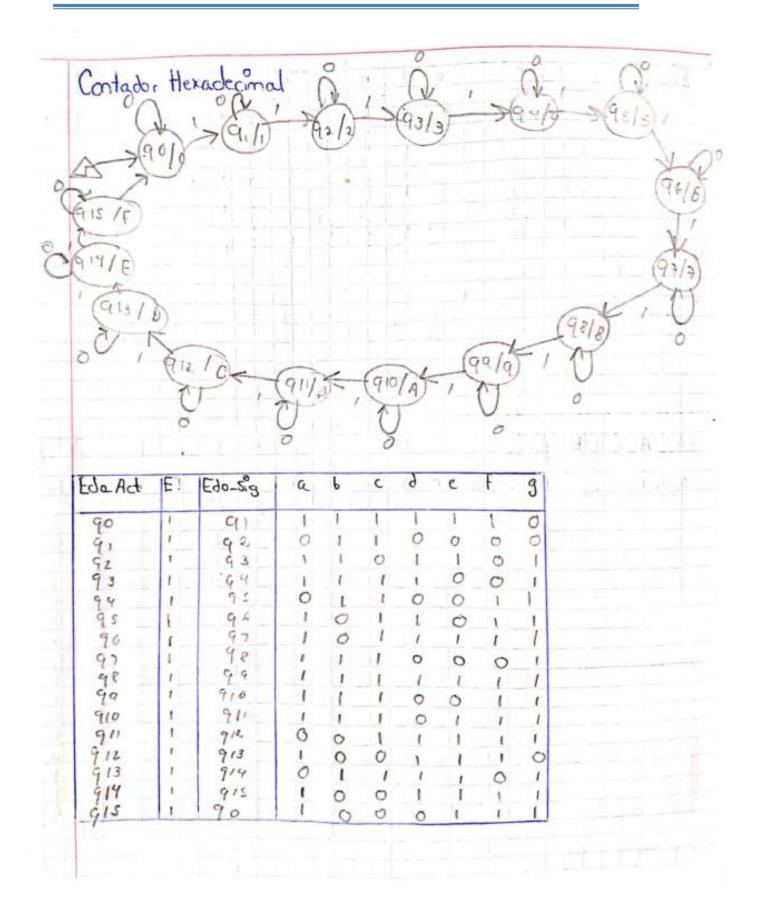
















da Act	E	Edo-Sig	a	16	C	19	e	1	8				
90	O	90	ī	1	1	1	t	t	0				
d.	0	91	0	1	1	0	0	0	0				
92	0	G Z	1	1	0	1	1	0	1				
92	0	93	1	1	1	1	000	0	1				
94	0	94	0	1	1	0	0	1	1				
94	0	95	1	0	1	1	0	1	1				
96	0	96	1	00	1	1	1	1	1				
97	0	92	1	1	1	0	0	0	1				
98	0	9.8	1	1	1	1	1	1	1				
99	0	99	1	1	1	0	0	1	1				
910	0	910	1	1	1	0	1	1	1				
911	0	911	0	0	1	1	t	1	1				
912	0	913	1	0	0	1	1	1	0				
913	0	715	0	1	1	1	1	0	1				
914	0		1	0	0 -	1.	1	1	-1				
	1	915 Edo-Si		00	0	10	e	t	اا	T3	2	4	
915 do_ Ac-	6	915		0	0	1	e	t	3	T3	2	4	1
915 30_ Act	0 E   1	915 Edo-Si		0	0	1	e	t	3 0		0	10	1
915 30_ Ac-	6	915 E 600- Si	t a	0	0	1	e 10	\$	100	<i>L</i> 3			I
915 30_ Ac-	0 E   1	915 E 600- Si	+ a	0	0	9	t	1	0	0	0	0	I
915 30_ Ac-	Qc .	915 Edo-Si, Q3 Q2Q Q	1 1 0	0	C	9	t	0	00	0	00	0	I
915 30_ Ac-	Qc .	915 Edo-Si, Q3 Q2Q Q	1 1 0 0 1	0	C	9	101	100	00	0000	00001	0-0	1
915 30_ Ac-	Qc	915 Edo-Si, Q3 Q2 Q1 Q	1 1 0 0 1 0 1 0 0 1 0 0 1 0 0 0 0 0 0 0	6	C	0 1	1010	100	00	00000	000	0101	1
915 30_ Ac-	Qc	915 Edo-Si 03 020 0	1 1 0 0 1 0 1 0 0 1 0 0 1 0 0 0 0 0 0 0	0	C	0 1	10-00	100	00	00000	000-00	0101	T
915 30_ Ac-	Qc	915 Edo-Si 03 02 00 0 1 0 0 0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0	1 1 0 0 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1		0 1 0 1 1 1 1 1 1	9	10-00	100	00	000000	000-000-	01010101	
915 30_ Ac-	Qc	915 Edo-Si, 915 1 000 1 001 1 001 1 010 1 010 1 010 1 010 1 010 1 001	1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 1 0 0 1 1	C	9	-0-000-0	1000111	00	0000000-0	000-000-0	010101010	
915 30_ Ac-	Qc	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 1	0 1 0 1 1 1 1 1 1	9 -000	10-000-0	10001110	00	0000000-00	000-000-00	01010101	
915 30_ Ac-	Qc	915 Edo-Si, 915 1 000 1 0000 1 0000 1 0000 1 0000 1 0000 1 0000 1 0000 1 0000 1 0	1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 1 1 1	0 1 0 1 1 1 1 1 1	9 -000-0	101000101	10001110	00	0000000-000	000-000-000	0-0-0-0-0	
915 30_ Ac-	0	915 EDO-SI, 03 02 00 0 1 0 0 0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0 0 0 1 0	1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 1 0 0 1 1 1 0 0	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	9 -0-10-10-00-	1010001010	10001110	00	0000000-0000	000-000-00	010101010101	
915 30_ Ac-	0	913 23 02 0 0 1 0 0	1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 0 0 1 1 1 0 0	0 1 0 1 1 1 1 1 0	9 -0-10-0-0-1	10100010101	10001110	00	00000-00000	000-000-000-0	0-0-0-0-0-0	
915 30_ Ac- 0302 Q1 000 000 000 000 000 000 000 000 000 0	0	913 23 02 0 0 1 0 0	1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 1 0 0 0 1	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	9 -0-10-10-00-	101000101011	10001110	00	000000-000000	000-000-000-00	01010101010101	I
915 30_ Ac- 0302 Q1 000 000 000 000 000 000 000 000 000 0	0	913 23 02 0 0 1 0 0	1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 0 0 1 1 1 0 0	0 1 0 1 1 1 1 1 0	9 -0-10-0-0-1	101000101011	1000111011	00	00000-00000	000-000-000-0	0-0-0-0-0-0	

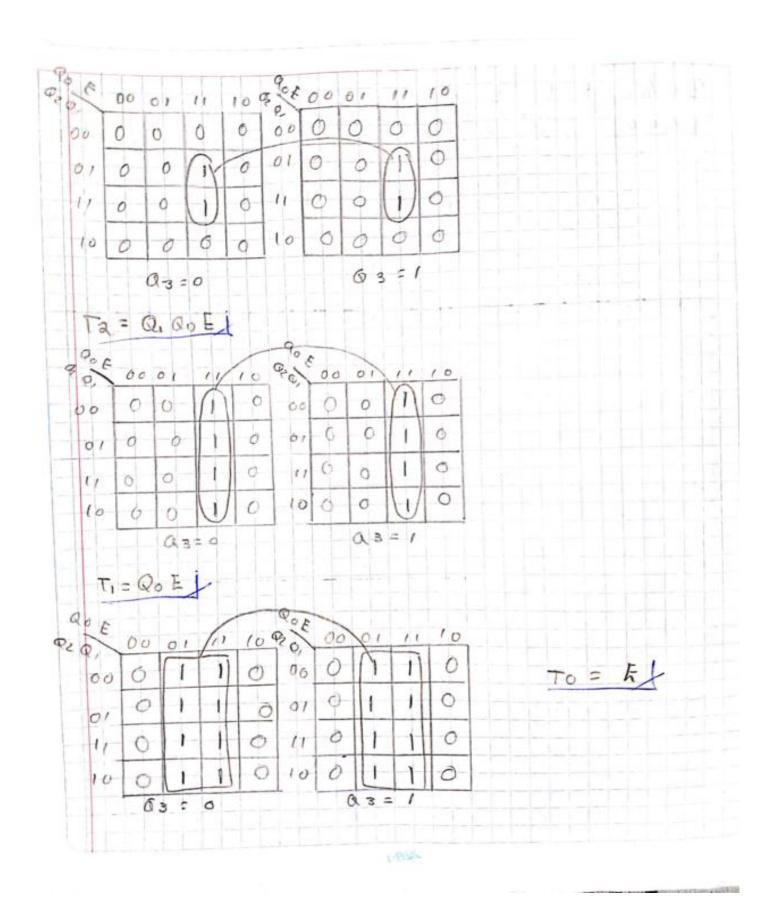




Edo.	Act a. ao	£	Eda Si		a	6	c	9	e	F	9	Ţ3	T.	T.	T
000000000000000000000000000000000000000	0 0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	000000000000000000000000000000000000000	0010100101010101	1	111110011100	1 1 1 1 1 1 0 1 0 0	10000	-0-000-0-0	1000111011	0.0	0000000000000000	00000000000000000	000000000000000000	
00	00 0	0 0	0 0	000		0	0	0	h						
01		0	0 0	0,		0	0	0							
11	0	0	0	",	0	0	0	0					12		
10	0	0	0	10	0	0	0	0		Ţ					
	Q:	3 = 0				0	3 =	/							i
٦	3 = 6	OzQ,	OOE												

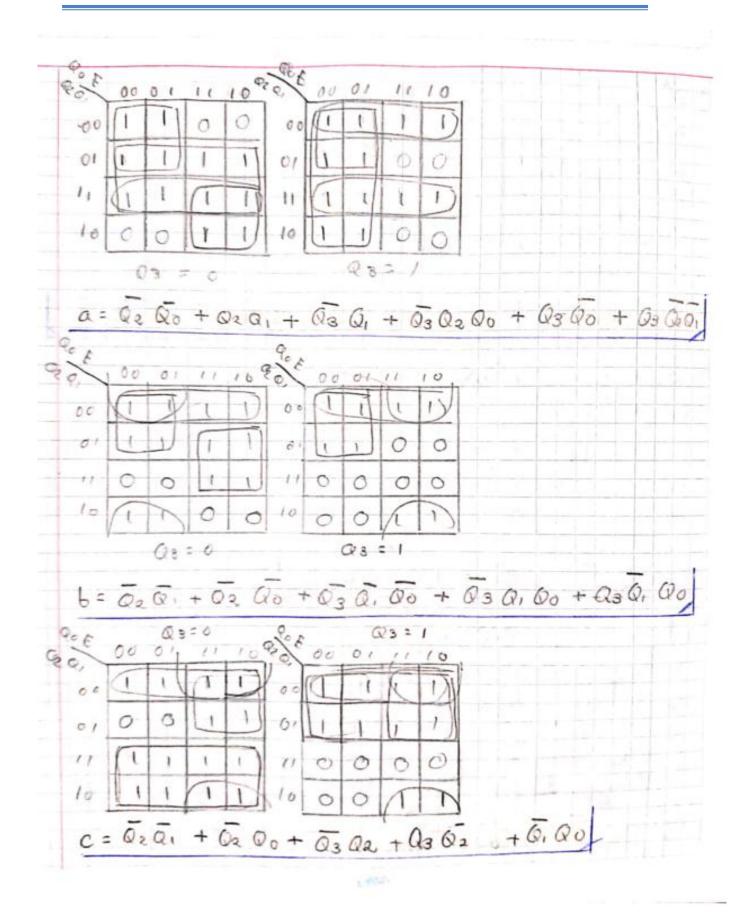






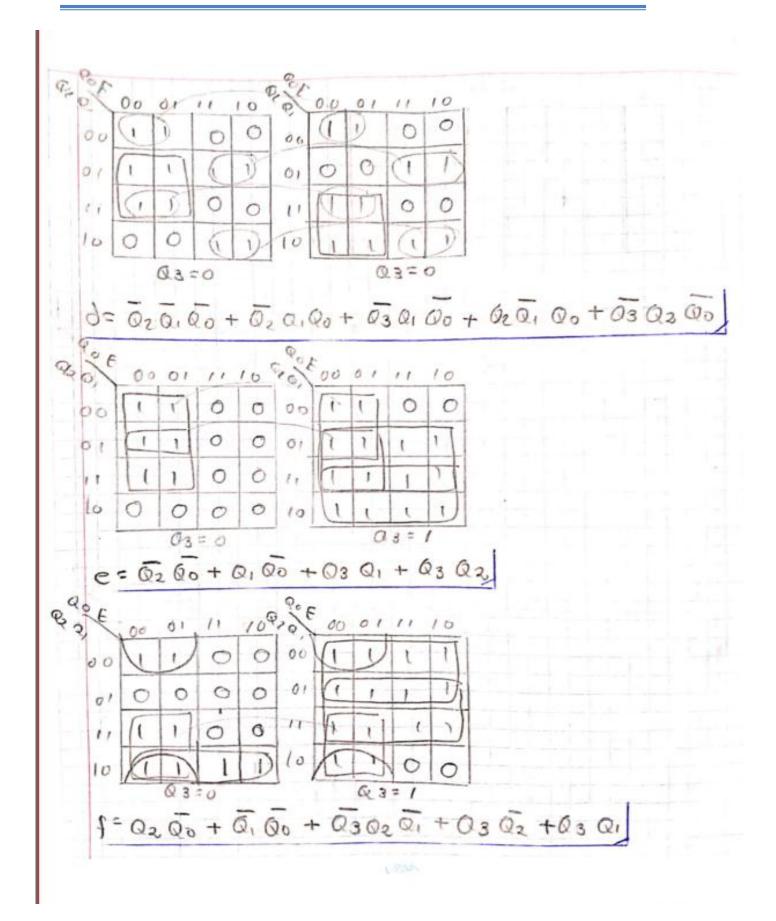






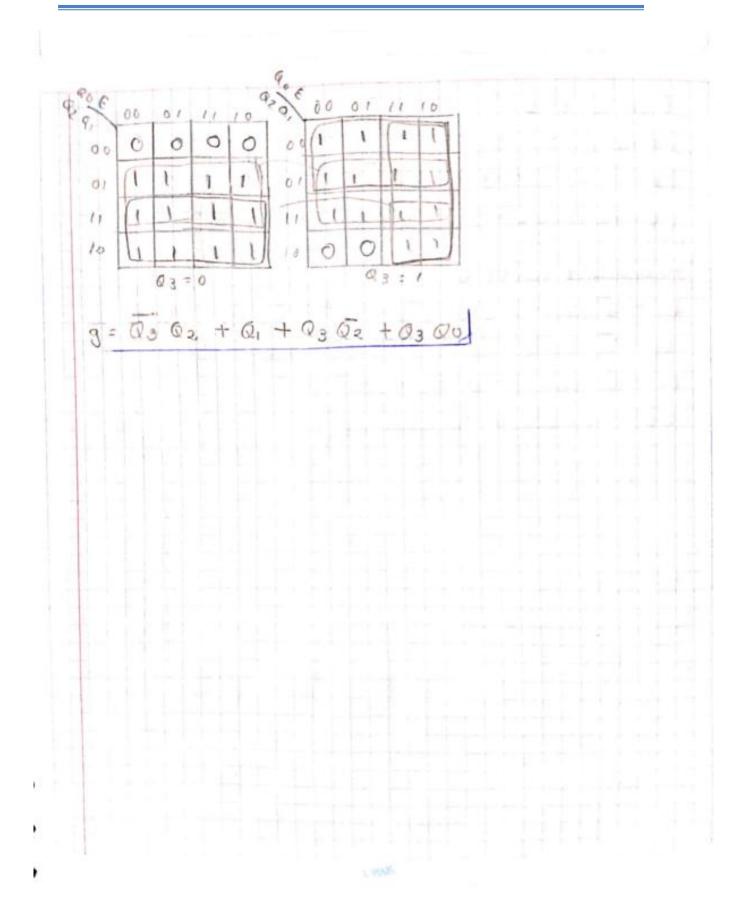






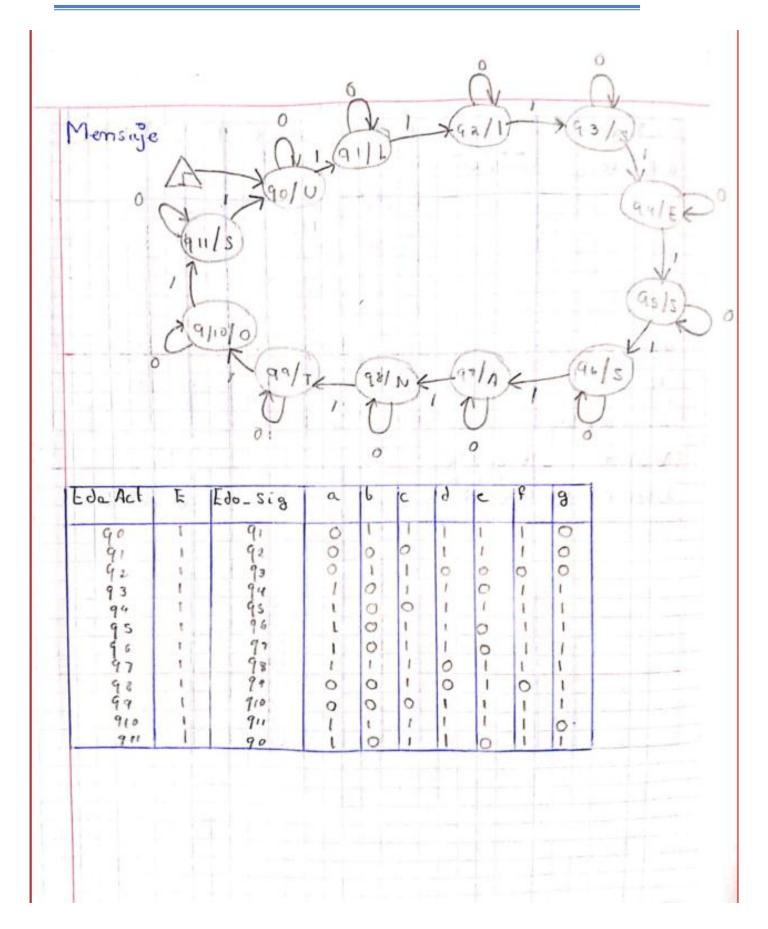












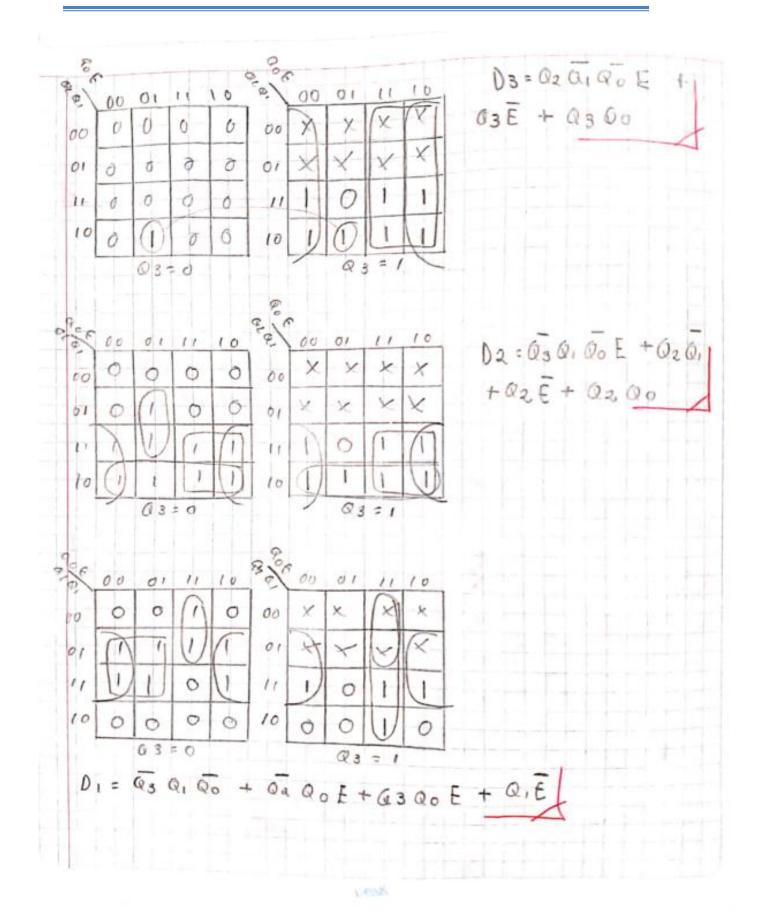




ada_Act as as as as	E	Eda Sig	a	Ь	C	d	e	ŧ	3	D3 D2 D1 D0
0000	1	0001	0	1	1	1	1	1	0	00001
0001	1	0011	0	0	0	1	1	1.	0	0 0 1
0011	1	0010	0	1	1	0	0	0	0	0010
0010	1	0110	1 -	0	1	1	0			0111
0 11 0	1	C 1 1 1	1	0	0	1	1			0101
0111	1	0101 .	1	0	t	1	0			0100
0101	1	0100	1	0	1		0	1		1100
0100	1	1100	1	t	. 1	0	1	0	1	11101
1100	1	1101	0	0	:	2	1	1	,	1 1 1 1
1101	1	1111	0	0	0	1.	1	1	0	1110
1111	1	0000	1,	0	1,	1	0		1	0000
O3 QLQ. Qo	E	Edo- 31 g	á.	6	c	9	e	F	8	Ds Dz Dı Do
0000	0	0000	0	1	1	1	1	1	0	0000
0001	0	0001	0	0	0	1	1	1	0	0001
0011	0	0011	0	1	1	0	0	0	0	0011
0010	0	0010	1	0	1	1	0	1	1	0010
0110	0	0110	1	0	0	1.	1	1	1	0110
0111	0	0111		0	1	1	0	1	1	0111
0101	0	0101		10		1	0	!	T.	0101
0100	0	1100	-	0	1	0	1	-	1	0100
1100	0	1 1 0 0	0 0	0	0	0	1	6	1	1100
	0	1101	- 0	1.	-	-1/	- 1	1	1	1101
1101	0	1 1 1 1	1	1	- 1	1				1 / 1 /

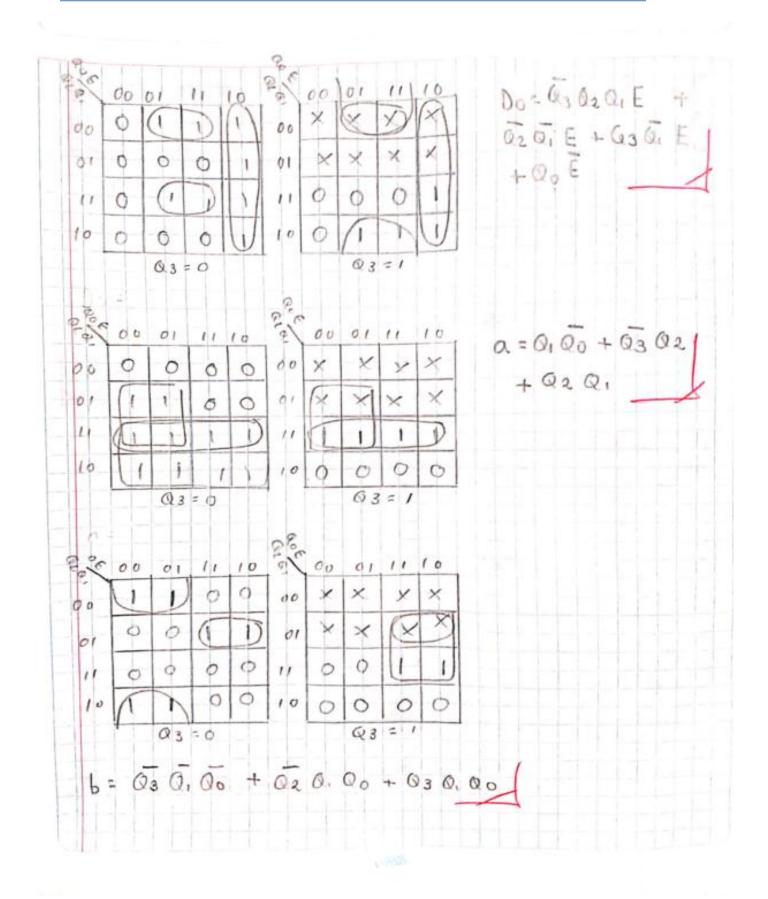






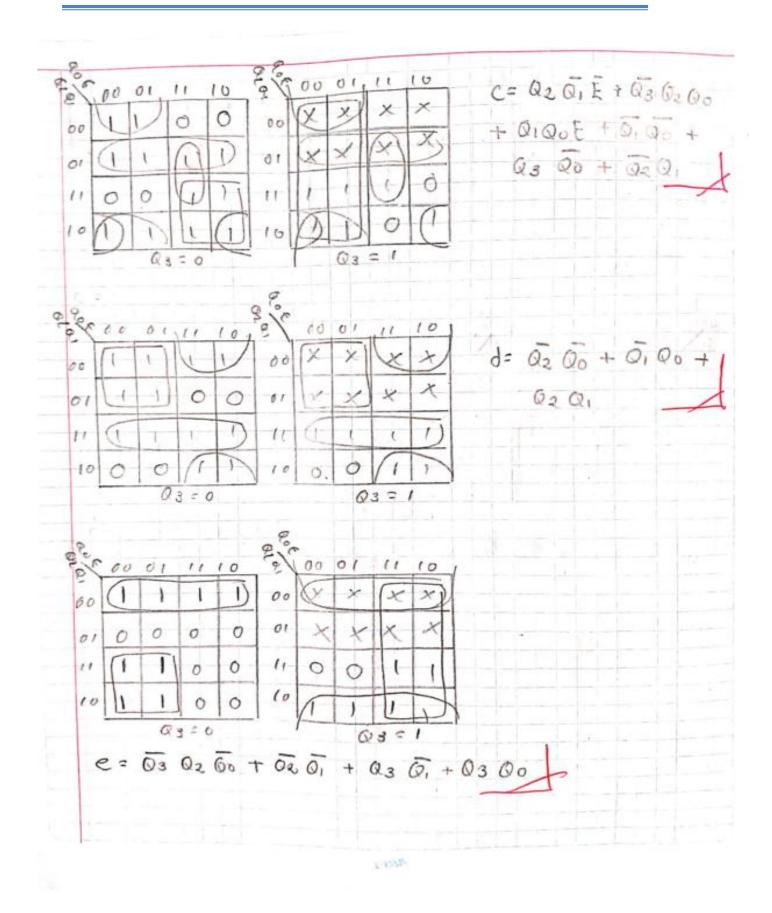






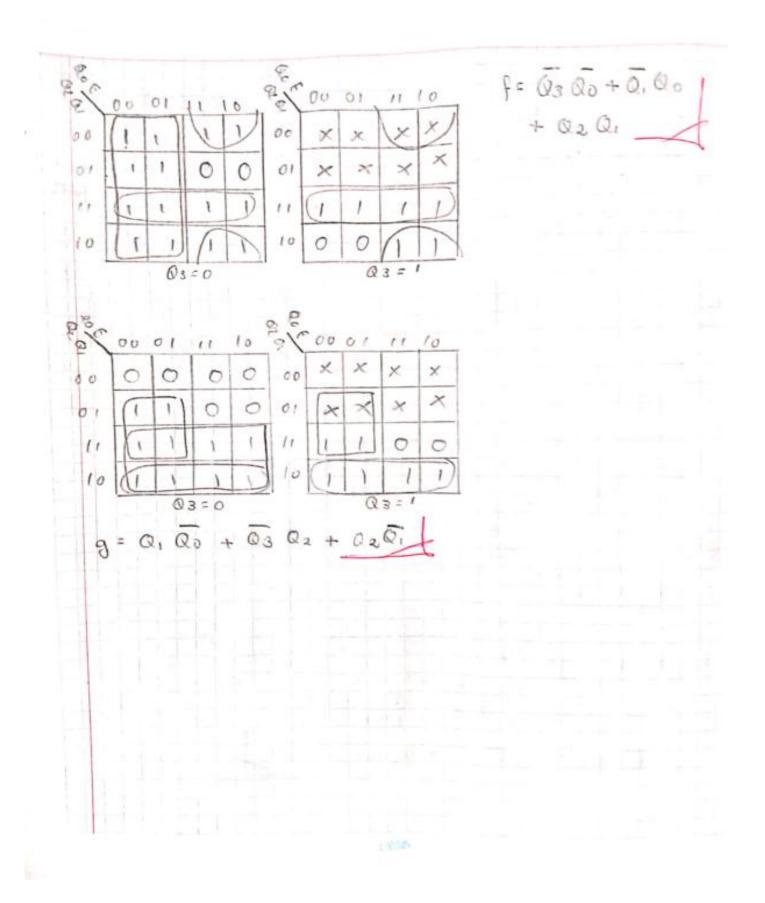






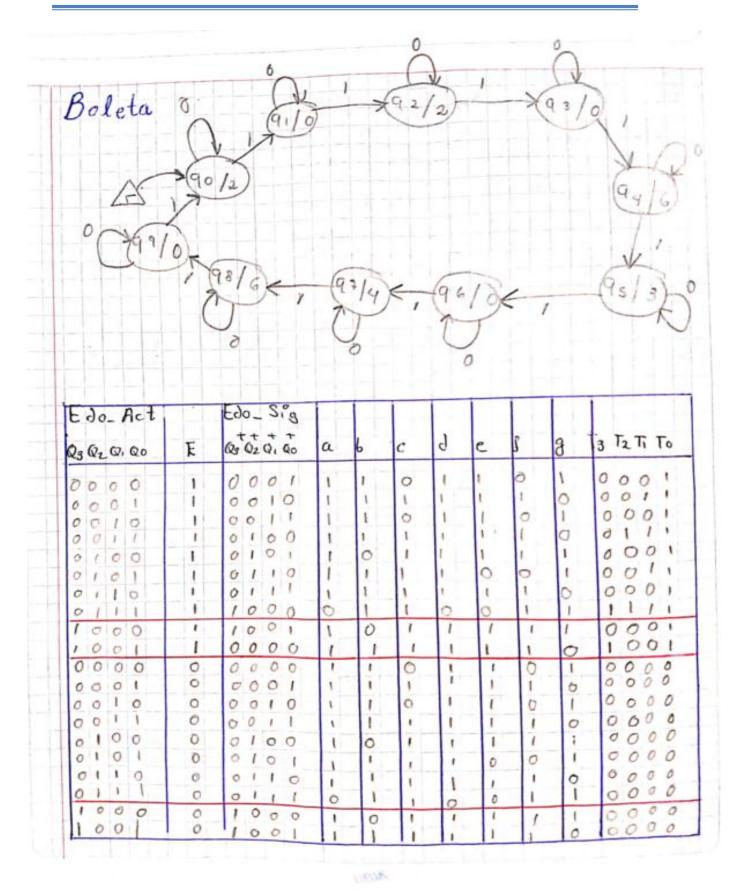








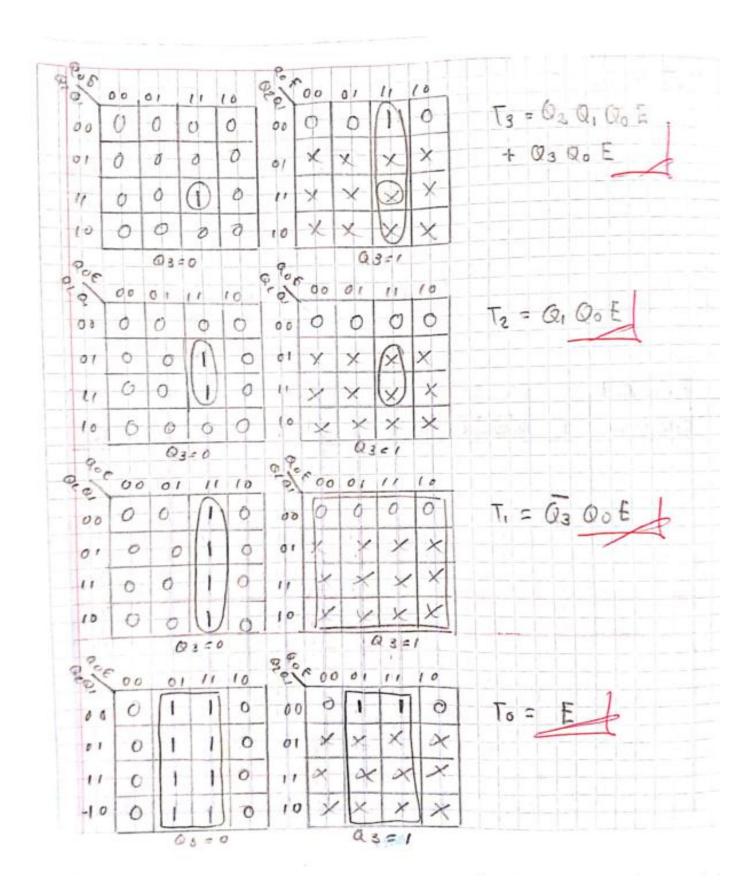




Facancada con ComCoonno

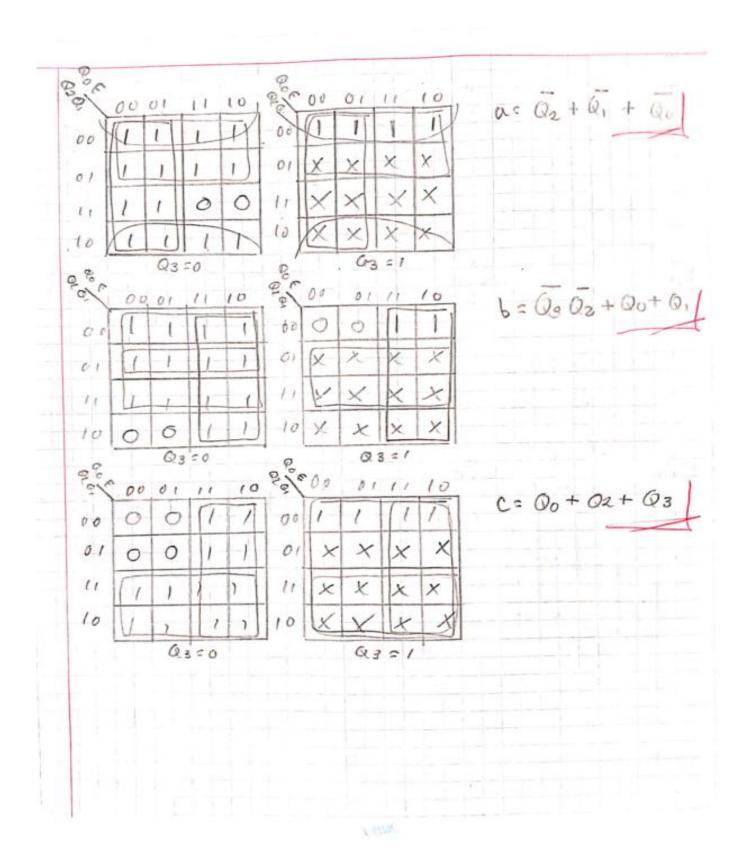






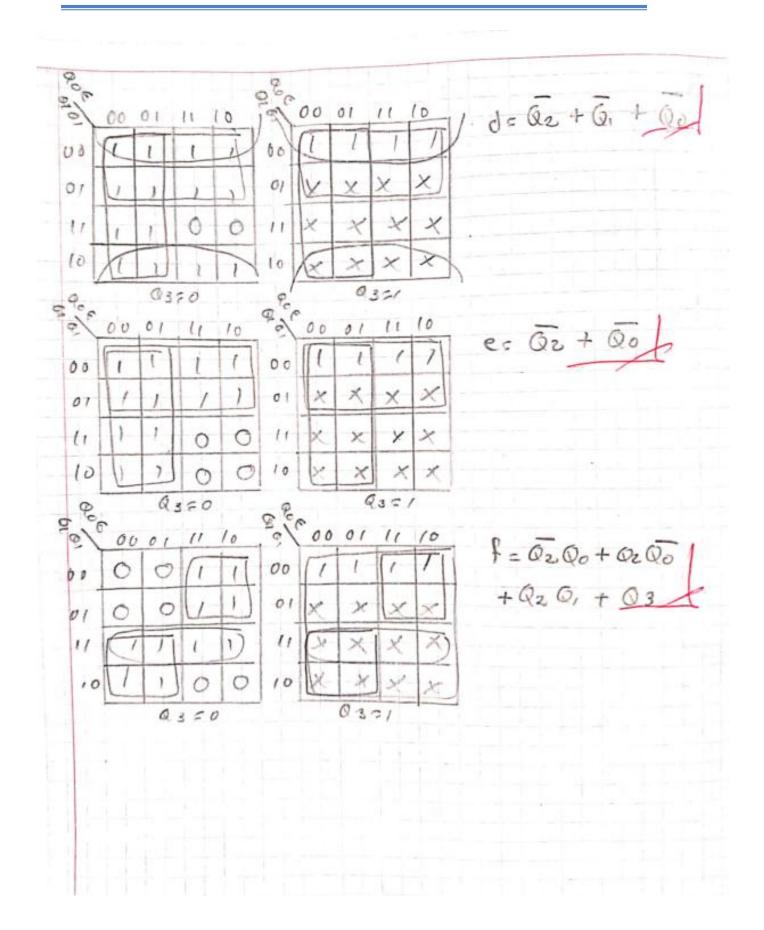






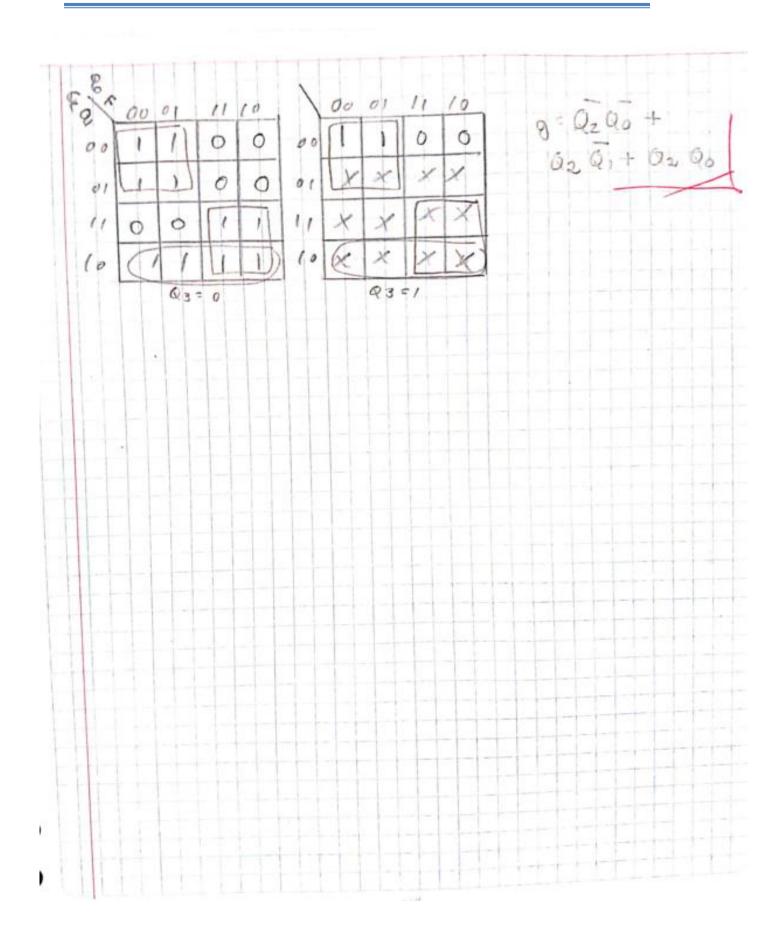
















## Código VHDL

1) Dados

```
1 -- Santos Mèndez Ulises Jesus
 2 -- 2CV8
 3 -- Pràctica 7"Aplicacion"//dados
 4 library ieee;
 5 use ieee.std logic 1164.all;
7 entity dados is
 8 port(clk,clr,en: in std logic;
9
       display: out std logic vector(6 downto 0));
10
11
       attribute pin numbers of dados: entity is
12
       "clr:13 en:2 display(6):21 display(5):20 "
13 €
       "display(4):19 display(3):18 display(2):17 "
14 & "display(1):16 display(0):15 ";
15 end dados;
16
17 architecture argdados of dados is
18 constant s1: std logic vector(6 downto 0) := "0110000";
19 constant s2: std logic vector(6 downto 0) := "1101101";
20 constant s3: std logic vector(6 downto 0) := "1111001";
21 constant s4: std logic vector(6 downto 0) := "0110011";
22 constant s5: std logic vector(6 downto 0) := "1011011";
23 constant s6: std logic vector(6 downto 0) := "10111111";
24 begin
```





```
25
26
       process(clk,clr)
27
       begin
28
           if(clr = '1')then
29
               display <= s1;
           elsif(rising edge(clk))then
30
               if(en = '1')then
31
32
                   case display is
33
                        when s1 => display <= s2;
34
                        when s2 => display <= s3;
35
                        when s3 => display <= s4;
36
                        when s4 => display <= s5;
37
                        when s5 => display <= s6;
38
                        when s6 => display <= s1;
39
                        when others => display <= s1;
40
                   end case:
41
               else
42
                   display <= display;
43
               end if:
           end if:
44
45
       end process;
46 end arqdados;
```





#### 2) Contador Hexadecimal

```
1 --Santos Mèndez Ulises Jesus
 2 --2CV8
 3 --Pràctica 7"Aplicacion"//contador hexadecimal
 4 library ieee;
 5 use ieee.std logic 1164.all;
 7 entity chexad is
 8 port(clk,clr,en: in std logic;
 9
        display: out std logic vector(6 downto 0));
10
11
        attribute pin numbers of chexad: entity is
12
        "clr:13 en:2 display(6):21 display(5):20 "
13 €
        "display(4):19 display(3):18 display(2):17 "
       "display(1):16 display(0):15 ";
14 €
15 end chexad:
16
17 architecture argchex of chexad is
18 constant s0: std logic vector(6 downto 0) := "11111110";
19 constant s1: std logic vector(6 downto 0) := "0110000";
20 constant s2: std logic vector(6 downto 0) := "1101101";
21 constant s3: std logic vector(6 downto 0) := "1111001";
22 constant s4: std logic vector(6 downto 0) := "0110011";
23 constant s5: std logic vector(6 downto 0) := "1011011";
24 constant s6: std logic vector(6 downto 0) := "10111111";
```





```
25 constant s7: std logic vector(6 downto 0) := "1110001";
26 constant s8: std logic vector(6 downto 0) := "11111111";
27 constant s9: std logic vector(6 downto 0) := "1110011";
28 constant sA: std logic vector(6 downto 0) := "1110111";
29 constant sB: std logic vector(6 downto 0) := "0011111";
30 constant sC: std logic vector(6 downto 0) := "1001110";
31 constant sD: std logic vector(6 downto 0) := "0111101";
32 constant sE: std logic vector(6 downto 0) := "1001111";
33 constant sF: std logic vector(6 downto 0) := "1000111";
34 begin
35
      process(clk,clr)
36
      begin
37
           if(clr = '1')then
38
               display <= s0;
           elsif(rising edge(clk))then
39
               if(en = '1')then
40
41
                   case display is
                       when s0 => display <= s1;
42
43
                       when s1 => display <= s2;
44
                       when s2 => display <= s3;
45
                       when s3 => display <= s4;
46
                       when s4 => display <= s5;
47
                       when s5 => display <= s6;
48
                       when s6 => display <= s7;
```





```
when s7 => display <= s8;
49
50
                        when s8 => display <= s9;
51
                        when s9 => display <= sA;
52
                        when sA => display <= sB;
53
                        when sB => display <= sC;
                        when sC => display <= sD;
54
55
                        when sD => display <= sE;
56
                        when sE => display <= sF;
57
                        when sF => display <= s0;
                        when others => display <= s0;
58
59
                   end case:
60
               else
61
                   display <= display;
62
               end if:
63
           end if:
64
       end process;
65 end argchex;
```





## 3) Mensaje (Letras repetidas)

```
1 -- Santos Mèndez Ulises Jesus
 2 --2CV8
 3 --Pràctica 7"Aplicacion"//mensaje
 4 library ieee;
 5 use ieee.std logic 1164.all;
 6
 7 entity mensaje is
 8 port(clk,clr,en: in std logic;
        display: out std logic vector(6 downto 0));
 9
10
11
        attribute pin numbers of mensaje: entity is
12
        "clr:13 en:2 display(6):21 display(5):20 "
        "display(4):19 display(3):18 display(2):17 "
13 €
       "display(1):16 display(0):15 ";
14 €
15 end mensaje;
16
17 architecture arqmensaje of mensaje is
18 constant 10: std logic vector(1 downto 0) := "00";
19 constant l1: std logic vector(1 downto 0) := "01";
20 constant 12: std logic vector(1 downto 0) := "10";
21 constant 13: std logic vector(1 downto 0) := "11";
22
23 constant sU: std logic vector(6 downto 0) := "0111110";
24 constant sL: std logic vector(6 downto 0) := "0001110";
```





```
25 constant sI: std logic vector(6 downto 0) := "0110000";
26 constant sS: std logic vector(6 downto 0) := "1011011";
27 constant sE: std logic vector(6 downto 0) := "1001111";
28 constant sA: std logic vector(6 downto 0) := "1110111";
29 constant sN: std logic vector(6 downto 0) := "0010101";
30 constant sT: std logic vector(6 downto 0) := "0001111";
31 constant s0: std logic vector(6 downto 0) := "11111110";
32
33 signal estado: std logic vector(8 downto 0);
34 begin
35
36
      process(clk,clr)
37
      begin
38
           if(clr = '1')then
39
               estado <= 10&sU;
40
           elsif(rising edge(clk))then
41
               if(en = '1')then
42
                   case estado is
43
                       when 10&sU => estado <= 10&sL;
                       when 10&sL => estado <= 10&sI;
44
45
                       when 10&sI => estado <= 10&sS:
46
                       when 10&sS => estado <= 10&sE;
47
                       when 10&sE => estado <= 11&sS:
48
                       when l1&sS => estado <= 12&sS:
49
                        when 12&sS => estado <= 10&sA;
50
                        when 10&sA => estado <= 10&sN;
51
                        when 10&sN => estado <= 10&sT;
52
                        when 10&sT => estado <= 10&sO;
53
                        when 10&s0 => estado <= 13&sS;
                        when 13&sS => estado <= 10&sU;
54
                        when others => estado <= "----";
55
56
                   end case:
57
               else
58
                   estado <= estado;
59
               end if:
60
           end if:
61
       end process;
62
       display <= estado(6 downto 0);
63 end argmensaje;
```





#### 4) Boleta alumno

```
1 -- Santos Mèndez Ulises Jesus
2 --2CV8
3 --Pràctica 7"Aplicacion"//No.Boleta
4 library ieee;
5 use ieee.std_logic_1164.all;
7 entity boleta is
8 port(clk,clr,en: in std logic;
       display: out std logic vector(6 downto 0));
9
10
11
        attribute pin numbers of boleta: entity is
12
       "clr:13 en:2 display(6):21 display(5):20 "
       "display(4):19 display(3):18 display(2):17 "
13 €
14 €
       "display(1):16 display(0):15 ";
15 end boleta;
16
17 architecture arqboleta of boleta is
18 constant 10: std logic vector(1 downto 0) := "00";
19 constant l1: std logic vector(1 downto 0) := "01";
20 constant 12: std logic vector(1 downto 0) := "10";
21 constant 13: std logic vector(1 downto 0) := "11";
22
23 constant s2: std logic vector(6 downto 0) := "1101101";
24 constant s0: std logic vector(6 downto 0) := "11111110";
```





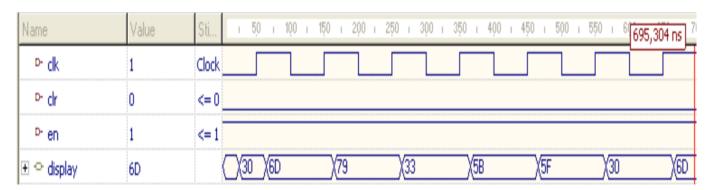
```
25 constant s6: std logic vector(6 downto 0) := "1011111";
26 constant s3: std logic vector(6 downto 0) := "1111001";
27 constant s4: std logic vector(6 downto 0) := "0110011";
28
29 signal estado: std logic vector(8 downto 0);
30 begin
31
32
      process(clk,clr)
33
      begin
34
           if(clr = '1')then
35
               estado <= 10&s2;
           elsif(rising edge(clk))then
36
               if(en = 11)then
37
38
                   case estado is
39
                       when 10&s2 => estado <= 10&s0;
40
                       when 10&s0 => estado <= 11&s2;
41
                       when 11&s2 => estado <= 11&s0;
42
                       when 11&s0 => estado <= 10&s6;
43
                       when 10&s6 => estado <= 10&s3;
44
                       when 10&s3 => estado <= 12&s0;
45
                       when 12&s0 => estado <= 10&s4;
46
                       when 10&s4 => estado <= 11&s6;
47
                       when 11&s6 => estado <= 13&s0;
48
                       when 13&s0 => estado <= 10&s2;
49
                        when others => estado <= "----";
50
                    end case:
51
               else
52
                    estado <= estado;
53
               end if:
           end if:
54
55
      end process:
56
       display <= estado(6 downto 0);
57 end arqboleta;
```

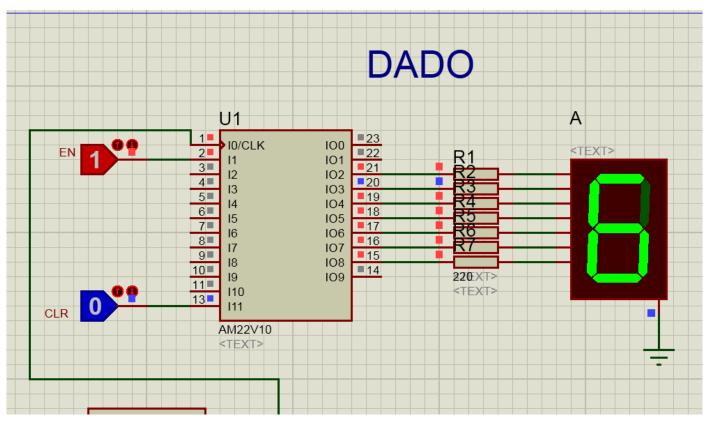




## Simulación en Proteus y en Active HDL-Sim

## 1) Dados

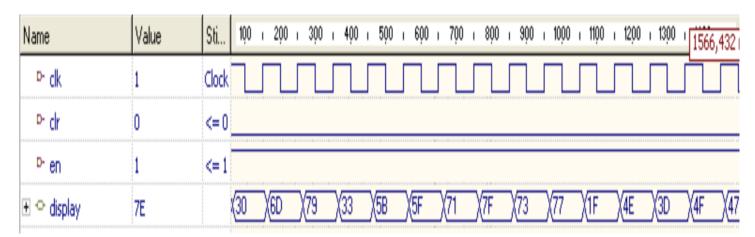


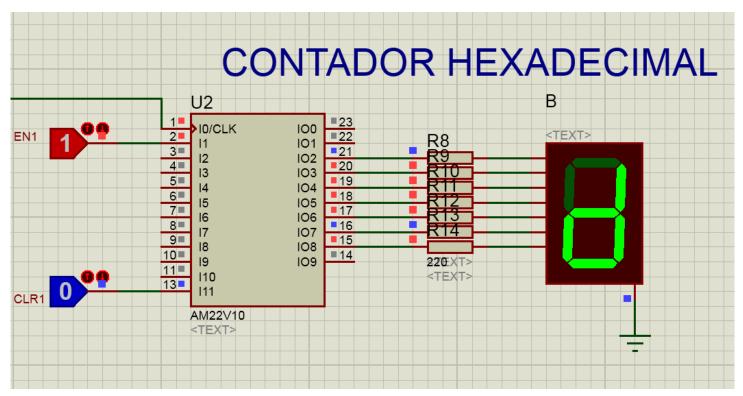






## 2) Contador Hexadecimal

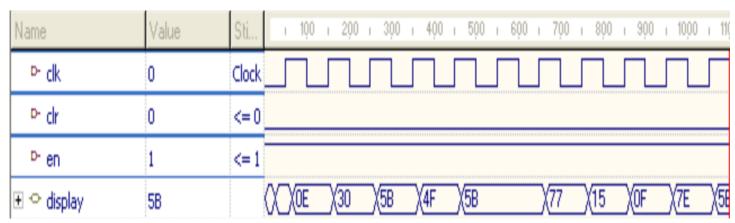


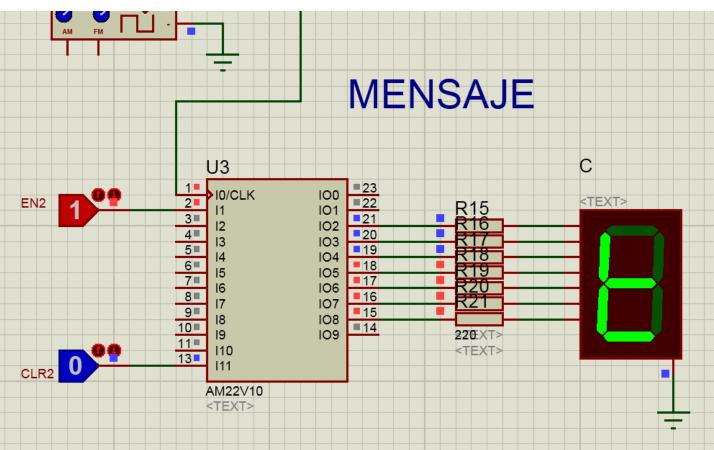






## 3) Mensaje (con letras repetidas)

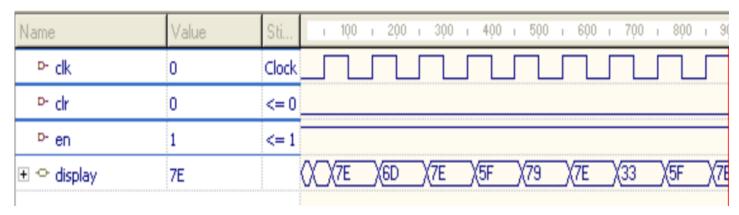


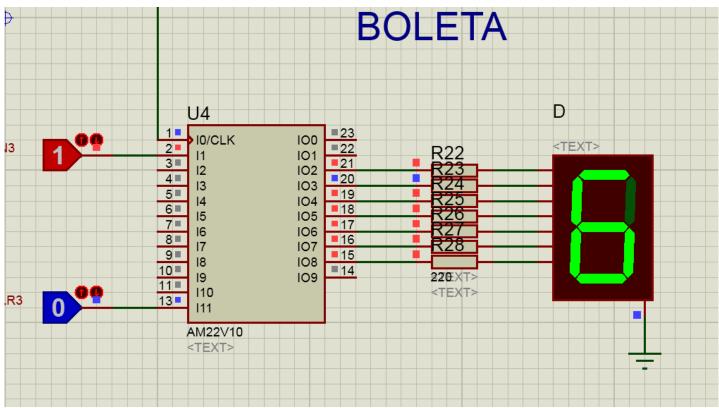






## 4) Boleta alumno









#### **CUESTIONARIO:**

- ¿Cuántos dispositivos PLD 22V10 son necesarios para el desarrollo de esta práctica?
   R= 1 dispositivo PLD 22V10.
- 2. ¿Cuántos dispositivos de la serie 74xx (TTL) ó 40xx (CMOS) hubieras necesitado para el desarrollo de esta práctica?
  - R= 1 555, 5 FF's 4023, 1 74ls139, 1 decodificador 7447, 12 7408, 12 7432, 12 7404
- ¿Cuántos pines de entrada/salida del PLD 22V10 se usan en los diseños?
   R= 3 pines de entrada y 7 de salida.
- 4. ¿Cuántos términos producto ocupan las ecuaciones para cada señal de salida y que porcentaje se usa en total del PLD 22V10 en cada aplicación?
  R= Para el programa de los dados se ocupan 28 términos producto y un 45% del PLD, para el contador hexadecimal se ocupan 43 términos producto y un 45% del PLD, para el mensaje se ocupan 36 términos producto y un 54% del PLD, para la boleta del alumno se ocupan 33 términos producto y un 54% del PLD.
- 5. ¿Es posible implementar los diseños usando cualquier tipo de codificación en el PLD22V10? R= Si, considerando el número de entradas y salidas del PLD que estés utilizando.
- 6. ¿Cuáles son las señales que funcionan de manera síncrona y cuáles de manera asíncrona? R= clear es asíncrona, enable es síncrona.
- 7. ¿Qué puedes concluir de esta práctica?

  R= Vimos distintas formas de usar los tipos de código para la implementación de un diseño con componentes limitadas usando nuevos comandos para facilitar la codificación.