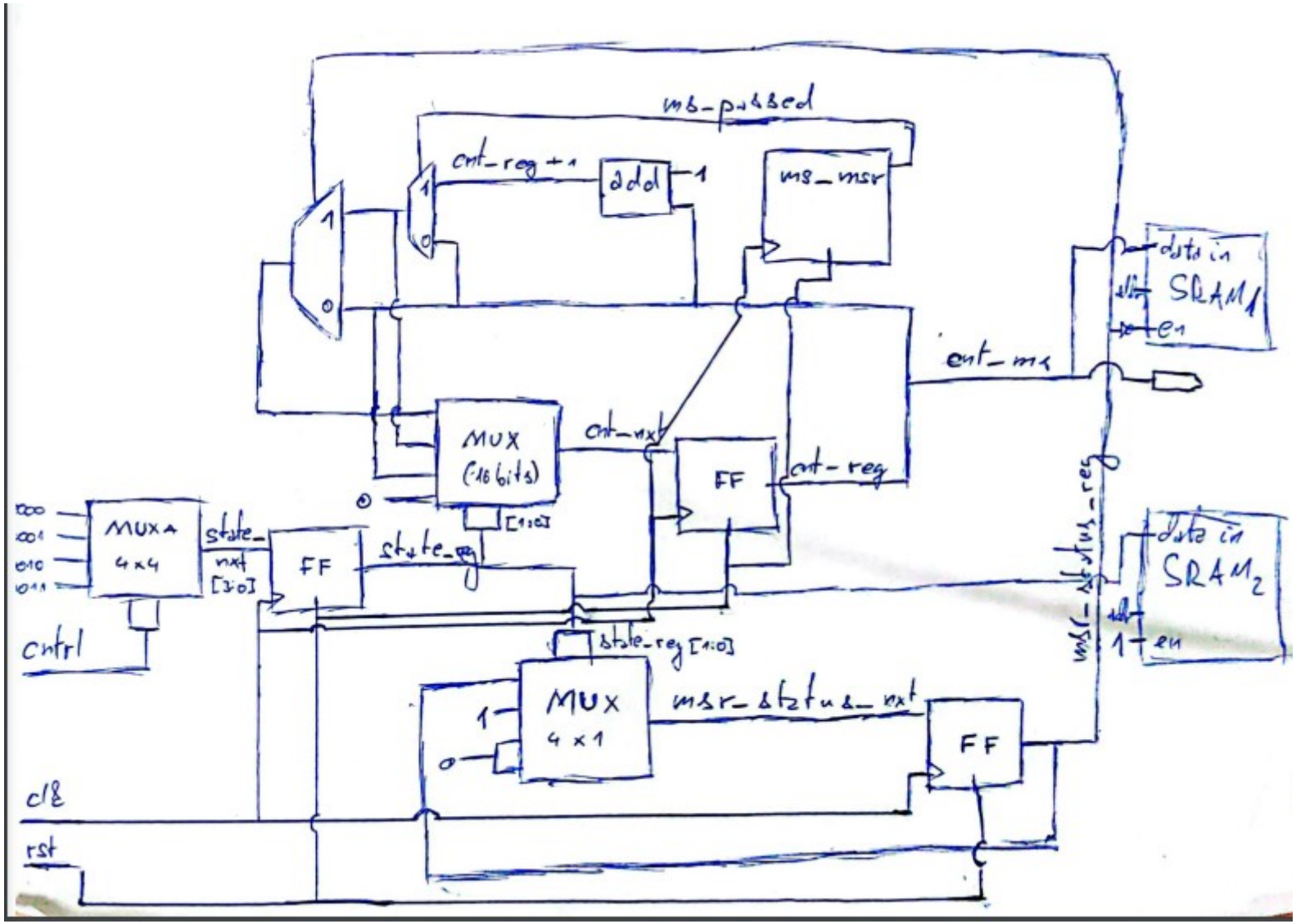
## Code:

```
module sram_memory_1port(       clk,
                        addr_in,
                        data_in,
                       data_out,
                         wr_en);
 input                                clk;
 input    [9 :0]  addr_in;
 input    [31:0]  data_in;

 output reg [31:0] data_out;

 input                          wr_en;

 reg [31:0] ram_memory [1023:0];

 always @ (posedge clk) begin
  if (wr_en)       ram_memory [addr_in] <= data_in;
  data_out <= ram_memory [addr_in];
 end

endmodule
```

## Scheme:


ms_pulsed
cnt_reg + 1
add
1
ms_msr
data in
SRAM1
en
cnt_ms
MUX
(16 bits)
cnt_nxt
FF
cnt_reg
MUX4
4x4
state_
nxt
[1:0]
FF
state_reg
state_reg [1:0]
cntrl
msr_status_reg
data in
SRAM2
1
en
MUX
4 x 1
msr_status_nxt
FF
clk
rst