**Code:**

module sram\_memory\_1port( clk,

addr\_in,

data\_in,

data\_out,

wr\_en);

input clk;

input [9 :0] addr\_in;

input [31:0] data\_in;

output reg [31:0] data\_out;

input wr\_en;

reg [31:0] ram\_memory [1023:0];

always @ (posedge clk) begin

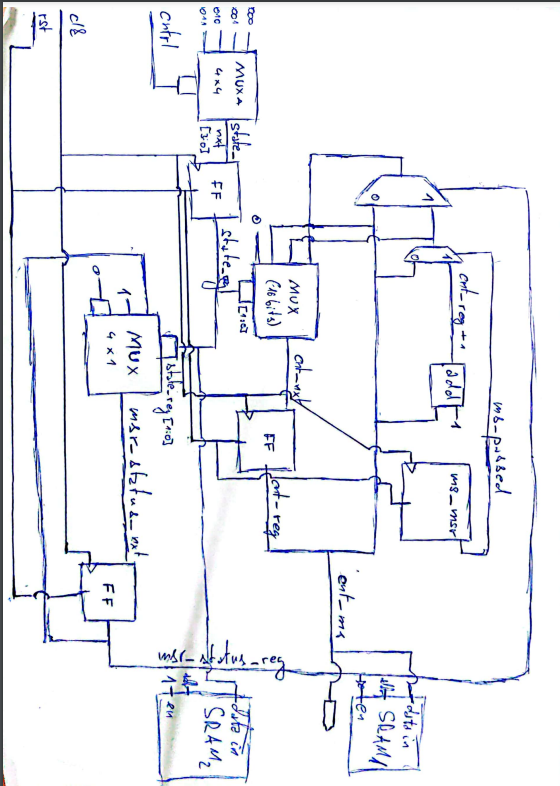
if (wr\_en) ram\_memory [addr\_in] <= data\_in;

data\_out <= ram\_memory [addr\_in];

end

endmodule

**Scheme:**

****