# Datasheet: `AppleIIcSlotMaker` Address Decoder and Control IC

## General Description

The `AppleIIcSlotMaker` is a programmable address decoder and control logic device implemented in a `p22v10` PLD. Designed for systems like the 6502 microprocessor, it decodes specific address ranges from a 16-bit address bus and generates **active-low** control signals (`IOSEL`, `DEVSEL`, `IOSTROBE`) for managing memory and I/O access. **IOSEL** enables ROM access within a 256-byte range, **DEVSEL** enables a 16-byte I/O space, and **IOSTROBE** enables mapping of addresses into the system's memory space when the internal state (`Q`) logic conditions are met.

The internal state of `Q` is maintained via feedback and is influenced by the active-low `RESET` signal, an internal combinatorial reset (`CRESET`), and the assertion of `IOSEL`. The device uses **CPIN** to define relevant address ranges, representing A12–A15 = `0xC`.

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## Features

- **Active-Low Control Signals**:
  - `IOSEL`: Enables ROM access for 256 bytes.
  - `DEVSEL`: Enables I/O access for 16 bytes.
  - `IOSTROBE`: Enables memory mapping for the range `0xC800–0xCFFF` when conditions are met.
- **Internal State (`Q`)**:
  - Set by `IOSEL` assertion.
  - Cleared by active `RESET`, internal combinatorial reset (`CRESET`), or specific address access.
- **RESET Signal**: External reset signal clears internal state.
- **Internal CRESET Logic**: Reset triggered by access to specific address ranges.
- **Compatible with 6502 Addressing**: Decodes address bus signals for memory-mapped I/O and ROM.

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# Pin Configuration

## Grouped Inputs

### Control Pins

| Pin | Name | Description |
|---|---|---|
| 1 | PH0 | Phase 0 clock signal. Indicates the address is stable. |
| 15 | SET | Set signal for internal state logic |
| 16 | RESET | External reset signal, clears internal state (active-low). |
| 17 | Q | Internal state bit |

### Address Bus

| Pin | Name | Description |
|---|---|---|
| 2–11 | A0–A9 | Lower 10 bits of the address bus |
| 13 | A10 | Address bit 10 |
| 14 | A11 | Address bit 11 |
| 18 | CPIN | Upper nibble of the 16-bit address bus (A12–A15) |

## Outputs

| Pin | Name | Description |
|---|---|---|
| 19 | IOSEL | ROM selection signal (active-low) |
| 20 | DEVSEL | Device I/O selection signal (active-low) |
| 21 | IOSTROBE | Address mapping enable signal (active-low) |

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# Functional Description

## 1. I/O Selection (`IOSEL`)

- **Active-Low Signal**: `IOSEL = 0` enables ROM access.
- Activated when:
  - **CPIN** = `1` (A12–A15 = `1100`).
  - Address Bits A8–A11 (`AH`) = `0100`.

**Address Range**: `0xC400–0xC4FF` (256 bytes).

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## 2. Device Selection (`DEVSEL`)

- **Active-Low Signal**: `DEVSEL = 0` enables I/O access.
- Activated when:
    - **CPIN** = `1` (A12–A15 = `1100`).
    - Address Bits A4–A7 (`AM`) = `1111`.
    - Address Bits A8–A11 (`AH`) = `0000`.

**Address Range**: `0xC0F0–0xC0FF` (16 bytes).

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## 3. I/O Strobe (`IOSTROBE`)

- **Active-Low Signal**: `IOSTROBE = 0` enables mapping of addresses in the range `0xC800–0xCFFF` into the system's memory space.
- Activated under these conditions:
    1. **CPIN** = `1` (A12–A15 = `1100`).
    2. Address Bits A8–A11 (`AH`) = `1000–1111`.
    3. Internal State (`Q`) is high.
        - `Q` is set by the assertion of `IOSEL`.
        - `Q` is cleared by an active `RESET`, `CRESET`, or access to `0xCFFF`.

**Address Range**: `0xC800–0xCFFF`.

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## 4. RESET Logic

- **RESET**: An external active-low signal clears the internal state (`Q`).
- **CRESET**: Internal combinatorial reset condition:

```
cupl
Copy code
CRESET = !(CPIN & AM:'h'F & AH:'h'F);
```

    - Asserts when:
        - **CPIN = 1** (A12–A15 = `1100`).
        - **AM = 0xF** (A4–A7 = `1111`).
        - **AH = 0xF** (A8–A11 = `1111`).

**Address Range for CRESET Activation**: `0xCFFF`.

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# Logic Truth Table

| Address Range | CPIN (A12–A15) | A8–A11 (AH) | A4–A7 (AM) | Q | Signal State |
|---|---|---|---|---|---|
| `0xC400–0xC4FF` | `1` | `0x4` | Any | Any | IOSEL = Active (0), Q Set |
| `0xC0F0–0xC0FF` | `1` | `0x0` | `0xF` | Any | DEVSEL = Active (0) |
| `0xC800–0xCFFF` | `1` | `0x8–0xF` | Any | High | IOSTROBE = Active (0) |
| `0xCFFF` | `1` | `0xF` | `0xF` | Any | RESET = Active (0), Q Cleared |

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# Behavior of `Q` (Internal State)

## Q Logic

The internal state `Q` is influenced by the following logic:

```
cupl
Copy code
Q = (Q & RESET & CRESET) # !IOSEL;
```

1. **Setting `Q`**:
   - `Q` is set when `IOSEL` is asserted (`IOSEL = 0`).
   - Address Range: `0xC400–0xC4FF`.
2. **Holding `Q`**:
   - `Q` maintains its current state if both `RESET` and `CRESET` are active (`RESET = 1` and `CRESET = 1`) and no conditions clear it.
3. **Clearing `Q`**:
   - `Q` is cleared by:
     - `RESET = 0`.
     - `CRESET = 0` (access to `0xCFFF`).

- Accessing `0xCFFF`.

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# Example Use Cases

## Accessing ROM (`IOSEL`)

- Write or read from an address in the range `0xC400–0xC4FF`.
- Set **CPIN** = `1`.

## Accessing Device I/O (`DEVSEL`)

- Write or read from an address in the range `0xC0F0–0xC0FF`.
- Set **CPIN** = `1`.

## Enabling Memory Mapping (`IOSTROBE`)

- Access an address in the range `0xC800–0xCFFF`.
- Ensure `Q` is high (set by accessing `0xC400–0xC4FF`).
- Set **CPIN** = `1`.

## Resetting Internal State (`RESET`)

- Use an external signal (`RESET = 0`) or access the address `0xCFFF` to activate `CRESET`.

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# Electrical Specifications

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Input Voltage | 0 | 5 | V |
| Output Voltage | 0 | 5 | V |
| Clock Frequency | 1 | 50 | MHz |
| Operating Temp | 0 | 70 | °C |

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## Pinout Diagram

```sql
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       +---------------------+
```

```
   PH0 |  1              24  | VCC
    A0 |  2              23  | GND
    A1 |  3              22  | NC
    A2 |  4              21  | IOSTROBE
    A3 |  5              20  | DEVSEL
    A4 |  6              19  | IOSEL
    A5 |  7              18  | CPIN
    A6 |  8              17  | Q
    A7 |  9              16  | RESET
    A8 | 10              15  | SET
    A9 | 11              14  | A11
   A10 | 13              12  | A10
       +--------------------+
```