Datasheet: `AppleIIcSlotMaker` Address Decoder and Control IC

General Description

The `AppleIIcSlotMaker` is a programmable address decoder and control logic device implemented in a `p22v10` PLD. Designed for systems like the 6502 microprocessor, it decodes specific address ranges from a 16-bit address bus and generates **active-low** control signals (`IOSEL`, `DEVSEL`, `IOSTROBE`) for managing memory and I/O access. **IOSEL** enables ROM access within a 256-byte range, **DEVSEL** enables a 16-byte I/O space, and **IOSTROBE** enables mapping of memory addresses into the system's address space based on internal state (`Q`) logic.

The internal state of `Q` is maintained via feedback and influenced by the active-low `RESET` signal and the assertion of `IOSEL`. The device uses **CPIN** to define relevant address ranges, representing A12–A15 = `0xC`.

Features

- **Active-Low Control Signals**:
    - `IOSEL`: Enables ROM access for 256 bytes.
    - `DEVSEL`: Enables I/O access for 16 bytes.
    - `IOSTROBE`: Enables memory mapping when conditions are met.
- **Internal State (`Q`)**:
    - Set by `IOSEL` assertion.
    - Cleared by active `RESET` or specific address conditions.
- **RESET Signal**: Clears the internal state (`Q`).
- **Compatible with 6502 Addressing**: Decodes address bus signals for memory-mapped I/O and ROM.

Pin Configuration

Grouped Inputs

Control Pins

Pin	Name	Description
1	PH0	Phase 0 clock signal. Indicates the address is stable.
15	SET	Set signal for internal state logic
16	RESET	Reset signal, clears internal state
17	Q	Internal state bit

Address Bus

Pin	Name	Description
2–11	A0–A9	Lower 10 bits of the address bus
13	A10	Address bit 10
14	A11	Address bit 11
18	CPIN	Upper nibble of the 16-bit address bus (A12–A15)

Outputs

Pin	Name	Description
19	IOSEL	ROM selection signal (active-low)
20	DEVSEL	Device I/O selection signal (active-low)
21	IOSTROBE	Address mapping enable signal (active-low)

Functional Description

1. I/O Selection (`IOSEL`)

- **Active-Low Signal**: `IOSEL = 0` enables ROM access.
- Activated when:
    - **CPIN** = `1` (A12–A15 = `1100`).
    - Address Bits A8–A11 (AH) = `0100`.

Address Range: `0xC400–0xC4FF` (256 bytes).

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2. Device Selection (`DEVSEL`)

- **Active-Low Signal**: `DEVSEL = 0` enables I/O access.
- Activated when:
    - **CPIN** = 1 (A12–A15 = `1100`).
    - Address Bits A4–A7 (AM) = `1111`.
    - Address Bits A8–A11 (AH) = `0000`.

Address Range: `0xC0F0–0xC0FF` (16 bytes).

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3. I/O Strobe (`IOSTROBE`)

- **Active-Low Signal**: `IOSTROBE = 0` enables mapping of addresses in the range `0xC800–0xCFFF` into the system's memory space.
- Activated under these conditions:
    1. **CPIN** = 1 (A12–A15 = `1100`).
    2. Address Bits A8–A11 (AH) = `1000–1111`.
    3. Internal State (`Q`) is high.
        - `Q` is set by the assertion of `IOSEL`.
        - `Q` is cleared by an active `RESET` or access to `0xCFF0–0xCFFF`.

Address Range: `0xC800–0xCFFF`.

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4. RESET Signal

- **Active-Low Signal**: `RESET = 0` clears internal state (`Q`).
- Activated when:
    - **CPIN** = 1 (A12–A15 = `1100`).
    - Address Bits A4–A11 (AM and AH) = `1111`.

Address Range: `0xCFF0–0xCFFF`.

Logic Truth Table

Address Range	CPIN (A12–A15)	A8–A11 (AH)	A4–A7 (AM)	Q	Signal State
0xC400–0xC4FF	1	0x4	Any	Any	IOSEL = Active (0), Q Set
0xC0F0–0xC0FF	1	0x0	0xF	Any	DEVSEL = Active (0)
0xC800–0xCFFF	1	0x8–0xF	Any	High	IOSTROBE = Active (0)
0xCFF0–0xCFFF	1	0xF	0xF	Any	RESET = Active (0), Q Cleared

Behavior of Q (Internal State)

Q Logic

The internal state Q is influenced by the following logic:

```cupl
Copy code
Q = (Q & RESET) # !IOSEL;
```

1. **Setting Q**:

   - Q is set when IOSEL is asserted (IOSEL = 0).
   - Address Range: 0xC400–0xC4FF.

2. **Holding Q**:

   - Q maintains its current state if RESET = 1 (inactive) and no conditions clear it.

3. **Clearing Q**:

   - RESET clears Q when asserted (RESET = 0).
   - Accessing the range 0xCFF0–0xCFFF also clears Q.

Example Use Cases

Accessing ROM (`IOSEL`)

- Write or read from an address in the range `0xC400–0xC4FF`.
- Set **CPIN** = 1.

Accessing Device I/O (`DEVSEL`)

- Write or read from an address in the range `0xC0F0–0xC0FF`.
- Set **CPIN** = 1.

Enabling Memory Mapping (`IOSTROBE`)

- Access an address in the range `0xC800–0xCFFF`.
- Ensure `Q` is high (set by accessing `0xC400–0xC4FF`).
- Set **CPIN** = 1.

Resetting Internal State (`RESET`)

- Write or read from an address in the range `0xCFF0–0xCFFF`.
- Set **CPIN** = 1.

Electrical Specifications

Parameter	Min	Max	Unit
Input Voltage	0	5	V
Output Voltage	0	5	V
Clock Frequency	1	50	MHz
Operating Temp	0	70	°C

Pinout Diagram

```sql
Copy code
         +--------------------+
  PH0  |  1               24  | VCC
   A0  |  2               23  | GND
   A1  |  3               22  | NC
   A2  |  4               21  | IOSTROBE
   A3  |  5               20  | DEVSEL
   A4  |  6               19  | IOSEL
   A5  |  7               18  | CPIN
   A6  |  8               17  | Q
   A7  |  9               16  | RESET
   A8  | 10               15  | SET
   A9  | 11               14  | A11
  A10  | 13               12  | A10
         +--------------------+
```